

TSOP
Commercial Temp
Industrial Temp

256K x 8 2Mb Asynchronous SRAM

7, 8, 10, 12 ns
3.3 V V_{DD}
Center V_{DD} and V_{SS}

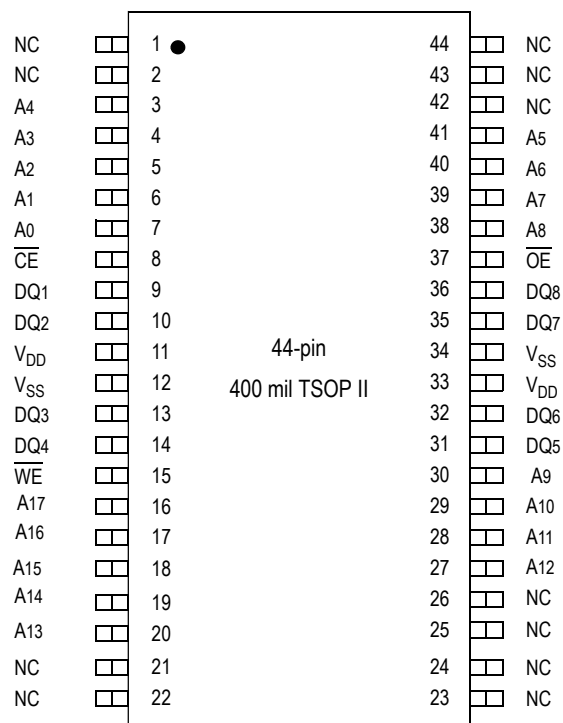
Features

- Fast access time: 7, 8, 10, 12 ns
- CMOS low power operation: 135/115/95/80 mA at minimum cycle time
- Single 3.3 V power supply
- All inputs and outputs are TTL-compatible
- Fully static operation
- Industrial Temperature Option: -40° to 85°C
- Package line up
 - TP: 400 mil, 44-pin TSOP Type II package
 - GP: RoHS-compliant 400 mil, 44-pin TSOP Type II package

Description

The GS72108A is a high speed CMOS Static RAM organized as 262,144 words by 8 bits. Static design eliminates the need for external clocks or timing strobes. The GS operates on a single 3.3 V power supply and all inputs and outputs are TTL-compatible. The GS72108A is available in 400 mil TSOP Type-II packages.

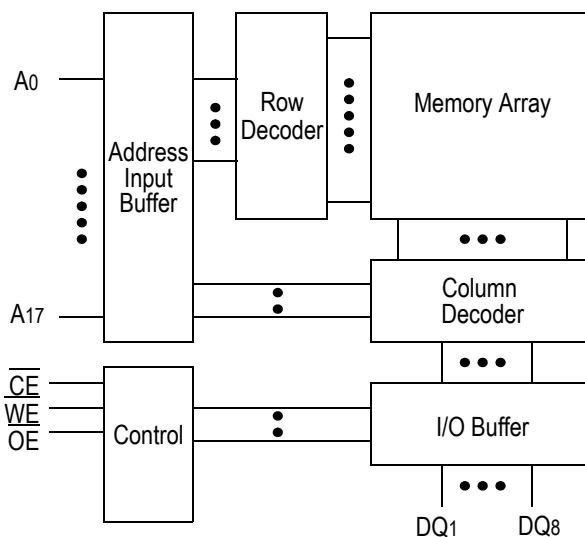
TSOP-II 256K x 8-Pin Configuration



Pin Descriptions

Symbol	Description
A ₀ –A ₁₇	Address input
DQ ₁ –DQ ₈	Data input/output
$\overline{\text{CE}}$	Chip enable input
$\overline{\text{WE}}$	Write enable input
$\overline{\text{OE}}$	Output enable input
V_{DD}	+3.3 V power supply
V_{SS}	Ground
NC	No connect

Block Diagram



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ1 to DQ8	V_{DD} Current
H	X	X	Not Selected	ISB1, ISB2
L	L	H	Read	IDD
L	X	L	Write	
L	H	H	High Z	

Note:

X: "H" or "L"

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V _{DD}	−0.5 to +4.6	V
Input Voltage	V _{IN}	−0.5 to V _{DD} +0.5 (≤ 4.6 V max.)	V
Output Voltage	V _{OUT}	−0.5 to V _{DD} +0.5 (≤ 4.6 V max.)	V
Allowable power dissipation	PD	0.7	W
Storage temperature	T _{STG}	−55 to 150	°C

Note:

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for -7/-8/-10/-12	V_{DD}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	—	$V_{DD} + 0.3$	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V
Ambient Temperature, Commercial Range	T_{Ac}	0	—	70	°C
Ambient Temperature, Industrial Range	T_{AI}	-40	—	85	°C

Notes:

- Input overshoot voltage should be less than $V_{DD} + 2$ V and not exceed 20 ns.
- Input undershoot voltage should be greater than -2 V and not exceed 20 ns.

Capacitance

Parameter	Symbol	Test Condition	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0$ V	5	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0$ V	7	pF

Notes:

- Tested at $T_A = 25^{\circ}\text{C}$, $f = 1$ MHz
- These parameters are sampled and are not 100% tested.

DC I/O Pin Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current	I_{IL}	$V_{IN} = 0$ to V_{DD}	-1 μA	1 μA
Output Leakage Current	I_{LO}	Output High Z $V_{OUT} = 0$ to V_{DD}	-1 μA	1 μA
Output High Voltage	V_{OH}	$I_{OH} = -4\text{mA}$	2.4	—
Output Low Voltage	V_{OL}	$I_{LO} = +4\text{mA}$	—	0.4 V

Power Supply Currents

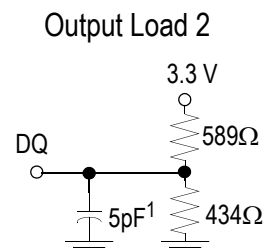
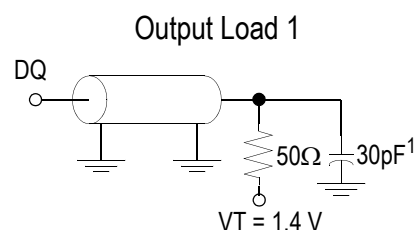
Parameter	Symbol	Test Conditions	0 to 70°C				-40 to 85°C			
			7 ns	8 ns	10 ns	12 ns	7 ns	8 ns	10 ns	12 ns
Operating Supply Current	$I_{DD}(\text{max})$	$\overline{CE} \leq V_{IL}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time $I_{OUT} = 0 \text{ mA}$	135 mA	115 mA	95 mA	80 mA	140 mA	120 mA	100 mA	85 mA
Standby Current	$I_{SB1}(\text{max})$	$\overline{CE} \geq V_{IH}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time	25 mA	20 mA	20 mA	15 mA	30 mA	25 mA	25 mA	20 mA
Standby Current	$I_{SB2}(\text{max})$	$\overline{CE} \geq V_{DD} - 0.2 \text{ V}$ All other inputs $\geq V_{DD} - 0.2 \text{ V}$ or $\leq 0.2 \text{ V}$	5 mA				10 mA			

AC Test Conditions

Parameter	Conditions
Input high level	$V_{IH} = 2.4 \text{ V}$
Input low level	$V_{IL} = 0.4 \text{ V}$
Input rise time	$t_r = 1 \text{ V/ns}$
Input fall time	$t_f = 1 \text{ V/ns}$
Input reference level	1.4 V
Output reference level	1.4 V
Output load	Fig. 1& 2

Notes:

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Output load 2 for t_{LZ} , t_{HZ} , t_{OLZ} and t_{OHZ}



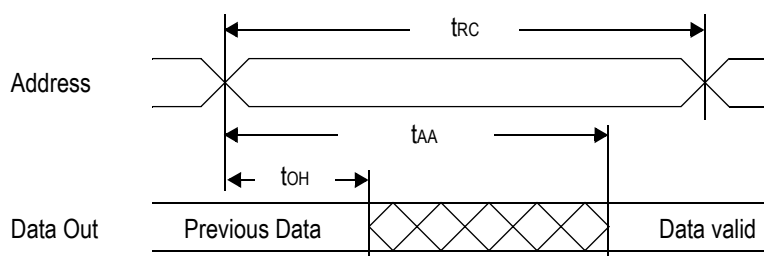
AC Characteristics

Read Cycle

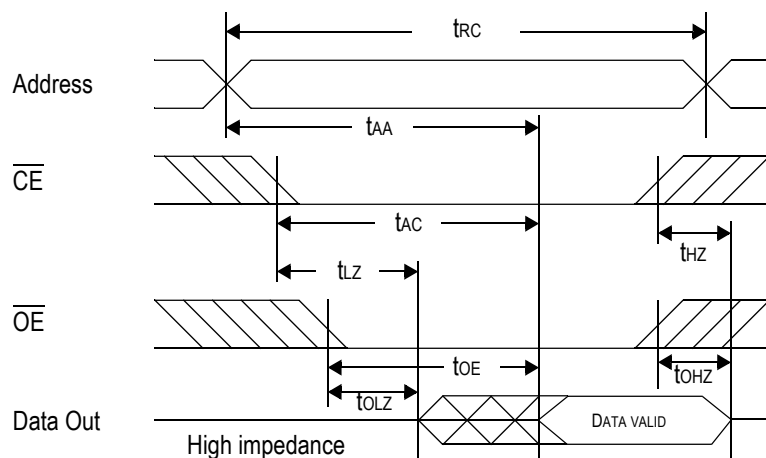
Parameter	Symbol	-7		-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	7	—	8	—	10	—	12	—	ns
Address access time	t_{AA}	—	7	—	8	—	10	—	12	ns
Chip enable access time ($\overline{CE}$)	t_{AC}	—	7	—	8	—	10	—	12	ns
Byte enable access time ($\overline{UB}$, $\overline{LB}$)	t_{AB}	—	3	—	3.5	—	4	—	5	ns
Output enable to output valid ($\overline{OE}$)	t_{OE}	—	3	—	3.5	—	4	—	5	ns
Output hold from address change	t_{OH}	3	—	3	—	3	—	3	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}^*	3	—	3	—	3	—	3	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}^*	0	—	0	—	0	—	0	—	ns
Byte enable to output in low Z ($\overline{UB}$, $\overline{LB}$)	t_{BLZ}^*	0	—	0	—	0	—	0	—	ns
Chip disable to output in High Z ($\overline{CE}$)	t_{HZ}^*	—	3.5	—	4	—	5	—	6	ns
Output disable to output in High Z ($\overline{OE}$)	t_{OHZ}^*	—	3	—	3.5	—	4	—	5	ns

* These parameters are sampled and are not 100% tested.

Read Cycle 1: $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$



Read Cycle 2: $\overline{WE} = V_{IH}$

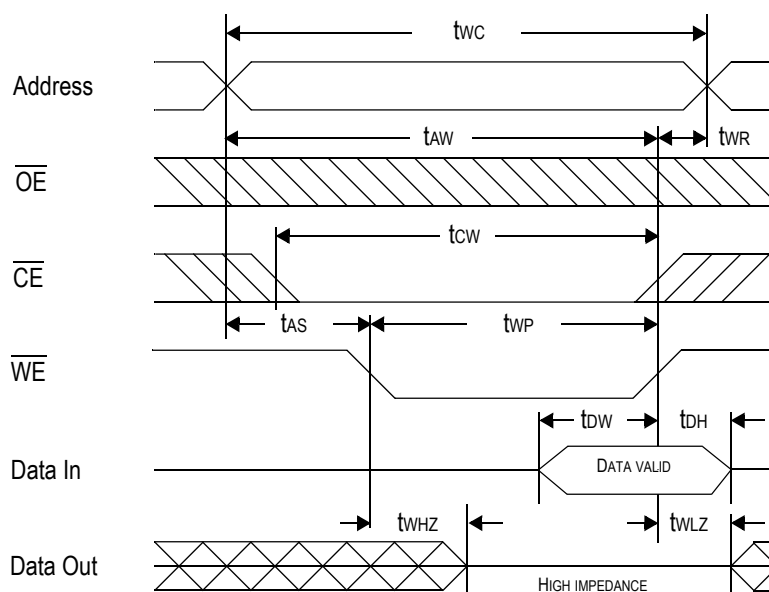


Write Cycle

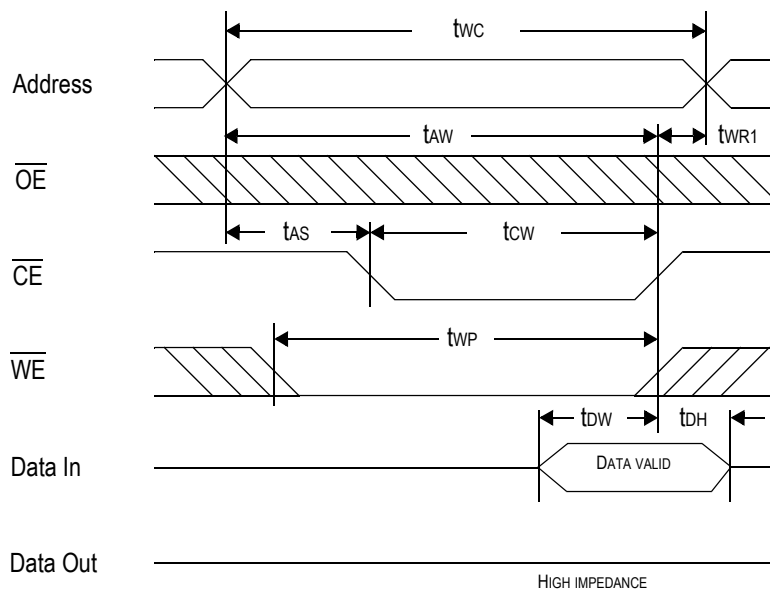
Parameter	Symbol	-7		-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write cycle time	tWC	7	—	8	—	10	—	12	—	ns
Address valid to end of write	tAW	5	—	5.5	—	7	—	8	—	ns
Chip enable to end of write	tCW	5	—	5.5	—	7	—	8	—	ns
Data set up time	tDW	3.5	—	4	—	5	—	6	—	ns
Data hold time	tDH	0	—	0	—	0	—	0	—	ns
Write pulse width	tWP	5	—	5.5	—	7	—	8	—	ns
Address set up time	tAS	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	tWR	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	tWR1	0	—	0	—	0	—	0	—	ns
Output Low Z from end of write	tWLZ*	3	—	3	—	3	—	3	—	ns
Write to output in High Z	tWHZ*	—	3	—	3.5	—	4	—	5	ns

* These parameters are sampled and are not 100% tested.

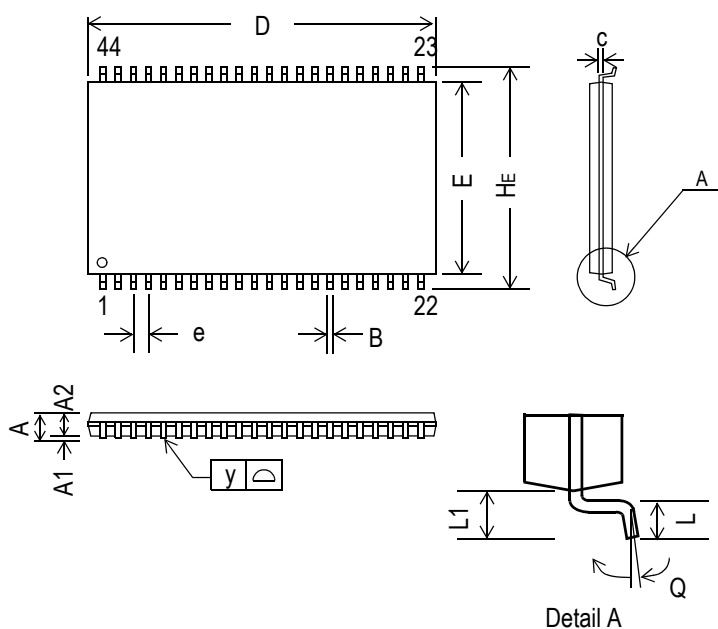
Write Cycle 1: $\overline{WE}$ control



Write Cycle 2: $\overline{CE}$ control



44-Pin, 400 mil TSOP-II



Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	—	—	0.047	—	—	1.20
A1	0.002	—	—	0.05	—	—
A2	0.037	0.039	0.041	0.95	1.00	1.05
B	0.01	0.014	0.018	0.25	0.35	0.45
c	—	0.006	—	—	0.15	—
D	0.721	0.725	0.729	18.31	18.41	18.51
E	0.396	0.400	0.404	10.06	10.16	10.26
e	—	0.031	—	—	0.80	—
HE	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
L1	—	0.031	—	—	0.80	—
y	—	—	0.004	—	—	0.10
Q	0°	—	5°	0°	—	5°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension B does not include dambar protrusion/intrusion.
3. Controlling dimension: mm

Ordering Information

Part Number*	Package	Access Time	Temp. Range
GS72108ATP-7	400 mil TSOP-II	7 ns	Commercial
GS72108ATP-8	400 mil TSOP-II	8 ns	Commercial
GS72108ATP-10	400 mil TSOP-II	10 ns	Commercial
GS72108ATP-12	400 mil TSOP-II	12 ns	Commercial
GS72108ATP78I	400 mil TSOP-II	7 ns	Industrial
GS72108ATP-8I	400 mil TSOP-II	8 ns	Industrial
GS72108ATP-10I	400 mil TSOP-II	10 ns	Industrial
GS72108ATP-12I	400 mil TSOP-II	12 ns	Industrial
GS72108AGP-7	RoHS-compliant 400 mil TSOP-II	7 ns	Commercial
GS72108AGP-8	RoHS-compliant 400 mil TSOP-II	8 ns	Commercial
GS72108AGP-10	RoHS-compliant 400 mil TSOP-II	10 ns	Commercial
GS72108AGP-12	RoHS-compliant 400 mil TSOP-II	12 ns	Commercial
GS72108AGP78I	RoHS-compliant 400 mil TSOP-II	7 ns	Industrial
GS72108AGTP-8I	RoHS-compliant 400 mil TSOP-II	8 ns	Industrial
GS72108AGP-10I	RoHS-compliant 400 mil TSOP-II	10 ns	Industrial
GS72108AGP-12I	RoHS-compliant 400 mil TSOP-II	12 ns	Industrial

Notes:

- Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. For example: GS72108TP-8T.

2Mb Asynchronous Datasheet Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Revisions/Reason
72108A_r1		• Creation of new datasheet
72108A_r1; 72108A_r1_01	Content	• Added 6 ns speed bin • Updated all power numbers
72108A_r1_01; 72108A_r1_02	Content	• Updated Recommended Operating Conditions table on page 4 • Changed FPBGA package from 6 x 10 to 6 x 8 (package U)
72108A_r1_02; 72108A_r1_03	Content	• Removed all references to "U" package
72108A_r1_03; 72108A_r1_04	Content	• Removed 6 ns speed bin from entire document • Added 7 ns speed bin to entire document
72108A_r1_04; 72108A_r1_05	Content	• Updated format • Added RoHS-compliant information for TSOP-II package
72108A_r1_05; 72108A_r1_06	Content	• Added RoHS-compliant 400 mil SOJ
72108A_r1_06; 72108A_r1_07	Content	• Updated to MP in ordering information table • Rev. 1.07a: Removed SOJ package references, removed Status Column from Ordering Information table