RoHS-compliant 260-Ball BGA
Commercial Temp
Industrial Temp

72Mb SigmaDDR-IIIe™ Burst of 2 ECCRAM™

675 MHz–500 MHz
1.35 V V_{DD}
1.2 V to 1.5 V V_{DDQ}

Features

- On-Chip ECC with virtually zero SER
- Configurable Read Latency (3.0 or 2.0 cycles)
- Simultaneous Read and Write SigmaDDR-IIIe™ Interface
- Common I/O Bus
- Double Data Rate interface
- Burst of 2 Read and Write
- Pipelined read operation
- Fully coherent Read and Write pipelines
- 1.35 V nominal V_{DD}
- 1.2 V JESD8-16A BIC-3 Compliant Interface
- 1.5 V HSTL Interface
- ZQ pin for programmable output drive impedance
- ZT for programmable input termination impedance
- Configurable Input Termination
- IEEE 1149.1 JTAG-compliant Boundary Scan
- 260-ball, 14 mm x 22 mm, 1 mm ball pitch BGA package
  - –GK: 6/6 RoHS-compliant package

SigmaDDR-IIIe™ Family Overview

The SigmaDDR-IIIe family of SRAMs are the Common I/O half of the SigmaQuad-IIIe/SigmaDDR-IIIe family of high performance SRAMs. Although very similar to GSI's second generation of networking SRAMs, the SigmaQuad-II/ SigmaDDR-II family, this third generation family of SRAMs offers new features that allow much higher speeds, such as user-configurable on-die input termination, improved output signal integrity, and adjustable pipeline length.

Clocking and Addressing Schemes

The GS8673ET18/36BGK SigmaDDR-IIIe ECCRAMs are synchronous devices. They employ dual, single-ended master clocks, CK and $\overline{CK}$. These clocks are single-ended clock inputs, not differential inputs to a single differential clock input buffer. CK and $\overline{CK}$ are used to control the address and control input registers, as well as all output timing.

The KD and $\overline{KD}$ clocks are dual mesochronous (with respect to CK and $\overline{CK}$) input clocks that are used solely to control the data input registers. Consequently, data input setup and hold windows can be optimized independently of address and control input setup and hold windows.

Each internal read and write operation in a SigmaDDR-IIIe B2 ECCRAM is two times wider than the device I/O bus. An input data bus de-multiplexer is used to accumulate incoming data before it is simultaneously written to the memory array. An output data multiplexer is used to capture the data produced from a single memory array read and then route it to the appropriate output drivers as needed. Therefore, the address field of a SigmaDDR-IIIe B2 ECCRAM is always one address pin less than the advertised index depth (e.g. the 4M x 18 has 2M addressable index).

On-Chip Error Correction Code

GSI's ECCRAMs implement an ECC algorithm that detects and corrects all single-bit memory errors, including those induced by Soft Error Rate (SER) events such as cosmic rays, alpha particles, etc. The resulting SER of these devices is anticipated to be <0.002 FITs/Mb — a 5-order-of-magnitude improvement over comparable SRAMs with no On-Chip ECC, which typically have an SER of 200 FITs/Mb or more. SER quoted above is based on reading taken at sea level.

Parameter Synopsis

Speed Bin	Operating Frequency	Data Rate (per pin)	Read Latency	V_{DD}
-675	675 / 450 MHz	1350 / 900 Mbps	3.0 / 2.0	1.3V to 1.4V
-625	625 / 400 MHz	1250 / 800 Mbps	3.0 / 2.0	1.3V to 1.4V
-550	550 / 375 MHz	1100 / 750 Mbps	3.0 / 2.0	1.25V to 1.4V
-500	500 / 333 MHz	1000 / 666 Mbps	3.0 / 2.0	1.25V to 1.4V

4M x 18 (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	V_{DD}	V_{DDQ}	V_{DD}	V_{DDQ}	MCL	MCH (CFG)	MCL	ZQ	PZT1	V_{DDQ}	V_{DD}	V_{DDQ}	V_{DD}
B	V_{SS}	NU_{IO}	V_{SS}	NU_I	MVQ	MCL	NC (RSVD)	MCL (SIOM)	PZT0	NU_I	V_{SS}	DQ0	V_{SS}
C	DQ17	V_{DDQ}	NU_I	V_{DDQ}	V_{SS}	SA	V_{DD}	SA	V_{SS}	V_{DDQ}	NU_I	V_{DDQ}	NU_{IO}
D	V_{SS}	NU_{IO}	V_{SS}	NU_I	SA	V_{DDQ}	NC (288 Mb)	V_{DDQ}	NC (144 Mb)	NU_I	V_{SS}	DQ1	V_{SS}
E	DQ16	V_{DDQ}	NU_I	V_{DD}	V_{SS}	SA	V_{SS}	SA	V_{SS}	V_{DD}	NU_I	V_{DDQ}	NU_{IO}
F	V_{SS}	NU_{IO}	V_{SS}	NU_I	SA	V_{DD}	V_{DDQ}	V_{DD}	SA	NU_I	V_{SS}	DQ2	V_{SS}
G	DQ15	NU_{IO}	NU_I	NU_I	V_{SS}	SA	MZT1	SA	V_{SS}	NU_I	NU_I	DQ3	NU_{IO}
H	DQ14	V_{DDQ}	NU_I	V_{DDQ}	SA	V_{DDQ}	R/$\overline{W}$	V_{DDQ}	SA	V_{DDQ}	NU_I	V_{DDQ}	NU_{IO}
J	V_{SS}	NU_{IO}	V_{SS}	NU_I	V_{SS}	SA	V_{SS}	SA	V_{SS}	NU_I	V_{SS}	DQ4	V_{SS}
K	CQ1	V_{DDQ}	V_{REF}	V_{DD}	KD1	V_{DD}	CK	V_{DD}	KD0	V_{DD}	V_{REF}	V_{DDQ}	CQ0
L	$\overline{CQ1}$	V_{SS}	QVLD1	V_{SS}	$\overline{KD1}$	V_{DDQ}	$\overline{CK}$	V_{DDQ}	$\overline{KD0}$	V_{SS}	QVLD0	V_{SS}	$\overline{CQ0}$
M	V_{SS}	DQ13	V_{SS}	NU_I	V_{SS}	SA	V_{SS}	SA	V_{SS}	NU_I	V_{SS}	NU_{IO}	V_{SS}
N	NU_{IO}	V_{DDQ}	NU_I	V_{DDQ}	DLL	V_{DDQ}	$\overline{LD}$	V_{DDQ}	MCH	V_{DDQ}	NU_I	V_{DDQ}	DQ5
P	NU_{IO}	DQ12	NU_I	NU_I	V_{SS}	SA	MZT0	SA	V_{SS}	NU_I	NU_I	NU_{IO}	DQ6
R	V_{SS}	DQ11	V_{SS}	NU_I	MCH	V_{DD}	V_{DDQ}	V_{DD}	RST	NU_I	V_{SS}	NU_{IO}	V_{SS}
T	NU_{IO}	V_{DDQ}	NU_I	V_{DD}	V_{SS}	SA	V_{SS}	SA	V_{SS}	V_{DD}	NU_I	V_{DDQ}	DQ7
U	V_{SS}	DQ10	V_{SS}	NU_I	NU_I	V_{DDQ}	$\overline{AZT1}$	V_{DDQ}	NU_I	NU_I	V_{SS}	NU_{IO}	V_{SS}
V	NU_{IO}	V_{DDQ}	NU_I	V_{DDQ}	V_{SS}	SA (x18)	V_{DD}	SA (B2)	V_{SS}	V_{DDQ}	NU_I	V_{DDQ}	DQ8
W	V_{SS}	DQ9	V_{SS}	NU_I	TCK	RLM0	NC (RSVD)	MCL	TMS	NU_I	V_{SS}	NU_{IO}	V_{SS}
Y	V_{DD}	V_{DDQ}	V_{DD}	V_{DDQ}	TDO	ZT	RLM1	MCL	TDI	V_{DDQ}	V_{DD}	V_{DDQ}	V_{DD}

Notes:

1. Pins 5A, 7A, and 6B are reserved for future use. They must be tied Low.
2. Pins 9N and 5R are reserved for future use. They must be tied High in this device.
3. Pin 6A is defined as mode pin CFG in the pinout standard. It must be tied High in this device to select x18 configuration.
4. Pin 8B is defined as mode pin SIOM in the pinout standard. It must be tied Low in this device to select Common I/O configuration.
5. Pin 6V is defined as address pin SA for x18 devices. It is used in this device.
6. Pin 8V is defined as address pin SA for B2 devices. It is used in this device.
7. Pin 9D is reserved as address pin SA for 144Mb devices. It is a true no-connect in this device.
8. Pin 7D is reserved as address pin SA for 288Mb devices. It is a true no-connect in this device.
9. Pins 5U and 9U are unused in this device. They must be left unconnected or driven Low.
10. Pins 8W and 8Y are reserved for internal use only. They must be tied Low.
11. Pins 7B and 7W are reserved for future use. They are true no-connects in this device.

2M x 36 (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	V_{DD}	V_{DDQ}	V_{DD}	V_{DDQ}	MCL	MCL (CFG)	MCL	ZQ	PZT1	V_{DDQ}	V_{DD}	V_{DDQ}	V_{DD}
B	V_{SS}	DQ35	V_{SS}	NU_I	MVQ	MCL	NC (RSVD))	MCL (SIOM)	PZT0	NU_I	V_{SS}	DQ0	V_{SS}
C	DQ26	V_{DDQ}	NU_I	V_{DDQ}	V_{SS}	SA	V_{DD}	SA	V_{SS}	V_{DDQ}	NU_I	V_{DDQ}	DQ9
D	V_{SS}	DQ34	V_{SS}	NU_I	SA	V_{DDQ}	NC (288 Mb)	V_{DDQ}	NC (144 Mb)	NU_I	V_{SS}	DQ1	V_{SS}
E	DQ25	V_{DDQ}	NU_I	V_{DD}	V_{SS}	SA	V_{SS}	SA	V_{SS}	V_{DD}	NU_I	V_{DDQ}	DQ10
F	V_{SS}	DQ33	V_{SS}	NU_I	SA	V_{DD}	V_{DDQ}	V_{DD}	SA	NU_I	V_{SS}	DQ2	V_{SS}
G	DQ24	DQ32	NU_I	NU_I	V_{SS}	SA	MZT1	SA	V_{SS}	NU_I	NU_I	DQ3	DQ11
H	DQ23	V_{DDQ}	NU_I	V_{DDQ}	SA	V_{DDQ}	R/$\overline{W}$	V_{DDQ}	SA	V_{DDQ}	NU_I	V_{DDQ}	DQ12
J	V_{SS}	DQ31	V_{SS}	NU_I	V_{SS}	SA	V_{SS}	SA	V_{SS}	NU_I	V_{SS}	DQ4	V_{SS}
K	CQ1	V_{DDQ}	V_{REF}	V_{DD}	KD1	V_{DD}	CK	V_{DD}	KD0	V_{DD}	V_{REF}	V_{DDQ}	CQ0
L	$\overline{CQ}$1	V_{SS}	QVLD1	V_{SS}	$\overline{KD}$1	V_{DDQ}	$\overline{CK}$	V_{DDQ}	$\overline{KD}$0	V_{SS}	QVLD0	V_{SS}	$\overline{CQ}$0
M	V_{SS}	DQ22	V_{SS}	NU_I	V_{SS}	SA	V_{SS}	SA	V_{SS}	NU_I	V_{SS}	DQ13	V_{SS}
N	DQ30	V_{DDQ}	NU_I	V_{DDQ}	DLL	V_{DDQ}	$\overline{LD}$	V_{DDQ}	MCH	V_{DDQ}	NU_I	V_{DDQ}	DQ5
P	DQ29	DQ21	NU_I	NU_I	V_{SS}	SA	MZT0	SA	V_{SS}	NU_I	NU_I	DQ14	DQ6
R	V_{SS}	DQ20	V_{SS}	NU_I	MCH	V_{DD}	V_{DDQ}	V_{DD}	RST	NU_I	V_{SS}	DQ15	V_{SS}
T	DQ28	V_{DDQ}	NU_I	V_{DD}	V_{SS}	SA	V_{SS}	SA	V_{SS}	V_{DD}	NU_I	V_{DDQ}	DQ7
U	V_{SS}	DQ19	V_{SS}	NU_I	NU_I	V_{DDQ}	$\overline{AZT1}$	V_{DDQ}	NU_I	NU_I	V_{SS}	DQ16	V_{SS}
V	DQ27	V_{DDQ}	NU_I	V_{DDQ}	V_{SS}	NU_I (x18)	V_{DD}	SA (B2)	V_{SS}	V_{DDQ}	NU_I	V_{DDQ}	DQ8
W	V_{SS}	DQ18	V_{SS}	NU_I	TCK	RLM0	NC (RSVD)	MCL	TMS	NU_I	V_{SS}	DQ17	V_{SS}
Y	V_{DD}	V_{DDQ}	V_{DD}	V_{DDQ}	TDO	ZT	RLM1	MCL	TDI	V_{DDQ}	V_{DD}	V_{DDQ}	V_{DD}

Notes:

1. Pins 5A, 7A, and 6B are reserved for future use. They must be tied Low.
2. Pins 9N and 5R are reserved for future use. They must be tied High in this device.
3. Pin 6A is defined as mode pin CFG in the pinout standard. It must be tied Low in this device to select x36 configuration.
4. Pin 8B is defined as mode pin SIOM in the pinout standard. It must be tied Low in this device to select Common I/O configuration.
5. Pin 6V is defined as address pin SA for x18 devices. It is unused in this device, and must be left unconnected or driven Low.
6. Pin 8V is defined as address pin SA for B2 devices. It is used in this device.
7. Pin 9D is reserved as address pin SA for 144Mb devices. It is a true no-connect in this device.
8. Pin 7D is reserved as address pin SA for 288Mb devices. It is a true no-connect in this device.
9. Pins 5U and 9U are unused in this device. They must be left unconnected or driven Low.
10. Pins 8W and 8Y are reserved for internal use only. They must be tied Low.
11. Pins 7B and 7W are reserved for future use. They are true no-connects in this device.

Pin Description

Symbol	Description	Type
SA	**Address**—Read or Write Address is registered on ↑CK	Input
DQ[35:0]	**Write/Read Data**—Registered on ↑KD and ↑$\overline{KD}$ during Write operations. Driven by ↑CK and ↑$\overline{CK}$, and synchronized with ↑CQ and ↑$\overline{CQ}$ during Read operations. DQ[17:0]—x18 and x36. DQ[35:18]—x36 only.	I/O
QVLD[1:0]	**Read Data Valid**—Driven high one half cycle before valid Read Data.	Output
CK, $\overline{CK}$	**Primary Input Clocks**—Dual single-ended. For Address and Control input latching, internal timing control, and Read Data and Echo Clock output timing control.	Input
$\overline{KD}$[1:0], KD[1:0]	**Write Data Input Clocks**—Dual single-ended. For Write Data input latching. KD0, $\overline{KD}$0—latch Write Data (DQ[17:0] in x36, DQ[8:0] in x18). KD1, $\overline{KD}$1—latch Write Data (DQ[35:18] in x36, DQ[17:9] in x18).	Input
$\overline{CQ}$[1:0], CQ[1:0]	**Echo Clocks**—Free running source synchronous output clocks.	Output
$\overline{LD}$	**Load Enable**—Registered on↑CK. $\overline{LD}$ = 0: Loads a new address and initiates a Read or Write operation. $\overline{LD}$ = 1: Initiates a NOP operation.	Input
R/$\overline{W}$	**Read / Write Enable**—Registered on ↑CK. R/$\overline{W}$ = 0: initiates a Write operation when $\overline{LD}$ = 0. R/$\overline{W}$ = 1: initiates a Read operation when $\overline{LD}$ = 0.	Input
$\overline{AZT1}$	**Address Input Termination Pull-Up Enable**—Registered on↑CK. $\overline{AZT1}$ = 0: enables termination pull-up on Address (SA) $\overline{AZT1}$ = 1: disables termination pull-up on Address (SA)	Input
DLL	**DLL Enable**—Weakly pulled High internally. DLL = 0: disables internal DLL. DLL = 1: enables internal DLL.	Input
RST	**Reset**—Holds the device inactive and resets the device to its initial power-on state when asserted High. Weakly pulled Low internally.	Input
RLM[1:0]	**Read Latency Select 1:0**—Must be tied High or Low. RLM[1:0] = 00: reserved. RLM[1:0] = 01: selects 2.0 cycle Read Latency. RLM[1:0] = 10: selects 3.0 cycle Read Latency. RLM[1:0] = 11: reserved.	Input
ZQ	**Output Driver Impedance Control Resistor Input**—Must be connected to V_{SS} through an external resistor RQ to program output driver impedance.	Input
ZT	**Input Termination Impedance Control Resistor Input**—Must be connected to V_{SS} through an external resistor RT to program input termination impedance.	Input

Pin Description (Continued)

Symbol	Description	Type
MZT[1:0]	**Input Termination Mode Select**—Selects the termination mode used for all terminated inputs. Must be tied High or Low. MZT[1:0] = 00: disabled. MZT[1:0] = 01: RT/2 Thevenin-equivalent (pull-up = RT, pull-down = RT). MZT[1:0] = 10: RT Thevenin-equivalent (pull-up = 2*RT, pull-down = 2*RT). MZT[1:0] = 11: reserved.	Input
PZT[1:0]	**Input Termination Configuration Select**—Selects which inputs are terminated. Must be tied High or Low. PZT[1:0] = 00: Write Data only. PZT[1:0] = 01: Write Data, Input Clocks. PZT[1:0] = 10: Write Data, Address, Control. PZT[1:0] = 11: Write Data, Address, Control, Input Clocks.	Input
MVQ	**I/O Voltage Select**—Indicates what voltage is supplied to the V_{DDQ} pins. Must be tied High or Low. MVQ = 0: Configure for 1.2 V to 1.35 V nominal V_{DDQ}. MVQ = 1: Configure for 1.5 V nominal V_{DDQ}.	Input
V_{DD}	**Core Power Supply**—1.35 V nominal core supply voltage.	—
V_{DDQ}	**I/O Power Supply**—1.2 V to 1.5 V nominal I/O supply voltage. Configured via MVQ pin.	—
V_{REF}	**Input Reference Voltage**—Input buffer reference voltage.	—
V_{SS}	**Ground**	—
TCK	**JTAG Clock**	Input
TMS	**JTAG Mode Select**—Weakly pulled High internally.	Input
TDI	**JTAG Data Input**—Weakly pulled High internally.	Input
TDO	**JTAG Data Output**	Output
MCH	**Must Connect High**—May be tied to V_{DDQ} directly or via a 1kΩ resistor.	Input
MCL	**Must Connect Low**—May be tied to V_{SS} directly or via a 1kΩ resistor.	Input
NC	**No Connect**—There is no internal chip connection to these pins. They may be left unconnected, or tied High or Low.	—
NU_I	**Not Used, Input**—There is an internal chip connection to these input pins, but they are unused by the device. They are pulled Low internally. They may be left unconnected or tied Low. They should not be tied High.	Input
NU_{IO}	**Not Used Input/Output**—There is an internal chip connection to these I/O pins, but they are unused by the device. The drivers are tri-stated internally. They are pulled Low internally. They may be left unconnected or tied Low. They should not be tied High.	I/O

On-Chip Error Correction

SigmaDDR-IIIe ECCRAMs implement a single-bit error detection and correction algorithm (specifically, a Hamming Code) on each DDR data word (comprising two 9-bit data bytes) transmitted on each 9-bit data bus (i.e., transmitted on DQ[8:0], DQ[17:9], DQ[26:18], or DQ[35:27]). To accomplish this, 5 ECC parity bits (invisible to the user) are utilized per every 18 data bits (visible to the user).

The ECC algorithm neither corrects nor detects multi-bit errors. However, GSI ECCRAMs are architected in such a way that a single SER event very rarely causes a multi-bit error across any given "transmitted data unit", where a "transmitted data unit" represents the data transmitted as the result of a single read or write operation to a particular address. The extreme rarity of multi-bit errors results in the SER mentioned previously (i.e., <0.002 FITs/Mb (measured at sea level)).

Not only does the on-chip ECC significantly improve SER performance, but it also frees up the entire memory array for data storage. Very often SRAM applications allocate 1/9th of the memory array (i.e., one "error bit" per eight "data bits", in any 9-bit "data byte") for error detection (either simple parity error detection, or system-level ECC error detection and correction). Such error-bit allocation is unnecessary with ECCRAMs the entire memory array can be utilized for data storage, effectively providing 12.5% greater storage capacity compared to SRAMs of the same density not equipped with on-chip ECC.

Functional Description

Common I/O ECCRAMs, from a system architecture point of view, are attractive in read dominated or block transfer applications. Therefore, the SigmaDDR-IIIe ECCRAM interface and truth table are optimized for burst reads and writes. Common I/O ECCRAMs are unpopular in applications where alternating reads and writes are needed because bus turnaround delays can cut high speed Common I/O ECCRAM data bandwidth in half. Applications of this sort are better served by Separate I/O ECCRAMs such as the SigmaQuad-IIIe series.

Power Up Requirements

For reliability purposes, power supplies must power up simultaneously, or in the following sequence:
V_{SS}, V_{DD}, V_{DDQ}, V_{REF} and inputs.
Power supplies must power down simultaneously, or in the reverse sequence.

After power supplies power up, the following start-up sequence must be followed.

Step 1 (Recommended, but not required): Assert RST High for at least 1ms.
While RST is asserted high:
• The DLL is disabled, regardless of the state of the DLL pin.
• Read and Write operations are ignored.

Note: If possible, RST should be asserted High before input clocks (CK, $\overline{CK}$, KD, $\overline{KD}$) begin toggling, and remain asserted High until input clocks are stable and toggling within specification, in order to prevent unstable, out-of-spec input clocks from causing trouble in the SRAM.

Step 2: Begin toggling input clocks.
After input clocks begin toggling, but not necessarily within specification:
• DQ are placed in the non-Read state, and remain so until the first Read operation.
• QVLD are driven Low, and remain so until the first Read operation.
• CQ, $\overline{CQ}$ begin toggling, but not necessarily within specification.

Step 3: Wait until input clocks are stable and toggling within specification.

Step 4: De-assert RST Low (if asserted High).

Step 5: Wait at least 160K (163,840) cycles.
During this time:
• Output driver and input termination impedances are calibrated (i.e. set to the programmed values).

Note: The DLL pin may be asserted High or de-asserted Low during this time. If asserted High, DLL synchronization begins immediately after output driver and input termination impedance calibration has completed. If de-asserted Low, DLL synchronization begins after the DLL pin is asserted High (see Step 6). In either case, Step 7 must follow thereafter.

Step 6: Assert DLL pin High (if de-asserted Low).

Step 7: Wait at least 64K (65,536) cycles.
During this time:
• The DLL is enabled and synchronized properly.

After DLL synchronization has completed:
• CQ, $\overline{CQ}$ begin toggling within specification.

Step 8: Begin initiating Read and Write operations.

Reset (RST) Requirements

Although not generally recommended, RST may be asserted High at any time after completion of the initial power-up sequence described previously, to reset the SRAM control logic to its initial power-on state. However, whenever RST is subsequently de-asserted Low (as in Step 4 in the power up sequence), Steps 5~7 in the power-up sequence must be followed before Read and Write operations are initiated.

Note: Memory array content may be perturbed/corrupted when RST is asserted High.

Note: In applications that choose to utilize the RST pin, it is strongly recommended that system boards be designed with the optional ability to tie it Low.

DLL Operation

An on-chip DLL is used to align output timing with input clocks. The DLL uses the CK input clock as a source, and is enabled when all of the following conditions are met:

1. The DLL pin is asserted High, and
2. The RST pin is de-asserted Low, and
3. The input clock $t_{CKHCKH} \leq 6.0$ ns.

Once enabled, the DLL requires 64K (65,536) stable clock cycles in order to synchronize properly.

The DLL must be resynchronized (i.e. disabled and then re-enabled) whenever the input clock frequency is changed by ≥ 10%.

When the DLL is enabled, read latency is determined by the RLM mode pins, as defined in the Read Latency section. Output timing is aligned with the input clocks.

The DLL is disabled when any of the following conditions are met:

1. The DLL pin is de-asserted Low, or
2. The RST pin is asserted High, or
3. The input clock $t_{CKHCKH} \geq 30$ ns, or
4. The input clock is stopped for at least 30 ns.

When the DLL is disabled, read latency is set to 1.0 cycles regardless of the states of the RLM mode pins. Output timing is not aligned with the input clocks; rather tKQ (max) = ~6 ns.

Read Latency (RL)

Read Latency is the Read pipeline length, and directly impacts the maximum operating frequency of the device. It is user-programmable through mode pins RLM [1:0].

GS8673ET18/36BGK-675 Read Latency

Read Latency (RL)	RLM1	RLM0	Frequency
3.0 cycles	1	0	167 MHz–675 MHz
2.0 cycles	0	1	167 MHz–450 MHz

GS8673ET18/36BGK-625 Read Latency

Read Latency (RL)	RLM1	RLM0	Frequency
3.0 cycles	1	0	167 MHz–625 MHz
2.0 cycles	0	1	167 MHz–400 MHz

GS8673ET18/36BGK-550 Read Latency

Read Latency (RL)	RLM1	RLM0	Frequency
3.0 cycles	1	0	167 MHz–550 MHz
2.0 cycles	0	1	167 MHz–375 MHz

GS8673ET18/36BGK-500 Read Latency

Read Latency (RL)	RLM1	RLM0	Frequency
3.0 cycles	1	0	167 MHz–500 MHz
2.0 cycles	0	1	167 MHz–333 MHz

Truth Table

SA	$\overline{LD}$	R/$\overline{W}$	Current Operation	DQ (D)		DQ (Q)	
↑CK (t_n)	↑CK (t_n)	↑CK (t_n)	(t_n)	↑KD (t_{n+1})	↑$\overline{KD}$ ($t_{n+1½}$)	↑CK (t_m)	↑$\overline{CK}$ ($t_{m+½}$)
V	1	X	NOP	X	X	Hi-Z / *	Hi-Z / *
V	0	0	Write	D1	D2	Hi-Z / *	Hi-Z / *
V	0	1	Read	X	X	Q1	Q2

1. 1 = input High 0 = input Low; V = input valid; X = input don't care.
2. $t_m = t_{n + RL}$, where RL = Read Latency of the device.
3. D1 and D2 indicate the first and second pieces of Write Data transferred during Write operations.
4. Q1 and Q2 indicate the first and second pieces of Read Data transferred during Read operations.
5. When DQ input termination is disabled (MZT[1:0] = 00), DQ drivers are disabled (i.e. DQ pins are tri-stated) for one cycle in response to NOP and Write commands, RL cycles after the command is sampled.
6. When DQ input termination is enabled (MZT[1:0] = 01 or 10), DQ drivers are disabled for one cycle in response to NOP and Write commands, RL cycles after the command is sampled. The state of the DQ pins during that time (denoted by * in the table above) is determined by the state of the DQ input termination, as depicted in the Extended DQ Truth Tables below.

DQ Input Termination Control

A robust methodology has been developed for these devices for controlling when DQ input termination is enabled and disabled during Write-to-Read and Read-to-Write transitions. Specifically, the methodology can ensure that the DQ bus is never pulled to $V_{DDQ}/2$ by the ECCRAM and/or Memory Controller input termination during the transitions (or at any other time). Such a condition is best avoided, because if an input signal is pulled to $V_{DDQ}/2$ (i.e. to V_{REF} - the switch point of the diff-amp receiver), it could cause the receiver to enter a meta-stable state and consume more power than it normally would. This could result in the device's operating currents being higher.

The fundamental concept of the methodology is - both the ECCRAM and the Memory Controller drive the DQ bus Low (with DQ input termination disabled) at all times except:

1. When a particular device is driving the DQ bus with valid data, and
2. From shortly before to shortly after a particular device is receiving valid data on the DQ bus, during which time the receiving device enables its DQ termination.

And, during Write-to-Read and Read-to-Write transitions, each device enables and disables its DQ termination while the other device is driving DQ Low, thereby ensuring that the DQ bus is never pulled to $V_{DDQ}/2$.

Note: This methodology also reduces power consumption, since there will be no DC current through either device's DQs when both devices are driving Low.

In order for this methodology to work as described, the Memory Controller must have the ability to:

1. Place the ECCRAM into "DQ Drive Low Mode" at the appropriate times (i.e. before and after the ECCRAM drives valid Read Data), and
2. Place the ECCRAM into "DQ Termination Mode" at the appropriate times (i.e. before, during, and after the ECCRAM receives valid Write Data).

That ability is provided via the existing R/$\overline{W}$ control pin.

When the ECCRAM samples R/$\overline{W}$ High (regardless of the state of $\overline{LD}$), it disables its DQ termination, and drives the DQ bus Low except while driving valid Read Data in response to Read operations.

When the ECCRAM samples R/$\overline{W}$ Low (regardless of the state of $\overline{LD}$), it disables its DQ drivers, and enables its DQ termination.

Note that NOPs initiated with R/$\overline{W}$ High and $\overline{LD}$ High are referred to as "NOPr" operations.
Note that NOPs initiated with R/$\overline{W}$ Low and $\overline{LD}$ High are referred to as "NOPw" operations.

This extended definition of the R/$\overline{W}$ control pin allows the Memory Controller to:

- Place the ECCRAM in DQ Termination Mode, via NOPw operations, before initiating Write operations.
- Keep the ECCRAM in DQ Termination Mode, via NOPw operations, after initiating Write operations.
- Place the ECCRAM in DQ Drive Low Mode, via NOPr operations, before initiating Read operations.
- Keep the ECCRAM in DQ Drive Low Mode, via NOPr operations, after initiating Read operations.

Extended DQ Truth Table - RL = 2

$\overline{LD}$	R/$\overline{W}$	Current Operation	DQ State
↑CK (t_n)	↑CK (t_n)	(t_n)	↑CK (t_{n+2})
1	0	NOPw	Termination Enabled
0	0	Write	Termination Enabled
1	1	NOPr	Termination Disabled, Drive Low
0	1	Read	Termination Disabled, Drive Read Data

Extended DQ Truth Table - RL = 3

$\overline{LD}$	R/$\overline{W}$	Current Operation	DQ State	
↑CK (t_n)	↑CK (t_n)	(t_n)	↑CK (t_{n+2})	↑CK (t_{n+3})
1	0	NOPw	Termination Enabled	---
0	0	Write	Termination Enabled	---
1	1	NOPr	Termination Disabled, Drive Low	---
0	1	Read	Termination Disabled, Drive Low	Drive Read Data

Note:

When a Read operation is initiated in cycle "n", R/$\overline{W}$ must be "High" at ↑CK of cycle "n+1" (i.e. a Read operation must always be followed by a Read or NOPr operation). In that case, the DQ state in cycle "n+3" is "Drive Read Data", as indicated above.

NOPr/NOPw Requirements vs. Read Latency

When DQ input termination is enabled, the number of NOPw + NOPr needed during Write-to-Read transitions, and the number of NOPr + NOPw needed during Read-to-Write transitions, vary with Read Latency, as follows:

Read Latency	Write-to-Read Transition	Read-to-Write
2	0 NOPw + 2 NOPr (0 NOPw after Write is the minimum requirement) (1 NOPr before Read is the minimum requirement)	2 NOPr + 3 NOPw (1 NOPr after Read is the minimum requirement) (2 NOPw before Write is the minimum requirement)
3	0 NOPw + 1 NOPr (0 NOPw after Write is the minimum requirement) (0 NOPr before Read is the minimum requirement)	3 NOPr + 3 NOPw (2 NOPr after Read is the minimum requirement) (2 NOPw before Write is the minimum requirement)

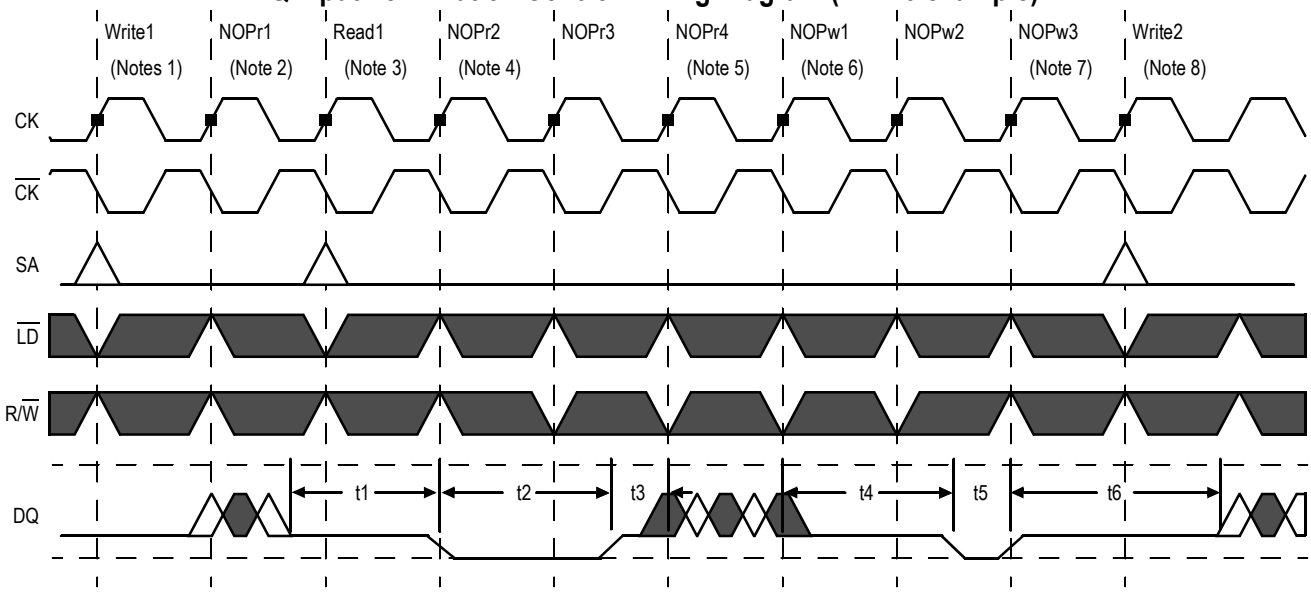
Note:

The non-parenthetical information listed in the table above depicts the NOPr / NOPw requirements during Write-to-Read and Read-to-Write transitions that should be sufficient, in most applications, to ensure that the DQ bus is never pulled to $V_{DDQ}/2$. They are not, however, absolute requirements. In some applications fewer NOPr / NOPw may be sufficient, and in other applications more NOPr / NOPw may be required.

DQ State Transition Timing Specifications

Parameter	Symbol	Min	Max	Units
CK Clock High to DQ State Transition	tCKHDQT	–0.4	0.4	ns

DQ Input Termination Control Timing Diagram (RL = 3 example)



Notes (all timing depicted at the ECCRAM pins):

1. **The Controller initiates Write1.** It stops driving DQ Low and begins driving valid Write Data ~0.75 cycles later.
   Note: At the moment Write1 is initiated, the Controller is driving DQ Low and the ECCRAM is enabling its DQ termination.
2. **The Controller initiates one NOPr (NOPr1) before Read1**. It completes driving valid Write Data and begins driving DQ Low again ~0.75 cycles later.
   In response to NOPr1, the ECCRAM disables its DQ termination and begins driving DQ Low 2 cycles later (in NOPr2), "t1" after the Controller completes driving valid Write Data and begins driving DQ Low.
   Note: t1 = "~1.25 cycles + tCKHDQT" above; if it were depicted at the Controller pins, it would *increase* by 2*tPD, where "tPD" is the trace propagation delay between Controller and ECCRAM. So, t1 must be >0 at the ECCRAM. As shown, t1 is the minimum it can be, because R/W is driven High in the cycle after Write1 above. It can be increased by initiating NOPw after Write1, but that is unnecessary to ensure the successful completion of Write1.
   Note: This one NOPr before Read1 causes the ECCRAM to drive DQ Low 2 cycles (instead of 1 cycle, without it) before valid Read Data.
3. **The Controller initiates Read1**. It stops driving DQ Low and enables its DQ termination 2.5 cycles later (in NOPr3), "t2" after the ECCRAM disables its DQ termination and begins driving DQ Low (in NOPr2), and "t3" before the ECCRAM begins driving valid Read Data (in NOPr4).
   In response to Read1, the ECCRAM stops driving DQ Low, and begins driving valid Read Data 3 cycles later (in NOPr4).
   Note: t2 = "1.5 cycles - tCKHDQT" above; if it were depicted at the Controller pins, t2 would *decrease* by 2*tPD. So, t2 must be >0 at the Controller.
   t2 can be increased by initiating more NOPr in step 2, and decreased by initiating fewer NOPr in step 2.
   Note: t3 = "0.5 cycles + tCKHDQT" above; if it were depicted at the Controller pins, t3 would *increase* by 2*tPD. So, t3 must be >0 at the ECCRAM.
   As shown, t3 is the minimum it could realistically be. It can be increased if the Controller enables its DQ termination earlier, but then t2 would decrease accordingly.
4. **The Controller initiates two NOPr (NOPr2 ~ NOPr3)**, to meet the minimum ECCRAM requirement after a Read. It continues to enable its DQ termination.
   In response to NOPr3, the ECCRAM completes driving valid Read Data and begins driving DQ Low again 2 cycles later (in NOPw1).
5. **The Controller initiates one additional NOPr (NOPr4) before initiating NOPw1**. It continues to enable its DQ termination.
   Note: This 3rd NOPr before NOPw1 causes the ECCRAM to drive DQ Low 2 cycles (instead of 1 cycle, without it) after valid Read Data.
6. **The Controller initiates two NOPw (NOPw1 ~ NOPw2)**, to meet the minimum ECCRAM requirement before a Write. It disables its DQ termination and begins driving DQ Low 1.5 cycles later (in NOPw2), "t4" after the ECCRAM stops driving valid Read data and begins driving DQ Low, and "t5" before the ECCRAM stops driving DQ Low and enables its DQ termination.
   In response to NOPw1, the ECCRAM stops driving DQ Low and enables its DQ termination 2 cycles later (in NOPw3).
   Note: t4 = "1.5 cycles - tCKHDQT" above; if it were depicted at the Controller pins, t4 would *decrease* by 2*tPD. So, t4 must be >0 at the Controller.
   t4 can be increased by initiating more NOPr in step 5, and decreased by initiating fewer NOPr in step 5.
   Note: t5 = "0.5 cycles + tCKHDQT" above; if it were depicted at the Controller pins, t5 would *increase* by 2*tPD. So, t5 must be >0 at the ECCRAM.
   As shown, t5 is the minimum it could realistically be. It can be increased if the Controller disables its DQ termination earlier, but then t4 would decrease accordingly.
7. **The Controller initiates one additional NOPw (NOPw3) before initiating Write2**. It continues to drive DQ Low.
   Note: This 3rd NOPw before Write2 causes the ECCRAM to enable its DQ termination "t6" (instead of "t6 - 1 cycle", without it) before the Controller begins driving valid Write Data.
8. **The Controller initiates Write2**. It stops driving DQ Low and begins driving valid Write Data later ~0.75 cycles later, "t6" after the ECCRAM stops driving DQ Low and enables its termination.
   Note: t6 = "~1.75 cycles - tCKHDQT" above; if it were depicted at the Controller pins, t6 would *decrease* by 2*tPD. So, t6 must be >0 at the Controller.
   t6 can be increased by initiating more NOPw in step 7, and decreased by initiating fewer NOPw in step 7.

Low Power NOP Mode

When input termination is enabled on the Address (SA) inputs, those inputs can be place in Low Power NOP (LP NOP) mode via the synchronous $\overline{AZT1}$ input. When NOP operations are initiated with $\overline{AZT1}$ High, the termination pull-ups on the SA inputs are disabled, thereby reducing the DC power associated with those inputs.

Note: When input termination is enabled on the Write Data (DQ) inputs, those inputs can also be place in a similar Low Power mode via NOPr operations. When NOPr operations are initiated, DQ termination is disabled and DQ drivers are in a "Drive Low" state, thereby reducing the DC power associated with those inputs.

LP NOP Truth Table

LD	R/$\overline{W}$	$\overline{AZT1}$	Current Operation	SA Pull-Up
↑CK (t_n)	↑CK (t_n)	↑CK (t_n)	(t_n)	↑CK (t_{n+2})
X	X	0	Any	Enabled
X	X	1	Any	Disabled

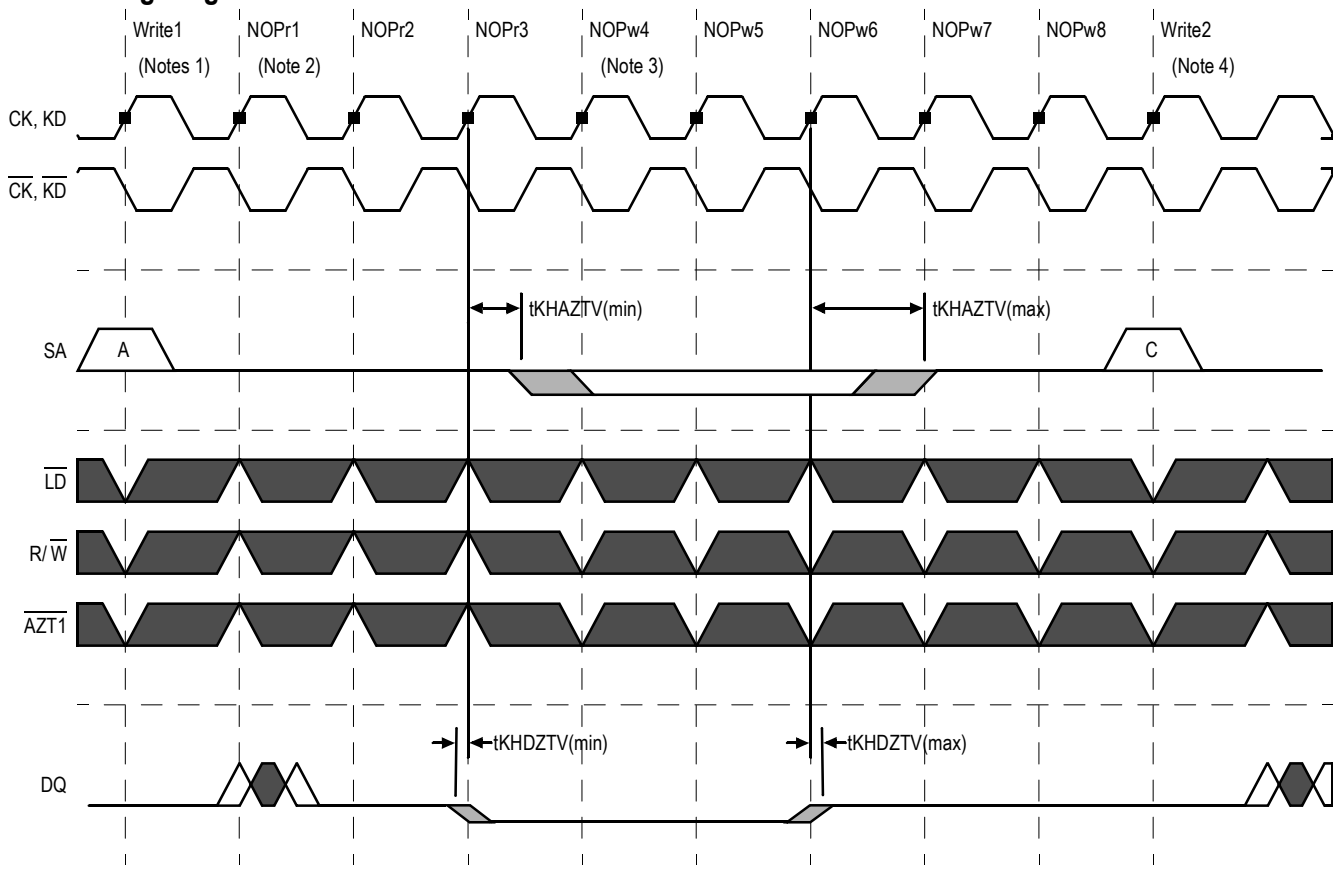
Notes:

1. 1 = input High; 0 = input Low; X = input don't care.
2. $\overline{AZT1}$ should only be driven High during NOP operations; SA input timing is not guaranteed in LP NOP Mode.
3. SA should be driven Low (or tri-stated) during LP NOP Mode, to take advantage of the power-savings feature.

LP NOP Timing Specifications

Parameter	Symbol	Min	Max	Units
CK Clock High to SA Pull-up Enable / Disable	$t_{CKHAZTV}$	0	2.0	ns

LP NOP Timing Diagram



Notes:

1. The Controller initiates Write1. The ECCRAM is enabling SA and DQ termination.
2. The Controller initiates three NOPr (NOPr1 ~ NOPr3) with AZT1 High, to cause the ECCRAM to enter LP NOP mode for three cycles.
   The ECCRAM disables SA termination pull up at ↑CK in NOP3, 2 cycles after sampling AZT1 = 1 at ↑CK in NOPr1.
   The ECCRAM disables DQ termination and begins driving DQ Low at ↑CK in NOPr3, 2 cycles after sampling R/W = 1 at ↑CK in NOPr1.
   The Controller drives SA and DQ Low during NOP1 ~ NOP8.
3. The Controller initiates five more NOPr (NOPr4 ~ NOPr8) with AZT1 Low, to allow time for the ECCRAM to exit LP NOP mode.
   The ECCRAM enables SA pull up at ↑CK in NOP6, 2 cycles after sampling AZT1 = 0 at ↑CK in NOPr4.
   The ECCRAM stops driving DQ Low and enables DQ termination at ↑CK in NOPr6, 2 cycles after sampling R/W = 0 at ↑CK in NOPr4.
4. The Controller initiates Write2. The ECCRAM is enabling SA and DQ termination.

Input Timing

Address (SA) inputs are latched with CK.
Address input timing is clock-centered; that is, CK edges must be driven such that adequate setup and hold time is provided to the address input registers, as specified by the ECCRAM.

Control ($\overline{LD}$, R/$\overline{W}$, $\overline{AZT1}$) inputs are latched with CK.
Control input timing is clock-centered; that is, CK edges must be driven such that adequate setup and hold time is provided to the control input registers, as specified by the ECCRAM.

Write Data (DQ) inputs are latched with KD[1:0] and $\overline{KD}$[1:0].

1. KD0 and $\overline{KD}$0 are used to latch DQ[17:0] in x36, and DQ[8:0] in x18.
2. KD1 and $\overline{KD}$1 are used to latch DQ[35:18] in x36, and DQ[17:9] in x18.

Write Data (DQ) input timing is clock-centered; that is, KD and $\overline{KD}$ edges must be driven such that adequate setup and hold time is provided to the data input registers, as specified by the ECCRAM.

Output Timing

The SigmaDDR-IIIe ECCRAMs feature source-synchronous output clocks, also known as echo clocks. These outputs, CQ0, $\overline{CQ0}$, CQ1, and $\overline{CQ1}$ are designed to be electrically identical to data output pins. They are designed to behave just like data output pins. They are designed to track variances demonstrated by the data outputs due to influences of temperature, voltage, process, or other factors. As a result, the specifications that describe the relationship between the CQ clock edges and the data output edges are much tighter than those that describe the relationship between the data outputs and the incoming CK clock.

Note that the CQ clock-to-data output specifications apply to specific combinations of clocks and data, as follows:

1. CQ0 and $\overline{CQ0}$ are associated with DQ[17:0] in x36, and with DQ[8:0] in x18. They are also associated with QVLD0.
2. CQ1 and $\overline{CQ1}$ are associated with DQ[35:18] in x36, and with DQ[17:9] in x18. They are also associated with QVLD1.

As can be seen, the echo clock pairs are, in each case, associated with data output pins on the nearest side of the chip. The left vs. right side groupings prevent skew across the device and pinout from degrading the data output valid window.

Output Alignment

Q1 Active	Q2 Inactive	↑CQ	↓$\overline{CQ}$	Q1 Inactive	Q2 Active	QVLD Active/Inactive	↑$\overline{CQ}$	↓CQ
Generated from ↑CK				Generated from ↑$\overline{CK}$				

Notes:

1. Output timing is aligned with input clocks.
2. Output timing is clock-aligned. That is, CQ, $\overline{CQ}$ edges are aligned with Q edges.

Output Driver Impedance Control

Programmable output drivers have been implemented on Read Data (DQ), Read Data Valid (QVLD), and Echo Clocks (CQ, $\overline{CQ}$). The output driver impedance can be programmed via the ZQ pin. When an external impedance-matching resistor (RQ) is connected between ZQ and V_{SS}, output driver impedance is set to RQ/5 nominally.

Output driver impedance is set to the programmed value within 160K cycles after input clocks are operating within specification, and RST is de-asserted Low. It is updated periodically thereafter, to compensate for temperature and voltage fluctuations in the system.

Input Termination Impedance Control

On-die input termination can be enabled on Write Data (DQ) Address (SA), Control ($\overline{LD}$, R/$\overline{W}$, $\overline{AZT1}$), and Input Clocks (CK, $\overline{CK}$, KD, $\overline{KD}$) via the MZT[1:0] and PZT[1:0] pins. The termination impedance can be programmed via the ZT pin. When an external impedance-matching resistor (RT) is connected between ZT and V_{SS}, termination impedance is set according to the table below.

Termination impedance is set to the programmed value within 160K cycles after input clocks are operating within specification, and RST is de-asserted Low. It is updated periodically thereafter, to compensate for temperature and voltage fluctuations in the system.

Note: When termination impedance is enabled on a particular input, that input should always be driven High or Low; it should never be tri-stated (i.e., in a High-Z state). If the input is tri-stated, the termination will pull the signal to V_{DDQ} / 2 (i.e., to the switch point of the diff-amp receiver), which could cause the receiver to enter a meta-stable state and consume more power than it normally would. This could result in the device's operating currents being higher.

The following table specifies the pull-up and pull-down termination impedances for each terminated input:

Pull-up and Pull-Down Termination Impedance

Terminated Inputs	PZT[1:0]	MZT[1:0]	Pull-Down Impedance	Pull-Up Impedance
CK, $\overline{CK}$, KD, $\overline{KD}$	X0	XX	disabled	disabled
	X1	01	RT	RT
		10	2 * RT	2 * RT
SA, $\overline{LD}$, R/$\overline{W}$, $\overline{AZT1}$	0X	XX	disabled	disabled
	1X	01	RT	RT
		10	2 * RT	2 * RT
DQ	XX	01	RT	RT
		10	2 * RT	2 * RT

Notes:

1. When MZT[1:0] = 00, input termination is disabled on all inputs.
2. When MZT[1:0] = 11, input termination state is not specified; it is reserved for future use.
3. During JTAG EXTEST and SAMPLE-Z instructions, input termination is disabled on all inputs.

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Core Supply Voltage	V_{DD}	–0.3 to +1.6	V
I/O Supply Voltage when MVQ = 0	V_{DDQ}	–0.3 to +1.6	V
I/O Supply Voltage when MVQ = 1	V_{DDQ}	–0.3 to +2.0	
Input Voltage when MVQ = 0	V_{IN}	–0.3 to V_{DDQ} + 0.3 (1.6 V max)	V
Input Voltage when MVQ = 1	V_{IN}	–0.3 to V_{DDQ} + 0.3 (2.0 V max)	
Maximum Junction Temperature	T_J	125	°C
Storage Temperature	T_{STG}	–55 to 125	°C

Note:

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions for an extended period of time may affect reliability of this component.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
Core Supply Voltage: -675 and -625 speed bins	V_{DD}	1.3	1.4	V
Core Supply Voltage: -550 and -500 speed bins	V_{DD}	1.25	1.4	V
I/O Supply Voltage when MVQ = 0	V_{DDQ}	1.14	1.42	V
I/O Supply Voltage when MVQ = 1	V_{DDQ}	1.4	1.6	V
Commercial Junction Temperature	T_{JC}	0	85	°C
Industrial Junction Temperature	T_{JI}	–40	100	°C

Note:

For reliability purposes, power supplies must power up simultaneously, or in the following sequence:

V_{SS}, V_{DD}, V_{DDQ}, V_{REF}, and Inputs.

Power supplies must power down simultaneously, or in the reverse sequence.

Thermal Impedance

Package	θ JA (C°/W) Airflow = 0 m/s	θ JA (C°/W) Airflow = 1 m/s	θ JA (C°/W) Airflow = 2 m/s	θ JB (C°/W)	θ JC (C°/W)
FBGA	15.5	13.1	12.1	4.4	0.2

I/O Capacitance

Parameter	Symbol	Min	Max	Units	Notes
Input Capacitance	C_{IN}	—	5.0	pF	1, 3
Output Capacitance	C_{OUT}	—	5.5	pF	2, 3

Notes:
1. $V_{IN} = V_{DDQ}/2$.
2. $V_{OUT} = V_{DDQ}/2$.
3. $T_A = 25°C$, f = 1 MHz.

Input Electrical Characteristics when MVQ = 0

Parameter	Symbol	Min	Max	Units	Notes
DC Input Reference Voltage	V_{REFdc}	0.48 * V_{DDQ}	0.52 * V_{DDQ}	V	—
DC Input High Voltage	V_{IH1dc}	V_{REF} + 0.08	V_{DDQ} + 0.15	V	4
DC Input Low Voltage	V_{IL1dc}	–0.15	V_{REF} – 0.08	V	4
DC Input High Voltage	V_{IH2dc}	0.75 * V_{DDQ}	V_{DDQ} + 0.15	V	5
DC Input Low Voltage	V_{IL2dc}	–0.15	0.25 * V_{DDQ}	V	5
AC Input Reference Voltage	V_{REFac}	0.47 * V_{DDQ}	0.53 * V_{DDQ}	V	1
AC Input High Voltage	V_{IH1ac}	V_{REF} + 0.15	V_{DDQ} + 0.25	V	2, 3, 4
AC Input Low Voltage	V_{IL1ac}	–0.25	V_{REF} – 0.15	V	2, 3, 4
AC Input High Voltage	V_{IH2ac}	V_{DDQ} – 0.2	V_{DDQ} + 0.25	V	2, 5
AC Input Low Voltage	V_{IL2ac}	– 0.25	0.2	V	2, 5

Notes:
1. V_{REFac} is equal to V_{REFdc} plus noise.
2. V_{IH} max and V_{IL} min apply for pulse widths less than one-quarter of the cycle time.
3. Input rise and fall times must be a minimum of 1 V/ns, and within 10% of each other.
4. Applies to: CK, $\overline{CK}$, KD[1.0], $\overline{KD}$[1.0], SA, DQ[35:0], $\overline{LD}$, R/$\overline{W}$, $\overline{AZT1}$.
5. Applies to: DLL, $\overline{RST}$, RLM[1:0], MZT[1:0], PZT[1:0].

Input Electrical Characteristics when MVQ = 1

Parameter	Symbol	Min	Max	Units	Notes
DC Input Reference Voltage	V_{REFdc}	0.47 * V_{DDQ}	0.53 * V_{DDQ}	V	—
DC Input High Voltage	V_{IH1dc}	V_{REF} + 0.1	V_{DDQ} + 0.15	V	4
DC Input Low Voltage	V_{IL1dc}	–0.15	V_{REF} – 0.1	V	4
DC Input High Voltage	V_{IH2dc}	0.7 * V_{DDQ}	V_{DDQ} + 0.15	V	5
DC Input Low Voltage	V_{IL2dc}	–0.15	0.3 * V_{DDQ}	V	5
AC Input Reference Voltage	V_{REFac}	0.46 * V_{DDQ}	0.54 * V_{DDQ}	V	1
AC Input High Voltage	V_{IH1ac}	V_{REF} + 0.2	V_{DDQ} + 0.25	V	2, 3, 4
AC Input Low Voltage	V_{IL1ac}	–0.25	V_{REF} – 0.2	V	2, 3, 4
AC Input High Voltage	V_{IH2ac}	V_{DDQ} – 0.2	V_{DDQ} + 0.25	V	2, 5
AC Input Low Voltage	V_{IL2ac}	–0.25	0.2	V	2, 5

Notes:

1. V_{REFac} is equal to V_{REFdc} plus noise.
2. V_{IH} max and V_{IL} min apply for pulse widths less than one-quarter of the cycle time.
3. Input rise and fall times must be a minimum of 1V/ns, and within 10% of each other.
4. Applies to: CK, $\overline{CK}$, KD[1.0], $\overline{KD}$[1.0], SA, DQ[35:0], $\overline{LD}$, R/$\overline{W}$, $\overline{AZT1}$.
5. Applies to: DLL, RST, RLM[1:0], MZT[1:0], PZT[1:0].

Input Termination Impedance when MVQ = 0

Parameter	MZT[1:0]	Symbol	Min	Max	Units	Notes
Input Termination Impedance	01	R_{IN1}	RT * 0.85	RT * 1.15	Ω	1, 2, 3
	10	R_{IN2}	2 * RT * 0.8	2 * RT * 1.2	Ω	1, 2, 3

Notes:

1. Applies to pull-up and pull-down individually.
2. Tested at $V_{IN} = V_{DDQ} * 0.2$ and $V_{DDQ} * 0.8$.
3. Parameter applies when $105 \leq RT \leq 135$.

Input Termination Impedance when MVQ = 1

Parameter	MZT[1:0]	Symbol	Min	Max	Units	Notes
Input Termination Impedance	01	R_{IN1}	RT * 0.8	RT * 1.2	Ω	1, 2, 3
	10	R_{IN2}	2 * RT * 0.75	2 * RT * 1.25	Ω	1, 2, 3

Notes:

1. Applies to pull-up and pull-down individually.
2. Tested at $V_{IN} = V_{DDQ} * 0.2$ and $V_{DDQ} * 0.8$.
3. Parameter applies when $105 \leq RT \leq 135$.

DC Output Electrical Characteristics

Parameter	Symbol	Min	Max	Units	Notes
Output High Voltage	V_{OH}	$V_{DDQ} - 0.3$	$V_{DDQ} + 0.3$	V	1, 2
Output Low Voltage	V_{OL}	– 0.3	0.3	V	1, 3

Notes:

1. RQ = 200Ω.
2. I_{OH} = – 6.0 mA.
3. I_{OL} = 6.0 mA.

Output Driver Impedance Characteristics when MVQ = 0

Parameter	Symbol	Min	Max	Units	Notes
Output Driver Impedance	R_{OUT}	(RQ/5) * 0.9	(RQ/5) * 1.1	Ω	1, 2

Notes:

1. Parameter applies when 175Ω ≤ RQ ≤ 225Ω.
2. Tested at $V_{OUT} = V_{DDQ} * 0.2$ and $V_{DDQ} * 0.8$.

Output Driver Impedance Characteristics when MVQ = 1

Parameter	Symbol	Min	Max	Units	Notes
Output Driver Impedance	R_{OUT}	(RQ/5) * 0.85	(RQ/5) * 1.15	Ω	1, 2

Notes:

1. Parameter applies when 175Ω ≤ RQ ≤ 275Ω.
2. Tested at $V_{OUT} = V_{DDQ} * 0.2$ and $V_{DDQ} * 0.8$.

Leakage Currents

Parameter	Symbol	Min	Max	Units	Notes
Input Leakage Current	I_{LI1}	–2	2	uA	1, 2, 3
	I_{LI2}	–20	2	uA	1, 4
	I_{LI3}	–2	20	uA	1, 5
	I_{LI4}	–2	—	uA	6
	I_{LI5}	—	2	uA	7
Output Leakage Current	I_{LO}	–2	2	uA	8, 9

Notes:

1. $V_{IN} = V_{SS}$ to V_{DDQ}.
2. Parameters apply to CK, $\overline{CK}$, KD, $\overline{KD}$, SA, DQ, $\overline{LD}$, R/$\overline{W}$, $\overline{AZT1}$ when input termination is disabled.
3. Parameters apply to RLM, MZT, PZT, MVQ, TCK.
4. Parameters apply to DLL, TMS, TDI (weakly pulled up).
5. Parameters apply to RST (weakly pulled down).
6. Parameters apply to MCL, NU_I. $V_{IN} = V_{SS}$ only (pins should not be tied High).
7. Parameters apply to MCH. $V_{IN} = V_{DDQ}$ only (pins should not be tied Low).
8. $V_{OUT} = V_{SS}$ to V_{DDQ}.
9. Parameters apply to DQ, CQ, $\overline{CQ}$, QVLD, TDO, NU_{IO}.

Operating Currents

P/N	RL	Operating Frequency	I_{DD} (V_{DD} = 1.25 V)		I_{DD} (V_{DD} = 1.3 V)		I_{DD} (V_{DD} = 1.35 V)		I_{DD} (V_{DD} = 1.4 V)		Units
			x18	x36	x18	x36	x18	x36	x18	x36	
GS8673ET18/36BGK-675	3	675 MHz	n/a	n/a	1560	2130	1650	2250	1750	2380	mA
	2	450 MHz			1140	1540	1210	1630	1290	1720	
GS8673ET18/36BGK-625	3	625 MHz	n/a	n/a	1470	2000	1550	2110	1650	2230	mA
	2	400 MHz			1040	1400	1110	1480	1190	1560	
GS8673ET18/36BGK-550	3	550 MHz	1260	1730	1330	1820	1410	1930	1490	2030	mA
	2	375 MHz	940	1260	990	1340	1060	1420	1130	1510	
GS8673ET18/36BGK-500	3	500 MHz	1150	1580	1220	1670	1300	1770	1380	1870	mA
	2	333 MHz	860	1150	920	1230	990	1300	1050	1380	

Notes:

1. I_{OUT} = 0 mA; V_{IN} = V_{IH} or V_{IL}.
2. Applies at 50% Reads + 50% Writes.

AC Test Conditions for 1.2 V nominal V_{DDQ} (MVQ = 0)

Parameter	Symbol	Conditions	Units
Core Supply Voltage: -675 and -625 speed bins	V_{DD}	1.3 to 1.4	V
Core Supply Voltage: -550 and -500 speed bins	V_{DD}	1.25 to 1.4	V
I/O Supply Voltage	V_{DDQ}	1.14 to 1.26	V
Input Reference Voltage	V_{REF}	0.6	V
Input High Level	V_{IH}	0.9	V
Input Low Level	V_{IL}	0.3	V
Input Rise and Fall Time	—	2.0	V/ns
Input and Output Reference Level	—	0.6	V

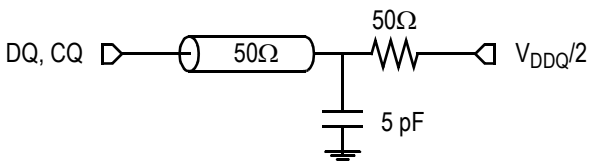
Note:
Output Load Conditions RQ = 200Ω. Refer to figure below.

AC Test Conditions for 1.5 V nominal V_{DDQ} (MVQ = 1)

Parameter	Symbol	Conditions	Units
Core Supply Voltage: -675 and -625 speed bins	V_{DD}	1.3 to 1.4	V
Core Supply Voltage: -550 and -500 speed bins	V_{DD}	1.25 to 1.4	V
I/O Supply Voltage	V_{DDQ}	1.4 to 1.6	V
Input Reference Voltage	V_{REF}	0.75	V
Input High Level	V_{IH}	1.25	V
Input Low Level	V_{IL}	0.25	V
Input Rise and Fall Time	—	2.0	V/ns
Input and Output Reference Level	—	0.75	V

Note:
Output Load Conditions RQ = 200Ω. Refer to figure below.

AC Test Output Load



AC Electrical Characteristics (independent of device speed grade)

Parameter	Symbol	Min	Max	Units	Notes
Input Clock Timing					
Clk High Pulse Width	t_{CKHCKL}	0.45	—	cycles	1
Clk Low Pulse Width	t_{CKLCKH}	0.45	—	cycles	1
Clk High to $\overline{\text{Clk}}$ High	$t_{CKH\overline{CKH}}$	0.45	0.55	cycles	2
Clk High to Write Data Clk High	t_{CKHKDH}	–0.2	0.2	ns	3
Clk Phase Jitter	$t_{K\ var}$	—	0.08	cycles	1, 4,11
DLL Lock Time	$t_{K\ lock}$	65,536	—	cycles	5
Clk Static to DLL Reset	$t_{K\ reset}$	30	—	ns	6, 11
Output Timing					
Clk High to Data Output Valid	t_{CKHQV}	—	400	ps	7
Clk High to Data Output Hold	t_{CKHQX}	–400	—	ps	7
Clk High to Data Output High-Z	t_{CKHQHZ}	—	400	ps	8
Clk High to Data Output Low-Z	t_{CKHQLZ}	–400	—	ps	8
Clk High to Echo Clock High	t_{CKHCQH}	–400	400	ps	9
Echo Clk High to $\overline{\text{Echo Clk}}$ High	$t_{CQH\overline{CQ}H}$	$t_{CKHC\overline{K}H}$ * 0.96	$t_{CKHC\overline{K}H}$ * 1.04	cycles	10, 11
Echo Clk Phase Jitter	$t_{CQ\ var}$	—	0.05	cycles	4, 11

Notes:

All parameters are measured from the mid-point of the object signal to the mid-point of the reference signal unless otherwise noted.

1. Parameters apply to CK, $\overline{\text{CK}}$, KD, $\overline{\text{KD}}$.
2. Parameters specify ↑CK → ↑$\overline{\text{CK}}$ and ↑KD → ↑$\overline{\text{KD}}$ requirements.
3. Parameters specify ↑CK → ↑KD and ↑$\overline{\text{CK}}$ → ↑$\overline{\text{KD}}$ requirements.
4. Parameter specifies the variance from clock rising edge to the next expected clock rising edge.
5. V_{DD} slew rate must be < 0.1V DC per 50 ns for DLL lock retention. DLL lock time begins once V_{DD} and input clock are stable.
6. Parameter applies to CK.
7. Parameters apply to DQ, QVLD, and are referenced to ↑CK & ↑$\overline{\text{CK}}$.
8. Parameters apply to DQ when MZT[1:0] = 00, and are referenced to CK. They are measured at ± 50 mV from steady state voltage.
9. Parameters specify ↑CK → ↑CQ and ↑$\overline{\text{CK}}$ → ↑$\overline{\text{CQ}}$ timing.
10. Parameters specify ↑CQ → ↑CQ timing.
11. Parameters are not tested. They are guaranteed by design, and verified through extensive corner-lot characterization.

AC Electrical Characteristics (variable with device speed grade)

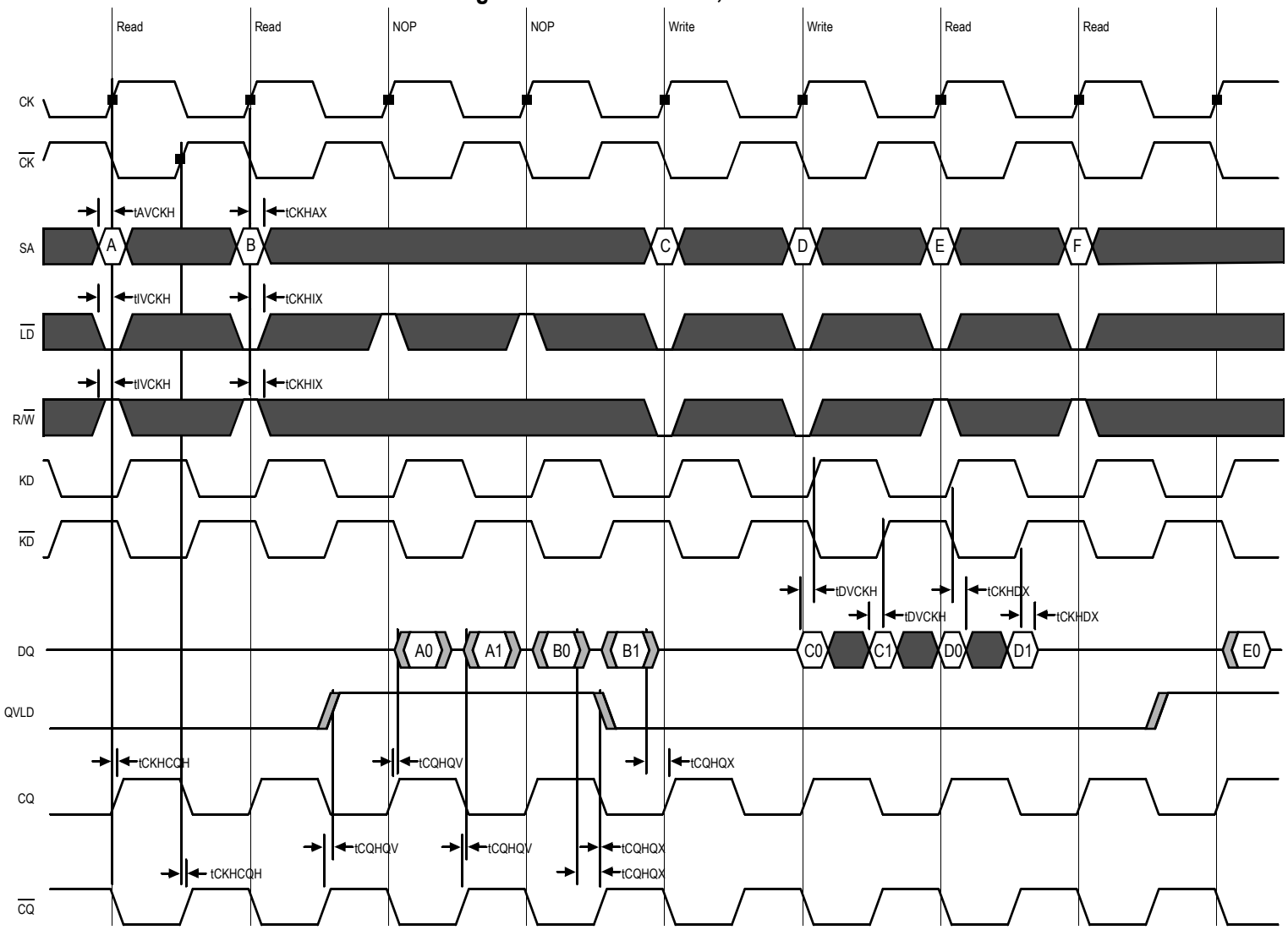
Parameter	Symbol	–675		–625		–550		–500		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Input Clock Timing											
Clk Cycle Time	t_{CKHCKH}	1.48	6.0	1.6	6.0	1.8	6.0	2.0	6.0	ns	1
		2.2	6.0	2.5	6.0	2.66	6.0	3.0	6.0	ns	2
Input Setup and Hold Timing											
Address Input Valid to Clk High	t_{AVCKH}	190	—	210	—	230	—	250	—	ps	3
Control Input Valid to Clk High	t_{IVCKH}	190	—	210	—	230	—	250	—	ps	4
Data Input Valid to Clk High	t_{DVCKH}	150	—	160	—	180	—	200	—	ps	5
Clk High to Address Input Hold	t_{CKHAX}	190	—	210	—	230	—	250	—	ps	3
Clk High to Control Input Hold	t_{CKHIX}	190	—	210	—	230	—	250	—	ps	4
Clk High to Data Input Hold	t_{CKHDX}	150	—	160	—	180	—	200	—	ps	5
Output Timing											
Echo Clk High to Data Output Valid	t_{CQHQV}	—	150	—	150	—	150	—	150	ps	6,7
Echo Clk High to Data Output Hold	t_{CQHQX}	-150	—	-150	—	-150	—	-150	—	ps	6,7

Notes:

All parameters are measured from the mid-point of the object signal to the mid-point of the reference signal.

1. Parameters apply to CK, $\overline{CK}$, KD, $\overline{KD}$ when RL = 3.
2. Parameters apply to CK, $\overline{CK}$, KD, $\overline{KD}$ when RL = 2.
3. Parameters apply to SA, and are referenced to ↑CK.
4. Parameters apply to $\overline{LD}$, R/$\overline{W}$, $\overline{AZT1}$, and are referenced to ↑CK.
5. Parameters apply to DQ, and are referenced to ↑KD & ↑$\overline{KD}$.
6. Parameters apply to DQ, QVLD and are referenced to ↑CQ & ↑$\overline{CQ}$.
7. Parameters are not tested. They are guaranteed by design, and verified through extensive corner-lot characterization.

SigmaDDR-IIIe Burst of 2, RL = 2.0



Note: The DQ = High-Z states depicted in this diagram apply when DQ input termination is disabled (MZT = 00). See page 13 for the DQ state timing diagram that applies when DQ input termination is enabled (MZT = 01 or 10).

JTAG Test Mode Description

These devices provide a JTAG Test Access Port (TAP) and Boundary Scan interface using a limited set of IEEE std. 1149.1 functions. This test mode is intended to provide a mechanism for testing the interconnect between master (processor, controller, etc.), ECCRAM, other components, and the printed circuit board. In conformance with a subset of IEEE std. 1149.1, these devices contain a TAP Controller and multiple TAP Registers. The TAP Registers consist of one Instruction Register and multiple Data Registers.

The TAP consists of the following four signals:

Pin	Pin Name	I/O	Description
TCK	Test Clock	I	Induces (clocks) TAP Controller state transitions.
TMS	Test Mode Select	I	Inputs commands to the TAP Controller. Sampled on the rising edge of TCK.
TDI	Test Data In	I	Inputs data serially to the TAP Registers. Sampled on the rising edge of TCK.
TDO	Test Data Out	O	Outputs data serially from the TAP Registers. Driven from the falling edge of TCK.

Concurrent TAP and Normal ECCRAM Operation

According to IEEE std. 1149.1, most public TAP Instructions do not disrupt normal device operation. In these devices, the only exceptions are EXTEST and SAMPLE-Z. See the Tap Registers section for more information.

Disabling the TAP

When JTAG is not used, TCK should be tied Low to prevent clocking the ECCRAM. TMS and TDI should either be tied High through a pull-up resistor or left unconnected. TDO should be left unconnected.

JTAG DC Operating Conditions when MVQ = 0

Parameter	Symbol	Min	Max	Units	Notes
JTAG Input High Voltage	V_{TIH}	0.75 * V_{DDQ}	V_{DDQ} + 0.3	V	1
JTAG Input Low Voltage	V_{TIL}	– 0.3	0.25 * V_{DDQ}	V	1
JTAG Output High Voltage	V_{TOH}	V_{DDQ} – 0.2	—	V	2, 3
JTAG Output Low Voltage	V_{TOL}	—	0.2	V	2, 4

Notes:

1. Parameters apply to TCK, TMS, and TDI during JTAG Testing.
2. Parameters apply to TDO during JTAG testing.
3. I_{TOH} = –2.0 mA.
4. I_{TOL} = 2.0 mA.

JTAG DC Operating Conditions when MVQ = 1

Parameter	Symbol	Min	Max	Units	Notes
JTAG Input High Voltage	V_{TIH}	0.7 * V_{DDQ}	V_{DDQ} + 0.3	V	1
JTAG Input Low Voltage	V_{TIL}	– 0.3	0.3 * V_{DDQ}	V	1
JTAG Output High Voltage	V_{TOH}	V_{DDQ} – 0.2	—	V	2, 3
JTAG Output Low Voltage	V_{TOL}	—	0.2	V	2, 4

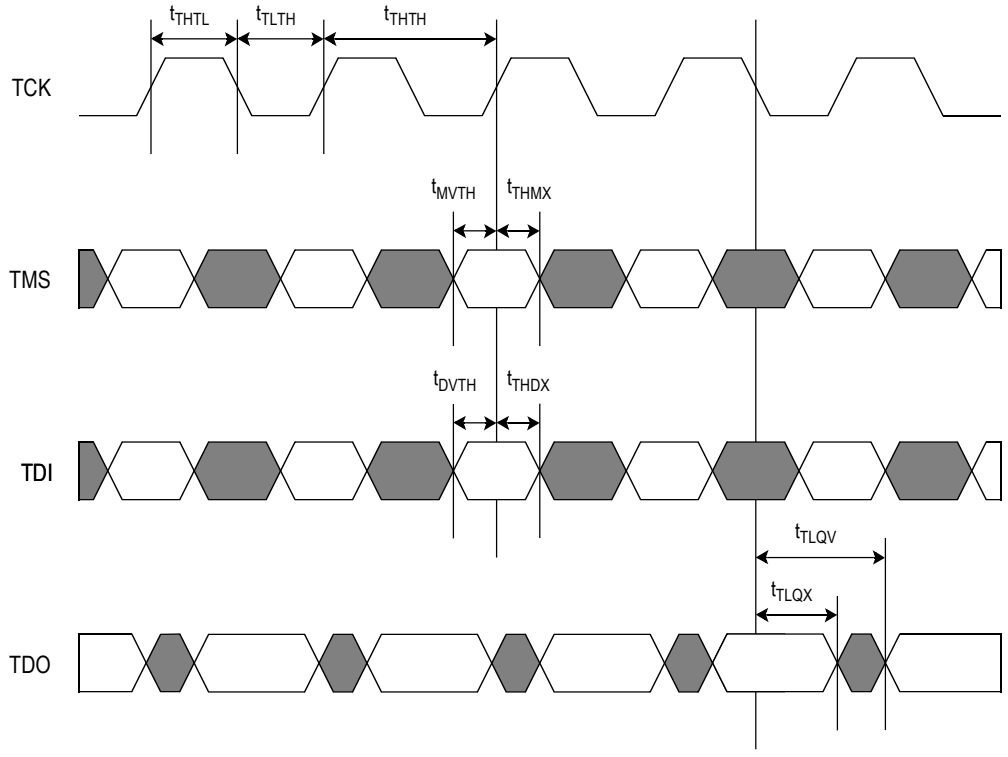
Notes:

1. Parameters apply to TCK, TMS, and TDI during JTAG Testing.
2. Parameters apply to TDO during JTAG testing.
3. I_{TOH} = –2.0 mA.
4. I_{TOL} = 2.0 mA.

JTAG AC Timing Specifications

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	t_{THTH}	50	—	ns
TCK High Pulse Width	t_{THTL}	20	—	ns
TCK Low Pulse Width	t_{TLTH}	20	—	ns
TMS Setup Time	t_{MVTH}	10	—	ns
TMS Hold Time	t_{THMX}	10	—	ns
TDI Setup Time	t_{DVTH}	10	—	ns
TDI Hold Time	t_{THDX}	10	—	ns
Capture Setup Time (Address, Control, Data, Clock)	t_{CS}	10	—	ns
Capture Hold Time (Address, Control, Data, Clock)	t_{CH}	10	—	ns
TCK Low to TDO Valid	t_{TLQV}	—	10	ns
TCK Low to TDO Hold	t_{TLQX}	0	—	ns

JTAG Timing Diagram



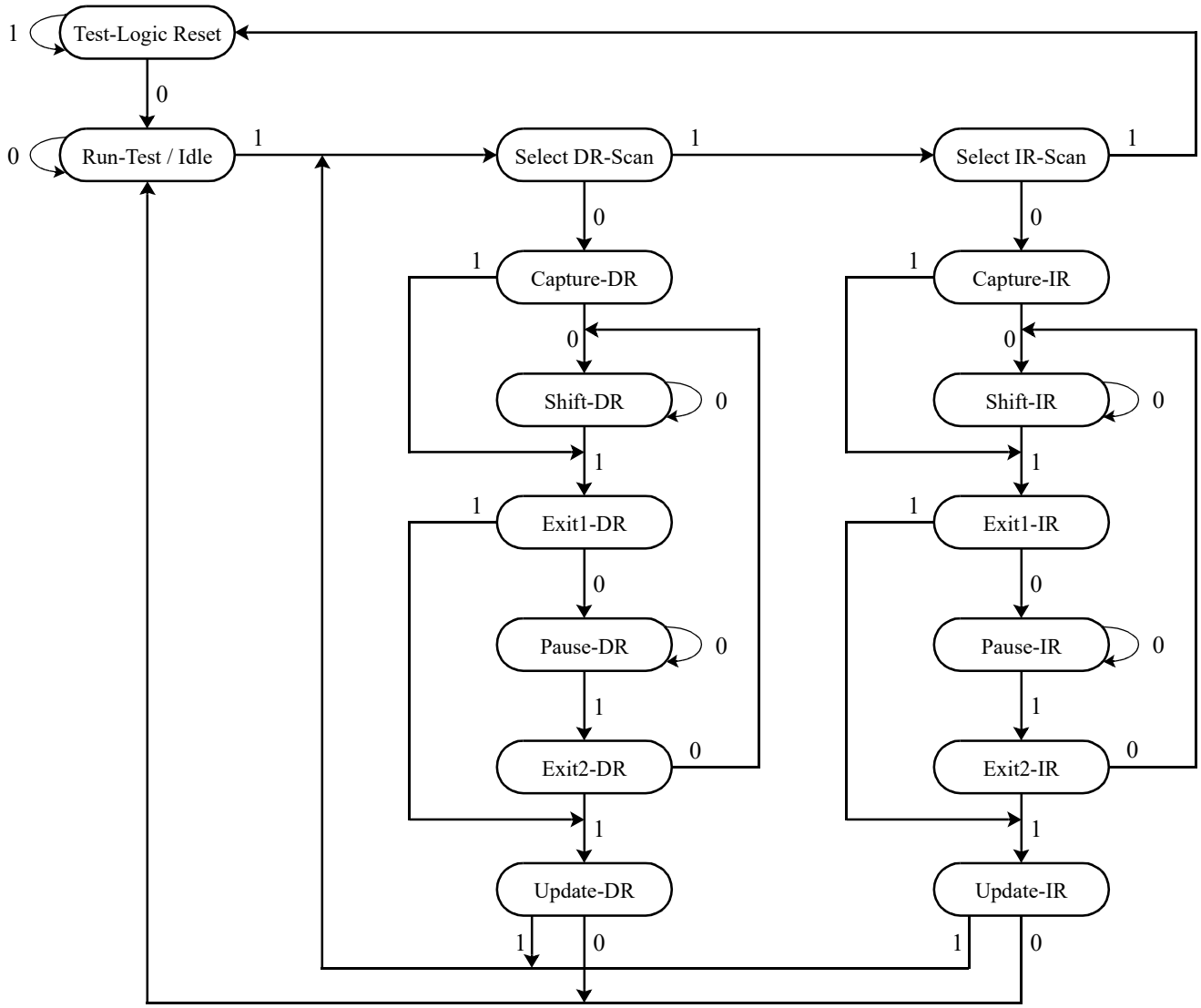
TAP Controller

The TAP Controller is a 16-state state machine that controls access to the various TAP Registers and executes the operations associated with each TAP Instruction. State transitions are controlled by TMS and occur on the rising edge of TCK.
The TAP Controller enters the Test-Logic Reset state in one of two ways:

1. At power up.
2. When a logic 1 is applied to TMS for at least 5 consecutive rising edges of TCK.

The TDI input receiver is sampled only when the TAP Controller is in either the Shift-IR state or the Shift-DR state.
The TDO output driver is enabled only when the TAP Controller is in either the Shift-IR state or the Shift-DR state.

TAP Controller State Diagram



TAP Registers

TAP Registers are serial shift registers that capture serial input data (from TDI) on the rising edge of TCK, and drive serial output data (to TDO) on the subsequent falling edge of TCK. They are divided into two groups: Instruction Registers (IR), which are manipulated via the IR states in the TAP Controller, and Data Registers (DR), which are manipulated via the DR states in the TAP Controller.

Instruction Register (IR—3 bits)

The Instruction Register stores the various TAP Instructions supported by ECCRAM. It is loaded with the IDCODE instruction (logic 001) at power-up, and when the TAP Controller is in the Test-Logic Reset and Capture-IR states. It is inserted between TDI and TDO when the TAP Controller is in the Shift-IR state, at which time it can be loaded with a new instruction. However, newly loaded instructions are not executed until the TAP Controller has reached the Update-IR state.

The Instruction Register is 3 bits wide, and is encoded as follows:

Code (2:0)	Instruction	Description
000	EXTEST	Loads the logic states of all signals composing the ECCRAM I/O ring into the Boundary Scan Register when the TAP Controller is in the Capture-DR state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the Shift-DR state. Also transfers the contents of the Boundary Scan Register associated with all output signals (DQ, QVLD, CQ, $\overline{CQ}$) directly to their corresponding output pins. However, newly loaded Boundary Scan Register contents do not appear at the output pins until the TAP Controller has reached the Update-DR state. Also disables all input termination. See the Boundary Scan Register description for more information.
001	IDCODE	Loads a predefined device- and manufacturer-specific identification code into the ID Register when the TAP Controller is in the Capture-DR state, and inserts the ID Register between TDI and TDO when the TAP Controller is in the Shift-DR state. See the ID Register description for more information.
010	SAMPLE-Z	Loads the logic states of all signals composing the ECCRAM I/O ring into the Boundary Scan Register when the TAP Controller is in the Capture-DR state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the Shift-DR state. Also disables all input termination. Also forces DQ output drivers to a High-Z state. See the Boundary Scan Register description for more information.
011	PRIVATE	Reserved for manufacturer use only.
100	SAMPLE	Loads the logic states of all signals composing the ECCRAM I/O ring into the Boundary Scan Register when the TAP Controller is in the Capture-DR state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the Shift-DR state. See the Boundary Scan Register description for more information.
101	PRIVATE	Reserved for manufacturer use only.
110	PRIVATE	Reserved for manufacturer use only.
111	BYPASS	Loads a logic 0 into the Bypass Register when the TAP Controller is in the Capture-DR state, and inserts the Bypass Register between TDI and TDO when the TAP Controller is in the Shift-DR state. See the Bypass Register description for more information.

Bypass Register (DR—1 bit)

The Bypass Register is one bit wide, and provides the minimum length serial path between TDI and TDO. It is loaded with a logic 0 when the BYPASS instruction has been loaded in the Instruction Register and the TAP Controller is in the Capture-DR state. It is inserted between TDI and TDO when the BYPASS instruction has been loaded into the Instruction Register and the TAP Controller is in the Shift-DR state.

ID Register (DR—32 bits)

The ID Register is loaded with a predetermined device- and manufacturer-specific identification code when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the Capture-DR state. It is inserted between TDI and TDO when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the Shift-DR state.

The ID Register is 32 bits wide, and is encoded as follows:

See BSDL Model (31:12)	GSI ID (11:1)	Start Bit (0)
XXXX XXXX XXXX XXXX XXXX	0001 1011 001	1

Bit 0 is the LSB of the ID Register, and Bit 31 is the MSB. When the ID Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

Boundary Scan Register (DR—127 bits)

The Boundary Scan Register is equal in length to the number of active signal connections to the ECCRAM (excluding the TAP pins) plus a number of place holder locations reserved for functional and/or density upgrades. It is loaded with the logic states of all signals composing the ECCRAM's I/O ring when the EXTEST, SAMPLE, or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the Capture-DR state. It is inserted between TDI and TDO when the EXTEST, SAMPLE, or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the Shift-DR state.

Additionally, the contents of the Boundary Scan Register associated with the ECCRAM outputs (DQ, QVLD, CQ, $\overline{CQ}$) are driven directly to the corresponding ECCRAM output pins when the EXTEST instruction is selected. However, after the EXTEST instruction has been selected, any new data loaded into Boundary Scan Register when the TAP Controller is in the Shift-DR state does not appear at the output pins until the TAP Controller has reached the Update-DR state.

The value captured in the boundary scan register for NU pins is determined by the external pin state while the NC pins are 0 regardless of the external pin state. The value captured in the internal cells is 1.

Output Driver State During EXTEST

EXTEST allows the Internal Cell (Bit 127) in the Boundary Scan Register to control the state of DQ drivers. That is, when Bit 127 = 1, DQ drivers are enabled (i.e., driving High or Low), and when Bit 127 = 0, DQ drivers are disabled (i.e., forced to High-Z state). See the Boundary Scan Register section for more information.

Input Termination State During EXTEST and SAMPLE-Z

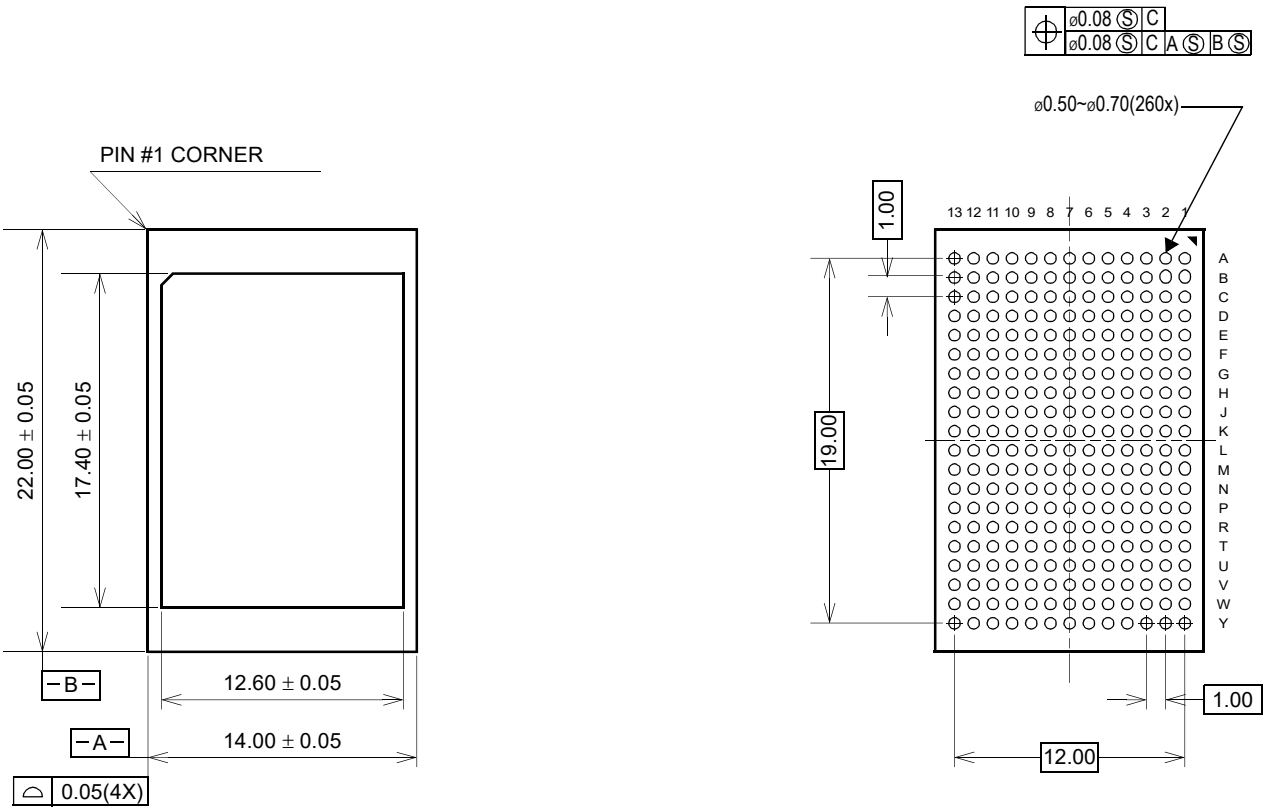
Input termination on all inputs is disabled during EXTEST and SAMPLE-Z.

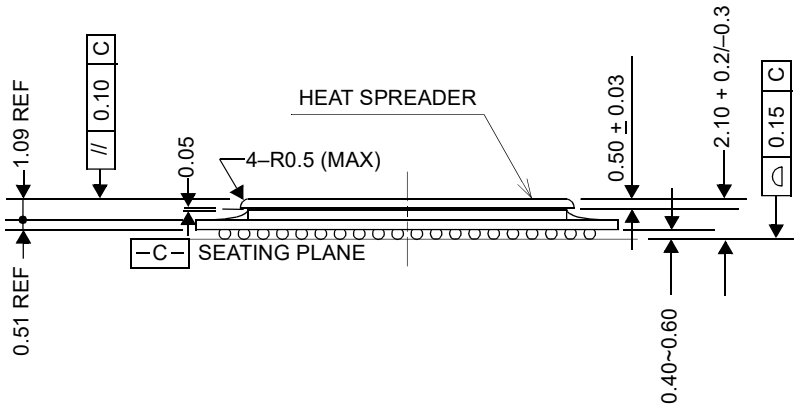
Boundary Scan Register Bit Order Assignment

The table below depicts the order in which the bits are arranged in the Boundary Scan Register. Bit 1 is the LSB and Bit 127 is the MSB. When the Boundary Scan Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

Bit	Pad	Bit	Pad	Bit	Pad	Bit	Pad	Bit	Pad
1	7L	29	11G	57	10W	85	4R	113	3C
2	7K	30	13G	58	8V	86	2R	114	2B
3	9L	31	10G	59	9U	87	3P	115	4B
4	9K	32	12G	60	8T	88	1P	116	6A
5	8J	33	11H	61	9R	89	4P	117	6B
6	7H	34	13H	62	8P	90	2P	118	6C
7	9H	35	10J	63	9N	91	3N	119	5D
8	7G	36	12J	64	8M	92	1N	120	6E
9	8G	37	13K	65	6M	93	4M	121	5F
10	9F	38	13L	66	7N	94	2M	122	6G
11	8E	39	11L	67	5N	95	3L	123	5H
12	7D	40	12M	68	7P	96	1L	124	6J
13	9D	41	10M	69	6P	97	1K	125	5K
14	8C	42	13N	70	5R	98	2J	126	5L
15	8B	43	11N	71	6T	99	4J	127	Internal
16	9B	44	12P	72	7U	100	1H		
17	7A	45	10P	73	5U	101	3H		
18	9A	46	13P	74	6V	102	2G		
19	10B	47	11P	75	6W	103	4G		
20	12B	48	12R	76	7Y	104	1G		
21	11C	49	10R	77	4W	105	3G		
22	13C	50	13T	78	2W	106	2F		
23	10D	51	11T	79	3V	107	4F		
24	12D	52	12U	80	1V	108	1E		
25	11E	53	10U	81	4U	109	3E		
26	13E	54	13V	82	2U	110	2D		
27	10F	55	11V	83	3T	111	4D		
28	12F	56	12W	84	1T	112	1C		

260-Pin BGA Package Drawing (Package GK)





Ball Pitch:	1.00	Substrate Thickness:	0.51
Ball Diameter:	0.60	Mold Thickness:	—

Ordering Information—GSI SigmaDDR-IIIe ECCRAM

Org	Part Number	Type	Package	Status	Speed (MHz)	T_A
4M x 18	GS8673ET18BGK-675	SigmaDDR-IIIe B2 ECCRAM	RoHS-compliant 260-ball BGA	Qual	675	C
4M x 18	GS8673ET18BGK-625	SigmaDDR-IIIe B2 ECCRAM	RoHS-compliant 260-ball BGA	Qual	625	C
4M x 18	GS8673ET18BGK-550	SigmaDDR-IIIe B2 ECCRAM	RoHS-compliant 260-ball BGA	Qual	550	C
4M x 18	GS8673ET18BGK-500	SigmaDDR-IIIe B2 ECCRAM	RoHS-compliant 260-ball BGA	Qual	500	C
4M x 18	GS8673ET18BGK-675I	SigmaDDR-IIIe B2 ECCRAM	RoHS-compliant 260-ball BGA	Qual	675	I
4M x 18	GS8673ET18BGK-625I	SigmaDDR-IIIe B2 ECCRAM	RoHS-compliant 260-ball BGA	Qual	625	I
4M x 18	GS8673ET18BGK-550I	SigmaDDR-IIIe B2 ECCRAM	RoHS-compliant 260-ball BGA	Qual	550	I
4M x 18	GS8673ET18BGK-500I	SigmaDDR-IIIe B2 ECCRAM	RoHS-compliant 260-ball BGA	Qual	500	I
2M x 36	GS8673ET36BGK-675	SigmaDDR-IIIe B2 ECCRAM	RoHS-compliant 260-ball BGA	Qual	675	C
2M x 36	GS8673ET36BGK-625	SigmaDDR-IIIe B2 ECCRAM	RoHS-compliant 260-ball BGA	Qual	625	C
2M x 36	GS8673ET36BGK-550	SigmaDDR-IIIe B2 ECCRAM	RoHS-compliant 260-ball BGA	Qual	550	C
2M x 36	GS8673ET36BGK-500	SigmaDDR-IIIe B2 ECCRAM	RoHS-compliant 260-ball BGA	Qual	500	C
2M x 36	GS8673ET36BGK-675I	SigmaDDR-IIIe B2 ECCRAM	RoHS-compliant 260-ball BGA	Qual	675	I
2M x 36	GS8673ET36BGK-625I	SigmaDDR-IIIe B2 ECCRAM	RoHS-compliant 260-ball BGA	Qual	625	I
2M x 36	GS8673ET36BGK-550I	SigmaDDR-IIIe B2 ECCRAM	RoHS-compliant 260-ball BGA	Qual	550	I
2M x 36	GS8673ET36BGK-500I	SigmaDDR-IIIe B2 ECCRAM	RoHS-compliant 260-ball BGA	Qual	500	I

Notes: C = Commercial Temperature Range. I = Industrial Temperature Range.

Revision History

Rev. Code	Types of Changes Format or Content	Revisions
GS8673ET1836BK_r1		• Creation of new datasheet
GS8673ET1836BK_r1_01	Content	• Changed speed bins to 625, 550, & 500 MHz. • Increased V_{DD} (min) spec from 1.25V to 1.3V for 625 MHz speed bin. • Improved t_{CKHQV} / t_{CKHQX} (and associated) specs from +/-500ps to +/-400ps. • Updated the DQ Input Termination Control section. • Updated the Low Power NOP Mode section.
GS8673ET1836BK_r1_02	Content	• Added 675 MHz speed bin. • Updated to MP status.
GS8673ET1836BK_r1_02a	Content	• Re-added t_{CKHCKH} (max) specs (previously inadvertently deleted). • Updated I_{DD} specs.
GS8673ET1836BK_r1_03	Content	• Added part numbers for lead-free RoHS-compliant BGA package.
GS8673ET1836BK_r1_04	Content	• Updated Addressing Schemes section, and moved to p.1. • Updated Absolute Maximum Ratings. • Updated Input Electrical Characteristics. • Corrected JTAG BScan Register bit order.
GS8673ET1836BK_r1_05	Content	• Updated status of lead-free RoHS-compliant BGA pkg to “Qual”.
GS8673ET1836BK_r1_06	Content	• Changed Junction Temp to Max Junction Temp in AbsMax table
GS8673ET1836BGK_r1_07	Content	• Separated non-RoHS and RoHS-compliant into two datasheets

