Rad-Tolerant SRAM

288Mb/144Mb/72Mb Burst of 2 SigmaQuad-II+™

165-Bump BGA
Military Temp

350 MHz–250 MHz
1.8 V V_{DD}
1.8 V and 1.5 V I/O

Features

- Aerospace-Level Product
- 2.0 clock Latency
- Simultaneous Read and Write SigmaQuad™ Interface
- JEDEC-standard pinout and package
- Dual Double Data Rate interface
- Byte Write controls sampled at data-in time
- Dual-Range On-Die Termination (ODT) on Data (D), Byte Write ($\overline{BW}$), and Clock (K, $\overline{K}$) inputs
- Burst of 2 Read and Write
- 1.8 V +100/–100 mV core power supply
- 1.5 V or 1.8 V HSTL Interface
- Pipelined read operation
- Fully coherent read and write pipelines
- ZQ pin for programmable output drive strength
- Data Valid Pin (QVLD) Support
- IEEE 1149.1 JTAG-compliant Boundary Scan
- 165-bump leaded BGA package

Radiation Performance

- Total Ionizing Dose (TID) > 50krads(Si)
- Destructive Single Event Latchup Immunity >42.2 MeV.cm^2/mg (100°C)

SigmaQuad™ Family Overview

The GS82582QT19/37, GS81302QT19/37, and GS8662QT19/37 are built in compliance with the SigmaQuad-II+ SRAM pinout standard for Separate I/O synchronous SRAMs. They are 301,989,888-bit (288Mb), 150,994,944-bit (144Mb), and 75,497,472-bit (72Mb) SRAMs. These SigmaQuad SRAMs comprise a family of low power, low voltage HSTL I/O Radiation-Tolerant (Rad-Tolerant) SRAMs designed to operate in Radiation environments.

Clocking and Addressing Schemes

The Rad-Tolerant SigmaQuad-II+ SRAMs are synchronous devices. They employ two input register clock inputs, K and $\overline{K}$. K and $\overline{K}$ are independent single-ended clock inputs, not differential inputs to a single differential clock input buffer.

Each internal read and write operation in a SigmaQuad-II+ B2 RAM is two times wider than the device I/O bus. An input data bus de-multiplexer is used to accumulate incoming data before it is simultaneously written to the memory array. An output data multiplexer is used to capture the data produced from a single memory array read and then route it to the appropriate output drivers as needed. Therefore, the address field of a SigmaQuad-II+ B2 RAM is always one address pin less than the advertised index depth (e.g., the 8M x 36 has an 4M addressable index).

Parameter Synopsis

	-350M	-250M
tKHKH	2.86 ns	4.0 ns
tKHQV	0.45 ns	0.45 ns

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16M x 18 SigmaQuad-II+ SRAM—Top View (288Mb)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	SA	SA	$\overline{W}$	$\overline{BW1}$	$\overline{K}$	SA	$\overline{R}$	SA	SA	CQ
B	NC	Q9	D9	SA	NC	K	$\overline{BW0}$	SA	NC	NC	Q8
C	NC	NC	D10	V_{SS}	SA	SA	SA	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	D1
P	NC	NC	Q17	SA	SA	QVLD	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	ODT	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—15 x 17 mm Body—1 mm Bump Pitch

Note:
$\overline{BW0}$ controls writes to D0:D8. $\overline{BW1}$ controls writes to D9:D17.

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8M x 36 SigmaQuad-II+ SRAM—Top View (288Mb)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	SA	SA	$\overline{W}$	$\overline{BW2}$	$\overline{K}$	$\overline{BW1}$	$\overline{R}$	SA	SA	CQ
B	Q27	Q18	D18	SA	$\overline{BW3}$	K	$\overline{BW0}$	SA	D17	Q17	Q8
C	D27	Q28	D19	V_{SS}	SA	SA	SA	V_{SS}	D16	Q7	D8
D	D28	D20	Q19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q16	D15	D7
E	Q29	D29	Q20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	Q15	D6	Q6
F	Q30	Q21	D21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D14	Q14	Q5
G	D30	D22	Q22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q13	D13	D5
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	D31	Q31	D23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D12	Q4	D4
K	Q32	D32	Q23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q12	D3	Q3
L	Q33	Q24	D24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	D11	Q11	Q2
M	D33	Q34	D25	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D10	Q1	D2
N	D34	D26	Q25	V_{SS}	SA	SA	SA	V_{SS}	Q10	D9	D1
P	Q35	D35	Q26	SA	SA	QVLD	SA	SA	Q9	D0	Q0
R	TDO	TCK	SA	SA	SA	ODT	SA	SA	SA	TMS	TDI

11 x 15 Bump CCGA—21 x 25 mm Body—1.27 mm Bump Pitch (TBR)

Note:
$\overline{BW0}$ controls writes to D0:D8; $\overline{BW1}$ controls writes to D9:D17; $\overline{BW2}$ controls writes to D18:D26; $\overline{BW3}$ controls writes to D27:D35

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8M x 18 SigmaQuad-II+ SRAM—Top View (144Mb)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	SA	SA	$\overline{W}$	$\overline{BW1}$	$\overline{K}$	MCL (288Mb)	$\overline{R}$	SA	SA	CQ
B	NC	Q9	D9	SA	NC	K	$\overline{BW0}$	SA	NC	NC	Q8
C	NC	NC	D10	V_{SS}	SA	SA	SA	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	D1
P	NC	NC	Q17	SA	SA	QVLD	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	ODT	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—15 x 17 mm Body—1 mm Bump Pitch

Note:
$\overline{BW0}$ controls writes to D0:D8. $\overline{BW1}$ controls writes to D9:D17.

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4M x 36 SigmaQuad-II+ SRAM—Top View (144Mb)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	MCL (288Mb)	SA	$\overline{W}$	$\overline{BW2}$	$\overline{K}$	$\overline{BW1}$	$\overline{R}$	SA	SA	CQ
B	Q27	Q18	D18	SA	$\overline{BW3}$	K	$\overline{BW0}$	SA	D17	Q17	Q8
C	D27	Q28	D19	V_{SS}	SA	SA	SA	V_{SS}	D16	Q7	D8
D	D28	D20	Q19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q16	D15	D7
E	Q29	D29	Q20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	Q15	D6	Q6
F	Q30	Q21	D21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D14	Q14	Q5
G	D30	D22	Q22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q13	D13	D5
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	D31	Q31	D23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D12	Q4	D4
K	Q32	D32	Q23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q12	D3	Q3
L	Q33	Q24	D24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	D11	Q11	Q2
M	D33	Q34	D25	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D10	Q1	D2
N	D34	D26	Q25	V_{SS}	SA	SA	SA	V_{SS}	Q10	D9	D1
P	Q35	D35	Q26	SA	SA	QVLD	SA	SA	Q9	D0	Q0
R	TDO	TCK	SA	SA	SA	ODT	SA	SA	SA	TMS	TDI

11 x 15 Bump CCGA—21 x 25 mm Body—1.27 mm Bump Pitch (TBR)

Note:
$\overline{BW0}$ controls writes to D0:D8; $\overline{BW1}$ controls writes to D9:D17; $\overline{BW2}$ controls writes to D18:D26; $\overline{BW3}$ controls writes to D27:D35

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4M x 18 SigmaQuad-II+ SRAM—Top View (72Mb)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	MCL (144Mb)	SA	$\overline{W}$	$\overline{BW1}$	$\overline{K}$	MCL (288Mb)	$\overline{R}$	SA	SA	CQ
B	NC	Q9	D9	SA	NC	K	$\overline{BW0}$	SA	NC	NC	Q8
C	NC	NC	D10	V_{SS}	SA	SA	SA	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	D1
P	NC	NC	Q17	SA	SA	QVLD	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	ODT	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—15 x 17 mm Body—1 mm Bump Pitch

Note:
$\overline{BW0}$ controls writes to D0:D8. $\overline{BW1}$ controls writes to D9:D17.

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2M x 36 SigmaQuad-II+ SRAM—Top View (72Mb)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	MCL (288Mb)	SA	$\overline{W}$	$\overline{BW2}$	$\overline{K}$	$\overline{BW1}$	$\overline{R}$	SA	MCL (144Mb)	CQ
B	Q27	Q18	D18	SA	$\overline{BW3}$	K	$\overline{BW0}$	SA	D17	Q17	Q8
C	D27	Q28	D19	V_{SS}	SA	SA	SA	V_{SS}	D16	Q7	D8
D	D28	D20	Q19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q16	D15	D7
E	Q29	D29	Q20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	Q15	D6	Q6
F	Q30	Q21	D21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D14	Q14	Q5
G	D30	D22	Q22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q13	D13	D5
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	D31	Q31	D23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D12	Q4	D4
K	Q32	D32	Q23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q12	D3	Q3
L	Q33	Q24	D24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	D11	Q11	Q2
M	D33	Q34	D25	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D10	Q1	D2
N	D34	D26	Q25	V_{SS}	SA	SA	SA	V_{SS}	Q10	D9	D1
P	Q35	D35	Q26	SA	SA	QVLD	SA	SA	Q9	D0	Q0
R	TDO	TCK	SA	SA	SA	ODT	SA	SA	SA	TMS	TDI

11 x 15 Bump CCGA—21 x 25 mm Body—1.27 mm Bump Pitch (TBR)

Note:
$\overline{BW0}$ controls writes to D0:D8; $\overline{BW1}$ controls writes to D9:D17; $\overline{BW2}$ controls writes to D18:D26; $\overline{BW3}$ controls writes to D27:D35

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Pin Description Table

Symbol	Description	Type	Comments
SA	Synchronous Address Inputs	Input	—
$\overline{R}$	Synchronous Read	Input	Active Low
$\overline{W}$	Synchronous Write	Input	Active Low
$\overline{BW0}$–$\overline{BW3}$	Synchronous Byte Writes	Input	Active Low
K	Input Clock	Input	Active High
$\overline{K}$	Input Clock	Input	Active Low
TMS	Test Mode Select	Input	—
TDI	Test Data Input	Input	—
TCK	Test Clock Input	Input	—
TDO	Test Data Output	Output	—
V_{REF}	HSTL Input Reference Voltage	Input	—
ZQ	Output Impedance Matching Input	Input	—
Qn	Synchronous Data Outputs	Output	—
Dn	Synchronous Data Inputs	Input	—
$\overline{Doff}$	Disable DLL when low	Input	Active Low
CQ	Output Echo Clock	Output	—
$\overline{CQ}$	Output Echo Clock	Output	—
V_{DD}	Power Supply	Supply	1.8 V Nominal
V_{DDQ}	Isolated Output Buffer Supply	Supply	1.8 V or 1.5 V Nominal
V_{SS}	Power Supply: Ground	Supply	—
QVLD	Q Valid Output	Output	—
ODT	On-Die Termination	Input	Low = Low Impedance Range High/Float = High Impedance Range
NC	No Connect	—	—
MCL	Must Connect Low	Input	May be tied to V_{SS} directly or via a 1kΩ resistor

Notes:
1. NC = Not Connected to die or any other pin
2. When ZQ pin is directly connected to V_{DDQ}, output impedance is set to minimum value and it cannot be connected to ground or left unconnected.
3. K and $\overline{K}$ cannot be set to V_{REF} voltage.

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Background

Separate I/O SRAMs, from a system architecture point of view, are attractive in applications where alternating reads and writes are needed. Therefore, the SigmaQuad-II+ SRAM interface and truth table are optimized for alternating reads and writes. Separate I/O SRAMs are unpopular in applications where multiple reads or multiple writes are needed because burst read or write transfers from Separate I/O SRAMs can cut the RAM's bandwidth in half.

SigmaQuad-II B2 SRAM DDR Read

The read port samples the status of the Address Input and $\overline{R}$ pins at each rising edge of K. A low on the Read Enable-bar pin, $\overline{R}$, begins a read cycle. Clocking in a high on the Read Enable-bar pin, $\overline{R}$, begins a read port deselect cycle.

SigmaQuad-II B2 SRAM DDR Write

The write port samples the status of the $\overline{W}$ pin at each rising edge of K and the Address Input pins on the following rising edge of $\overline{K}$. A low on the Write Enable-bar pin, $\overline{W}$, begins a write cycle. The first of the data-in pairs associated with the write command is clocked in with the same rising edge of K used to capture the write command. The second of the two data in transfers is captured on the rising edge of $\overline{K}$ along with the write address. Clocking in a high on $\overline{W}$ causes a write port deselect cycle.

Special Functions

Byte Write Control

Byte Write Enable pins are sampled at the same time that Data In is sampled. A High on the Byte Write Enable pin associated with a particular byte (e.g., $\overline{BW0}$ controls D0–D8 inputs) will inhibit the storage of that particular byte, leaving whatever data may be stored at the current address at that byte location undisturbed. Any or all of the Byte Write Enable pins may be driven High or Low during the data in sample times in a write sequence.

Each write enable command and write address loaded into the RAM provides the base address for a 2beat data transfer. The x18 version of the RAM, for example, may write 36 bits in association with each address loaded. Any 9-bit byte may be masked in any write sequence.

Example x18 RAM Write Sequence using Byte Write Enables

Data In Sample Time	$\overline{BW0}$	$\overline{BW1}$	D0–D8	D9–D17
Beat 1	0	1	Data In	Don't Care
Beat 2	1	0	Don't Care	Data In

Resulting Write Operation

Byte 1 D0–D8	Byte 2 D9–D17	Byte 3 D0–D8	Byte 4 D9–D17
Written	Unchanged	Unchanged	Written
Beat 1		Beat 2	

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FLXDrive-II Output Driver Impedance Control

HSTL I/O SigmaQuad-II+ SRAMs are supplied with programmable impedance output drivers. The ZQ pin must be connected to V_{SS} via an external resistor, RQ, to allow the SRAM to monitor and adjust its output driver impedance. The value of RQ must be 5X the value of the desired RAM output impedance. The allowable range of RQ to guarantee impedance matching continuously is between 175Ω and 350Ω. Periodic readjustment of the output driver impedance is necessary as the impedance is affected by drifts in supply voltage and temperature. The SRAM's output impedance circuitry compensates for drifts in supply voltage and temperature. A clock cycle counter periodically triggers an impedance evaluation, resets and counts again. Each impedance evaluation may move the output driver impedance level one step at a time towards the optimum level. The output driver is implemented with discrete binary weighted impedance steps.

Input Termination Impedance Control

These SigmaQuad-II+ SRAMs are supplied with programmable input termination on Data (D), Byte Write ($\overline{BW}$), and Clock (K,$\overline{K}$) input receivers. The input termination is always enabled, and the impedance is programmed via the same RQ resistor (connected between the ZQ pin and V_{SS}) used to program output driver impedance, in conjuction with the ODT pin (6R). When the ODT pin is tied Low, input termination is "strong" (i.e., low impedance), and is nominally equal to RQ*0.3 Thevenin-equivalent when RQ is between 175Ω and 350Ω. When the ODT pin is tied High (or left floating—the pin has a small pull-up resistor), input termination is "weak" (i.e., high impedance), and is nominally equal to RQ*0.6 Thevenin-equivalent when RQ is between 175Ω and 250Ω. Periodic readjustment of the termination impedance occurs to compensate for drifts in supply voltage and temperature, in the same manner as for driver impedance (see above).

Note:
D, $\overline{BW}$, K, $\overline{K}$ inputs should always be driven High or Low; they should never be tri-stated (i.e., in a High-Z state). If the inputs are tri-stated, the input termination will pull the signal to $V_{DDQ}/2$ (i.e., to the switch point of the diff-amp receiver), which could cause the receiver to enter a meta-stable state, resulting in the receiver consuming more power than it normally would. This could result in the device's operating currents being higher.

Power-Up Initialization

After power-up, stable input clocks must be applied to the device for 20 µs prior to issuing read and write commands. See the t_{KInit} timing parameter in the **AC Electrical Characteristics** section.

Note:
The t_{KInit} requirement is independent of the tLock requirement, which specifies how many cycles of stable input clocks (2048) must be applied after the $\overline{Doff}$ pin has been driven High in order to ensure that the DLL locks properly (and the DLL must lock properly before issuing read and write commands). However, t_{KInit} is greater than t_{KLock}, even at the slowest permitted cycle time of 8.4 ns (2048*8.4 ns = 17.2 µs). Consequently, the 20 µs associated with t_{KInit} is sufficient to cover the t_{KLock} requirement at power-up if the $\overline{Doff}$ pin is driven High prior to the start of the 20 µs period.

Also, t_{KInit} only needs to be met once, immediately after power-up, whereas t_{KLock} must be met any time the DLL is disabled/reset (whether by toggling $\overline{Doff}$ Low or by stopping K clocks for > 30 ns).

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Separate I/O SigmaQuad-II B2 SigmaQuad-II SRAM Read Truth Table

A	$\overline{R}$	Output Next State	Q	Q
K ↑ (t_n)	K ↑ (t_n)	K ↑ (t_n)	K ↑ (t_{n+2})	$\overline{K}$ ↑ ($t_{n+2½}$)
X	1	Deselect	Hi-Z	Hi-Z
V	0	Read	Q0	Q1

Notes:
1. X = Don't Care, 1 = High, 0 = Low, V = Valid.
2. $\overline{R}$ is evaluated on the rising edge of K.
3. Q0 and Q1 are the first and second data output transfers in a read.

Separate I/O SigmaQuad-II B2 SigmaQuad-II SRAM Write Truth Table

A	$\overline{W}$	$\overline{BWn}$	$\overline{BWn}$	Input Next State	D	D
$\overline{K}$ ↑ ($t_{n+½}$)	K ↑ (t_n)	K ↑ (t_n)	$\overline{K}$ ↑ ($t_{n+½}$)	K ↑, $\overline{K}$ ↑ (t_n), ($t_{n+½}$)	K ↑ (t_n)	$\overline{K}$ ↑ ($t_{n+½}$)
V	0	0	0	Write Byte Dx0, Write Byte Dx1	D0	D1
V	0	0	1	Write Byte Dx0, Write Abort Byte Dx1	D0	X
V	0	1	0	Write Abort Byte Dx0, Write Byte Dx1	X	D1
X	0	1	1	Write Abort Byte Dx0, Write Abort Byte Dx1	X	X
X	1	X	X	Deselect	X	X

Notes:
1. X = Don't Care, H = High, L = Low, V = Valid.
2. $\overline{W}$ is evaluated on the rising edge of K.
3. D0 and D1 are the first and second data input transfers in a write.
4. BWn represents any of the Byte Write Enable inputs (BW0, BW1, etc.).

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x36 Byte Write Enable ($\overline{BWn}$) Truth Table

$\overline{BW0}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	D0–D8	D9–D17	D18–D26	D27–D35
1	1	1	1	Don't Care	Don't Care	Don't Care	Don't Care
0	1	1	1	Data In	Don't Care	Don't Care	Don't Care
1	0	1	1	Don't Care	Data In	Don't Care	Don't Care
0	0	1	1	Data In	Data In	Don't Care	Don't Care
1	1	0	1	Don't Care	Don't Care	Data In	Don't Care
0	1	0	1	Data In	Don't Care	Data In	Don't Care
1	0	0	1	Don't Care	Data In	Data In	Don't Care
0	0	0	1	Data In	Data In	Data In	Don't Care
1	1	1	0	Don't Care	Don't Care	Don't Care	Data In
0	1	1	0	Data In	Don't Care	Don't Care	Data In
1	0	1	0	Don't Care	Data In	Don't Care	Data In
0	0	1	0	Data In	Data In	Don't Care	Data In
1	1	0	0	Don't Care	Don't Care	Data In	Data In
0	1	0	0	Data In	Don't Care	Data In	Data In
1	0	0	0	Don't Care	Data In	Data In	Data In
0	0	0	0	Data In	Data In	Data In	Data In

x18 Byte Write Enable ($\overline{BWn}$) Truth Table

$\overline{BW0}$	$\overline{BW1}$	D0–D8	D9–D17
1	1	Don't Care	Don't Care
0	1	Data In	Don't Care
1	0	Don't Care	Data In
0	0	Data In	Data In

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Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 2.9	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to V_{DD}	V
V_{REF}	Voltage in V_{REF} Pins	–0.5 to V_{DDQ}	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.5 (≤ 2.9 V max.)	V
V_{IN}	Input Voltage (Address, Control, Data, Clock)	–0.5 to V_{DDQ} +0.5 (≤ 2.9 V max.)	V
V_{TIN}	Input Voltage (TCK, TMS, TDI)	–0.5 to V_{DDQ} +0.5 (≤ 2.9 V max.)	V
I_{IN}	Input Current on Any Pin	+/–100	mA dc
I_{OUT}	Output Current on Any I/O Pin	+/–100	mA dc
T_J	Maximum Junction Temperature	125	°C
T_{STG}	Storage Temperature	–65 to 150 (TBR)	°C

Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions, for an extended period of time, may affect reliability of this component.

Recommended Operating Conditions

Power Supplies

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	1.7	1.8	1.9	V
I/O Supply Voltage	V_{DDQ}	1.4	—	V_{DD}	V
Reference Voltage	V_{REF}	$V_{DDQ}/2$ – 0.05	—	$V_{DDQ}/2$ + 0.05	V

Note:
The power supplies need to be powered up simultaneously or in the following sequence: V_{DD}, V_{DDQ}, V_{REF}, followed by signal inputs. The power down sequence must be the reverse. V_{DDQ} must not exceed V_{DD}. For more information, read **AN1021 SigmaQuad and SigmaDDR Power-Up.**

Operating Temperature

Parameter	Symbol	Min.	Typ.	Max.	Unit
Junction Temperature	T_J	–55	25	125	°C

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Thermal Impedance

Package	Test PCB Substrate	θ JA (C°/W) Airflow = 0 m/s	θ JA (C°/W) Airflow = 1 m/s	θ JA (C°/W) Airflow = 2 m/s	θ JB (C°/W)	θ JC (C°/W)
165 BGA	4-layer	16.10	13.69	12.73	6.54	2.08

Notes:
1. Thermal Impedance data is based on a number of of samples from multiple lots and should be viewed as a typical number.
2. Please refer to JEDEC standard JESD51-6.
3. The characteristics of the test fixture PCB influence reported thermal characteristics of the device. Be advised that a good thermal path to the PCB can result in cooling or heating of the RAM depending on PCB temperature.

HSTL I/O DC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
Input Reference Voltage	V_{REF}	V_{DDQ} /2 – 0.05	V_{DDQ} /2 + 0.05	V	—
Input High Voltage	V_{IH1}	V_{REF} + 0.1	V_{DDQ} + 0.3	V	1
Input Low Voltage	V_{IL1}	–0.3	V_{REF} – 0.1	V	1
Input High Voltage	V_{IH2}	0.7 * V_{DDQ}	V_{DDQ} + 0.3	V	2,3
Input Low Voltage	V_{IL2}	–0.3	0.3 * V_{DDQ}	V	2,3

Notes:
1. Parameters apply to K, $\overline{K}$, SA, D, $\overline{R}$, $\overline{W}$, $\overline{BW}$ during normal operation and JTAG boundary scan testing.
2. Parameters apply to Doff, ODT during normal operation and JTAG boundary scan testing.
3. Parameters apply to ZQ during JTAG boundary scan testing only.

HSTL I/O AC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
Input Reference Voltage	V_{REF}	V_{DDQ} /2 – 0.08	V_{DDQ} /2 + 0.08	V	—
Input High Voltage	V_{IH1}	V_{REF} + 0.2	V_{DDQ} + 0.5	V	1,2,3
Input Low Voltage	V_{IL1}	–0.5	V_{REF} – 0.2	V	1,2,3
Input High Voltage	V_{IH2}	V_{DDQ} – 0.2	V_{DDQ} + 0.5	V	4,5
Input Low Voltage	V_{IL2}	–0.5	0.2	V	4,5

Notes:
1. $V_{IH(MAX)}$ and $V_{IL(MIN)}$ apply for pulse widths less than one-quarter of the cycle time.
2. Input rise and fall times must be a minimum of 1 V/ns, and within 10% of each other.
3. Parameters apply to K, $\overline{K}$, SA, D, $\overline{R}$, $\overline{W}$, $\overline{BW}$ during normal operation and JTAG boundary scan testing.
4. Parameters apply to Doff, ODT during normal operation and JTAG boundary scan testing.
5. Parameters apply to ZQ during JTAG boundary scan testing only.

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Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 1.8 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	6	7	pF
Clock Capacitance	C_{CLK}	V_{IN} = 0 V	5	6	pF

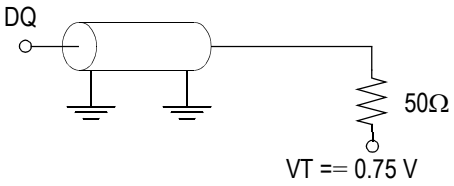
Note:
This parameter is sample tested.

AC Test Conditions

Parameter	Conditions
Input high level	1.25
Input low level	0.25 V
Max. input slew rate	2 V/ns
Input reference level	0.75
Output reference level	V_{DDQ}/2

Note:
Test conditions as specified with output loading as shown unless otherwise noted.

AC Test Load Diagram



RQ = 250 Ω (HSTL I/O)
V_{REF} = 0.75 V

Input and Output Leakage Characteristics

Parameter	Symbol	Test Conditions	Min.	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–2 uA	2 uA
$\overline{\text{Doff}}$	$I_{IL\overline{DOFF}}$	V_{IN} = 0 to V_{DD}	–2 uA	100 uA
ODT	$I_{IL\ ODT}$	V_{IN} = 0 to V_{DD}	–100 uA	2 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DDQ}	–2 uA	2 uA

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Programmable Impedance HSTL Output Driver DC Electrical Characteristics

Parameter	Symbol	Min.	Max.	Units	Notes
Output High Voltage	V_{OH1}	$V_{DDQ}/2 - 0.15$	$V_{DDQ}/2 + 0.15$	V	1, 3
Output Low Voltage	V_{OL1}	$V_{DDQ}/2 - 0.15$	$V_{DDQ}/2 + 0.15$	V	2, 3
Output High Voltage	V_{OH2}	$V_{DDQ} - 0.2$	V_{DDQ}	V	4, 5
Output Low Voltage	V_{OL2}	Vss	0.2	V	4, 6

Notes:

1. $I_{OH} = (V_{DDQ}/2) / (RQ/5)$ +/– 20% @ $V_{OH} = V_{DDQ}/2$ (for: $175\Omega \leq RQ \leq 350\Omega$).
2. $I_{OL} = (V_{DDQ}/2) / (RQ/5)$ +/– 20% @ $V_{OL} = V_{DDQ}/2$ (for: $175\Omega \leq RQ \leq 350\Omega$).
3. Parameter tested with $RQ = 250\Omega$ and $V_{DDQ} = 1.5$ V
4. $0\Omega \leq RQ \leq \infty\Omega$
5. $I_{OH} = -1.0$ mA
6. $I_{OL} = 1.0$ mA

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Operating Currents

Parameter	Symbol	Test Conditions	-350M	-250M	Unit	Notes
			–55 to 125°C	–55 to 125°C		
Operating Current (x36): DDR	I_{DD}	V_{DD} = Max, I_{OUT} = 0 mA Cycle Time ≥ t_{KHKH} Min	1430	1140	mA	2, 3
Operating Current (x18): DDR	I_{DD}	V_{DD} = Max, I_{OUT} = 0 mA Cycle Time ≥ t_{KHKH} Min	1280	1030	mA	2, 3
Standby Current (NOP): DDR	I_{SB1}	Device deselected, I_{OUT} = 0 mA, f = Max, All Inputs ≤ 0.2 V or ≥ V_{DD} – 0.2 V	590	520	mA	2, 4

Notes:

1. Power measured with output pins floating.
2. Minimum cycle, I_{OUT} = 0 mA
3. Operating current is calculated with 50% read cycles and 50% write cycles.
4. Standby Current is only after all pending read and write burst operations are completed.

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AC Electrical Characteristics

Parameter	Symbol	-350M		-250M		Units	Notes
		Min	Max	Min	Max		
Clock							
K, $\overline{K}$ Clock Cycle Time	t_{KHKH}	2.86	8.4	4.0	8.4	ns	
tK Variable	t_{KVar}	—	0.2	—	0.2	ns	4
K, $\overline{K}$ Clock High Pulse Width	t_{KHKL}	0.4	—	0.4	—	cycle	
K, $\overline{K}$ Clock Low Pulse Width	t_{KLKH}	0.4	—	0.4	—	cycle	
K to $\overline{K}$ High	$t_{KH\overline{K}H}$	1.22	—	1.8	—	ns	
$\overline{K}$ to K High	$t_{\overline{K}HKH}$	1.22	—	1.8	—	ns	
DLL Lock Time	t_{KLock}	2048	—	2048	—	cycle	5
K Static to DLL reset	t_{KReset}	30	—	30	—	ns	
K, $\overline{K}$ Clock Initialization	t_{KInit}	20	—	20	—	µs	6
Output Times							
K, $\overline{K}$ Clock High to Data Output Valid	t_{KHQV}	—	0.45	—	0.45	ns	
K, $\overline{K}$ Clock High to Data Output Hold	t_{KHQX}	–0.45	—	–0.45	—	ns	
K, $\overline{K}$ Clock High to Echo Clock Valid	t_{KHCQV}	—	0.45	—	0.45	ns	
K, $\overline{K}$ Clock High to Echo Clock Hold	t_{KHCQX}	–0.45	—	–0.45	—	ns	
CQ, $\overline{CQ}$ High Output Valid	t_{CQHQV}	—	0.23	—	0.30	ns	
CQ, $\overline{CQ}$ High Output Hold	t_{CQHQX}	–0.23	—	–0.30	—	ns	
CQ, $\overline{CQ}$ High to QVLD	t_{QVLD}	–0.23	0.23	–0.30	0.30	ns	
CQ Phase Distortion	$t_{CQH\overline{CQ}H}$ $t_{\overline{CQ}HCQH}$	1.19	—	1.67	—	ns	
K Clock High to Data Output High-Z	t_{KHQZ}	—	0.45	—	0.45	ns	
K Clock High to Data Output Low-Z	t_{KHQX1}	–0.45	—	–0.45	—	ns	
Setup Times							
Address Input Setup Time	t_{AVKH}	0.3	—	0.35	—	ns	1
Control Input Setup Time ($\overline{R}$, $\overline{W}$)	t_{IVKH}	0.3	—	0.35	—	ns	2
Control Input Setup Time ($\overline{BWX}$) ($\overline{BWX}$)	t_{IVKH}	0.3	—	0.35	—	ns	3
Data Input Setup Time	t_{DVKH}	0.3	—	0.35	—	ns	
Hold Times							
Address Input Hold Time	t_{KHAX}	0.3	—	0.35	—	ns	1
Control Input Hold Time ($\overline{R}$, $\overline{W}$)	t_{KHIX}	0.3	—	0.35	—	ns	2
Control Input Hold Time ($\overline{BWX}$) ($\overline{BWX}$)	t_{KHIX}	0.3	—	0.35	—	ns	3
Data Input Hold Time	t_{KHDX}	0.3	—	0.35	—	ns	

Notes:

1. All Address inputs must meet the specified setup and hold times for all latching clock edges.
2. Control signals are $\overline{R}$, $\overline{W}$
3. Control signals are $\overline{BW0}$, $\overline{BW1}$, and ($\overline{NW0}$, $\overline{NW1}$ for x8) and ($\overline{BW2}$, $\overline{BW3}$ for x36).
4. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
5. V_{DD} slew rate must be less than 0.1 V DC per 50 ns for DLL lock retention. DLL lock time begins once V_{DD} and input clock are stable.
6. After device power-up, 20µs of stable input clocks (as specified by t_{KInit}) must be supplied before reads and writes are issued.

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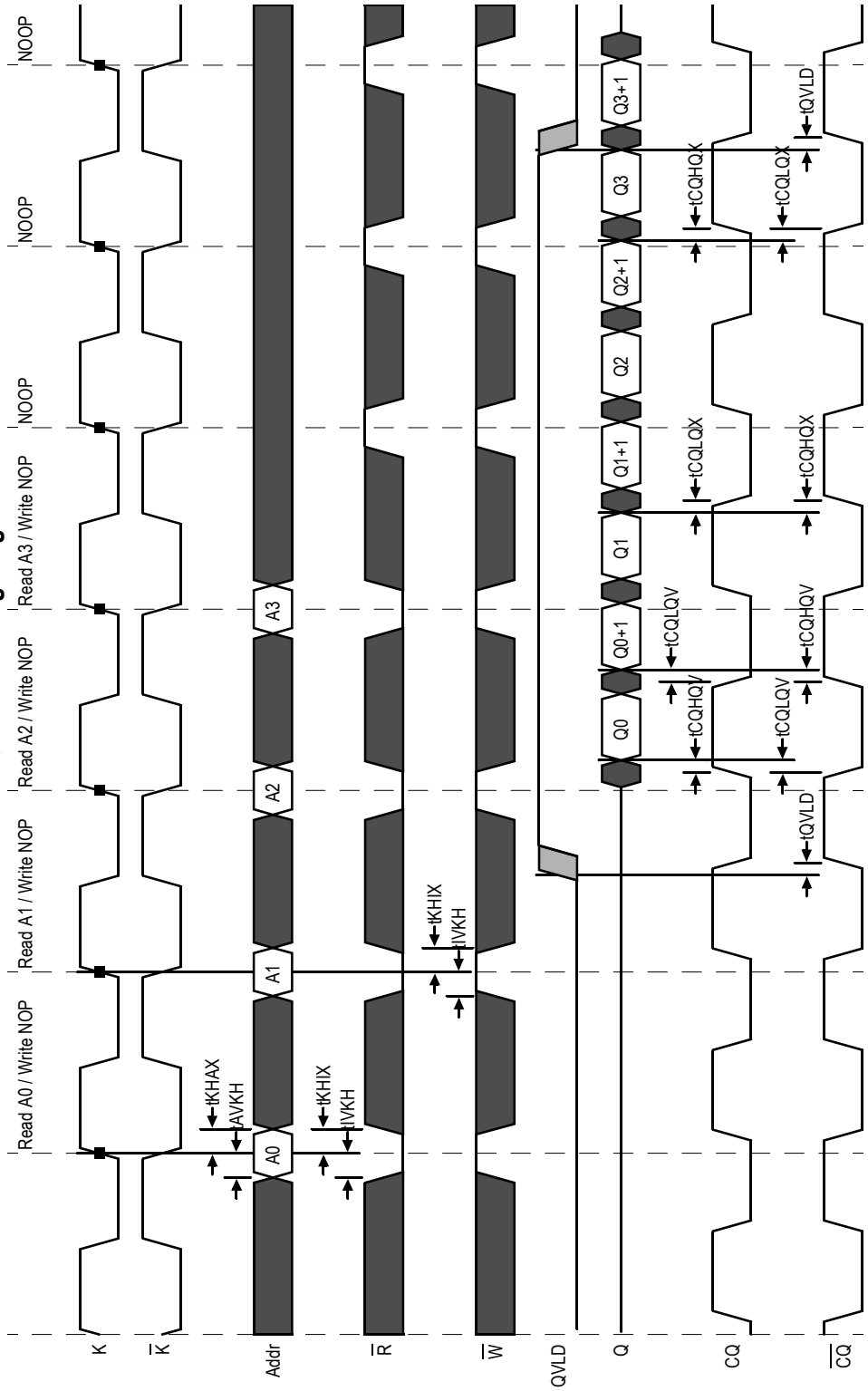
Read NOP CQ-Based Timing Diagram



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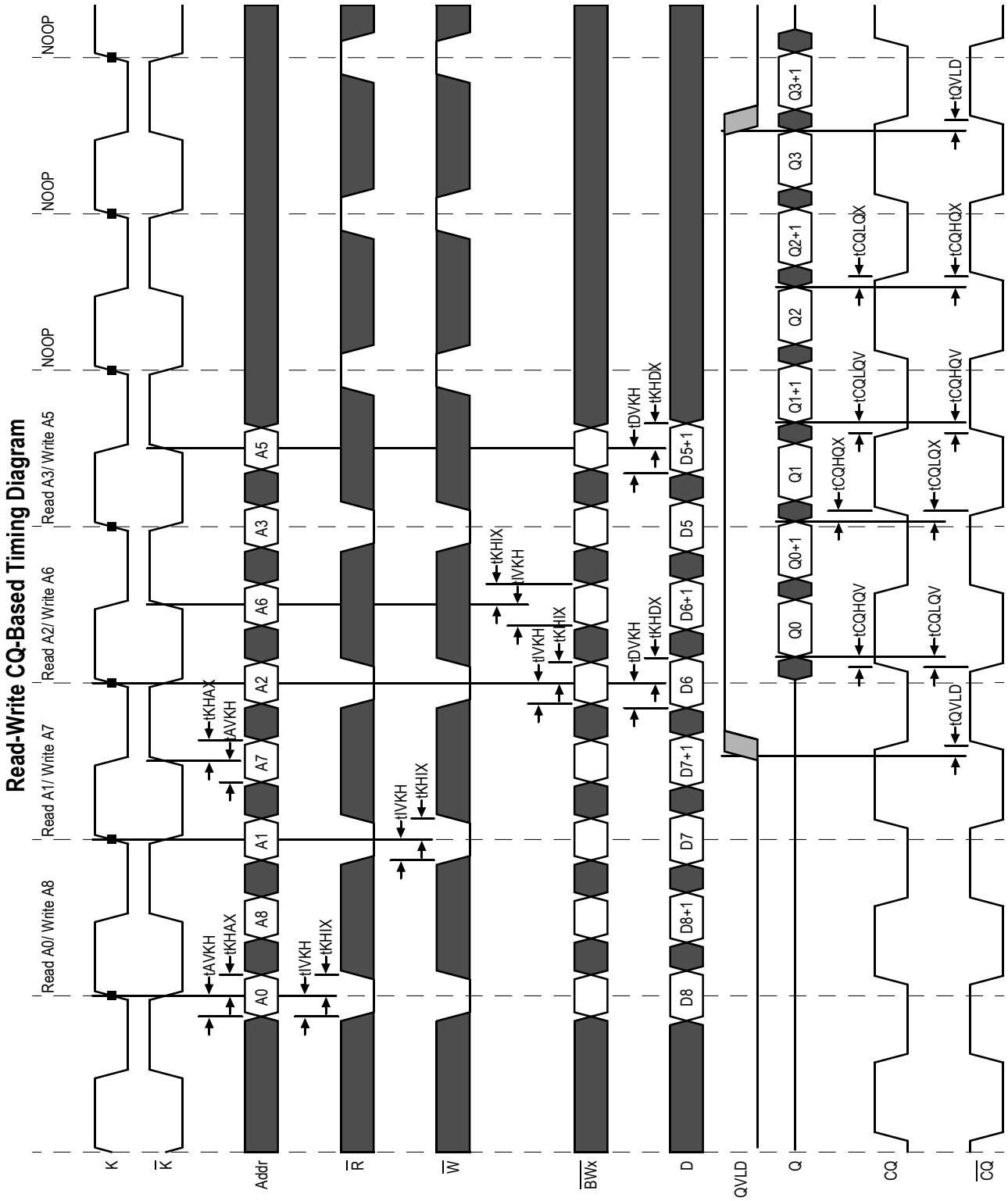
Read-Write CQ-Based Timing Diagram



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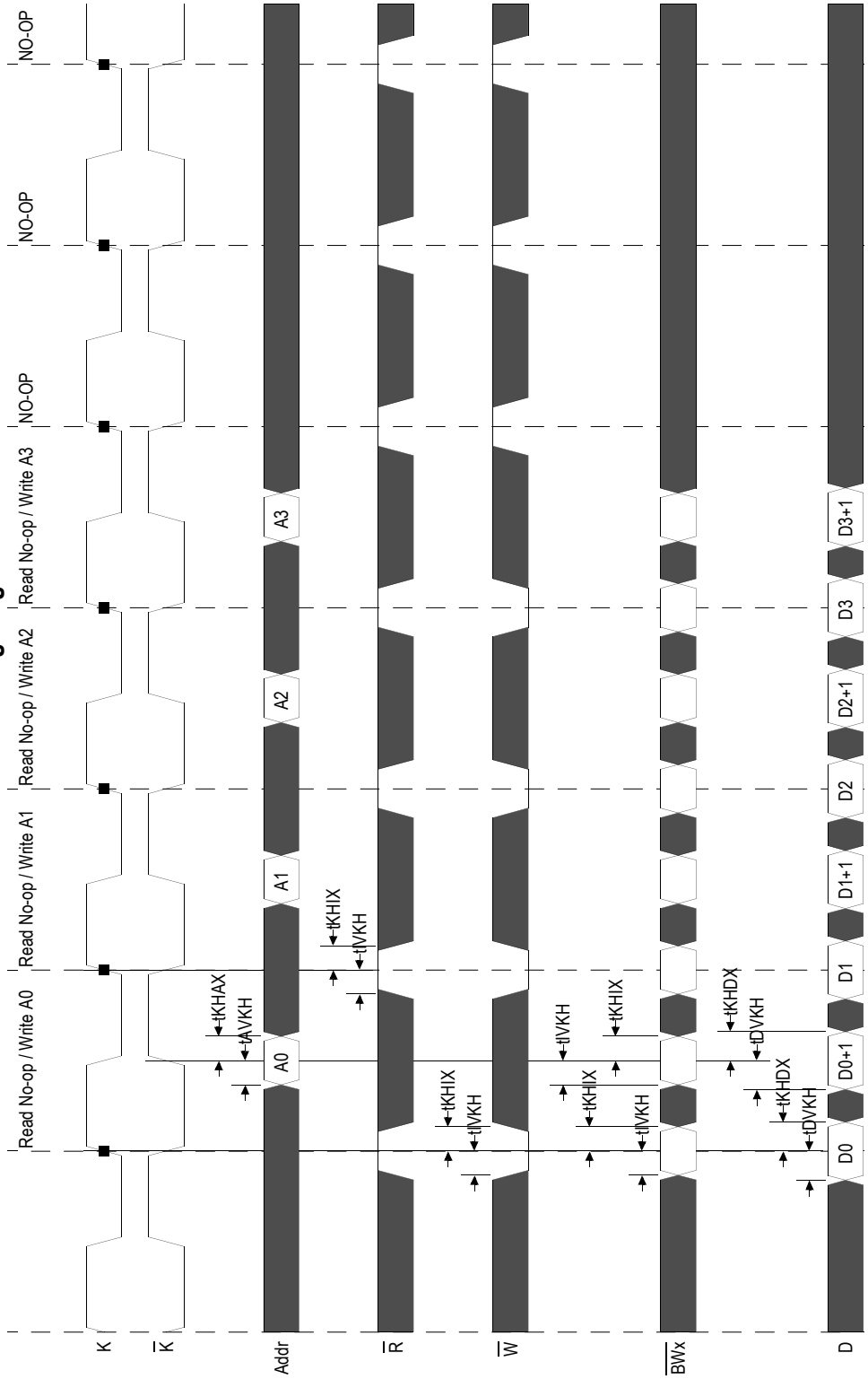
Write NOP Timing Diagram



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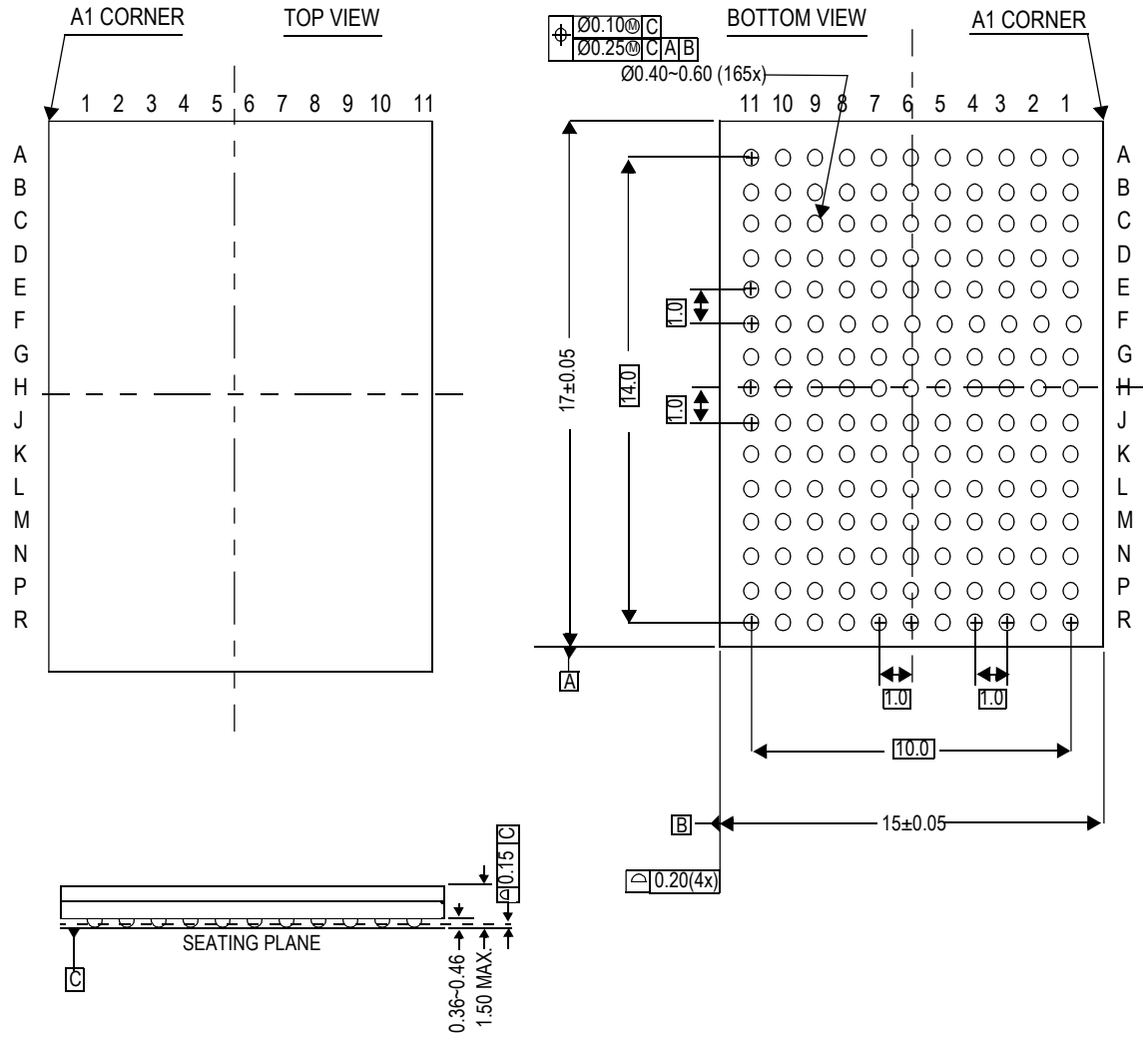
Package Dimensions—165-Bump FPBGA (Package E)



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Ordering Information—GSI SigmaQuad-II+ SRAM

Org	Part Number	Type	Package	Speed (MHz)	T_J*
288Mb					
8M x 36	GS82582QT37RE-350M	288Mb SigmaQuad-II+ B2 SRAM	165-bump BGA	350	M
8M x 36	GS82582QT37RE-250M	288Mb SigmaQuad-II+ B2 SRAM	165-bump BGA	250	M
16M x 18	GS82582QT19RE-350M	288Mb SigmaQuad-II+ B2 SRAM	165-bump BGA	350	M
16M x 18	GS82582QT19RE-250M	288Mb SigmaQuad-II+ B2 SRAM	165-bump BGA	250	M
144Mb					
4M x 36	GS81302QT37RE-350M	144Mb SigmaQuad-II+ B2 SRAM	165-bump BGA	350	M
4M x 36	GS81302QT37RE-250M	144Mb SigmaQuad-II+ B2 SRAM	165-bump BGA	250	M
8M x 18	GS81302QT19RE-350M	144Mb SigmaQuad-II+ B2 SRAM	165-bump BGA	350	M
8M x 18	GS81302QT19RE-250M	144Mb SigmaQuad-II+ B2 SRAM	165-bump BGA	250	M
72Mb					
2M x 36	GS8662QT37RE-350M	72Mb SigmaQuad-II+ B2 SRAM	165-bump BGA	350	M
2M x 36	GS8662QT37RE-250M	72Mb SigmaQuad-II+ B2 SRAM	165-bump BGA	250	M
4M x 18	GS8662QT19RE-350M	72Mb SigmaQuad-II+ B2 SRAM	165-bump BGA	350	M
4M x 18	GS8662QT19RE-250M	72Mb SigmaQuad-II+ B2 SRAM	165-bump BGA	250	M

Note:
M = Military Temperature Range.

SigmaQuad-II+ SRAM Revision History

File Name	Format/Content	Description of changes
82582QT37RE-RADTOL_r1		Creation of datasheet (Rev1.00a: Corrected typo in ordering information table) (Rev1.00b: Changed unused address pins from NC to MCL)
82582QT37RE-RADTOL_r1_01	Content	Removed Preliminary banner due to MP status

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