

4M x 36 SigmaDDR-II SRAM—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	\overline{CQ}	SA	SA	R/\overline{W}	$\overline{BW2}$	\overline{K}	$\overline{BW1}$	\overline{LD}	SA	SA	CQ
B	NC	DQ27	DQ18	SA	$\overline{BW3}$	K	$\overline{BW0}$	SA	NC/SA (288Mb)	NC	DQ8
C	NC	NC	DQ28	V_{SS}	SA	SA0	SA1	V_{SS}	NC	DQ17	DQ7
D	NC	DQ29	DQ19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	DQ16
E	NC	NC	DQ20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQ15	DQ6
F	NC	DQ30	DQ21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	DQ31	DQ22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ14
H	\overline{Doff}	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	DQ32	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ13	DQ4
K	NC	NC	DQ23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ12	DQ3
L	NC	DQ33	DQ24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	DQ34	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ11	DQ1
N	NC	DQ35	DQ25	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	DQ10
P	NC	NC	DQ26	SA	SA	C	SA	SA	NC	DQ9	DQ0
R	TDO	TCK	SA	SA	SA	\overline{C}	SA	SA	SA	TMS	TDI

 11 x 15 Bump BGA—13 x 15 mm² Body—1 mm Bump Pitch

Notes:

1. $\overline{BW0}$ controls writes to DQ0:DQ8; $\overline{BW1}$ controls writes to DQ9:DQ17; $\overline{BW2}$ controls writes to DQ18:DQ26; $\overline{BW3}$ controls writes to DQ27:DQ35.
2. B9 is the expansion address.

8M x 18 SigmaDDR-II SRAM—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{\text{CQ}}$	SA	SA	$\text{R}/\overline{\text{W}}$	$\overline{\text{BW1}}$	$\overline{\text{K}}$	SA	$\overline{\text{LD}}$	SA	SA	CQ
B	NC	DQ9	NC	SA	NC/SA (288Mb)	K	$\overline{\text{BW0}}$	SA	NC	NC	DQ8
C	NC	NC	NC	V_{SS}	SA	SA0	SA1	V_{SS}	NC	DQ7	NC
D	NC	NC	DQ10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ6
F	NC	DQ12	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	NC	DQ13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{\text{Doff}}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ4	NC
K	NC	NC	DQ14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ3
L	NC	DQ15	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ1	NC
N	NC	NC	DQ16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
P	NC	NC	DQ17	SA	SA	C	SA	SA	NC	NC	DQ0
R	TDO	TCK	SA	SA	SA	$\overline{\text{C}}$	SA	SA	SA	TMS	TDI

 11 x 15 Bump BGA—13 x 15 mm² Body—1 mm Bump Pitch

Notes:

1. $\overline{\text{BW0}}$ controls writes to DQ0:DQ8; $\overline{\text{BW1}}$ controls writes to DQ9:DQ17.
2. B5 is the expansion address.

16M x 9 SigmaDDR-II SRAM—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{\text{CQ}}$	SA	SA	$\text{R}/\overline{\text{W}}$	NC	$\overline{\text{K}}$	SA	$\overline{\text{LD}}$	SA	SA	CQ
B	NC	NC	NC	SA	NC/SA (288Mb)	K	$\overline{\text{BW0}}$	SA	NC	NC	DQ4
C	NC	NC	NC	V_{SS}	SA	NC	SA	V_{SS}	NC	NC	NC
D	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ5	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ3
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	NC	DQ6	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{\text{Doff}}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ2	NC
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	DQ7	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ1
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
N	NC	NC	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
P	NC	NC	DQ8	SA	SA	C	SA	SA	NC	NC	DQ0
R	TDO	TCK	SA	SA	SA	$\overline{\text{C}}$	SA	SA	SA	TMS	TDI

 11 x 15 Bump BGA—13 x 15 mm² Body—1 mm Bump Pitch

Notes:

1. Unlike the x36 and x18 versions of this device, the x8 and x9 versions do not give the user access to A0 and A1. SA0 and SA1 are set to 0 at the beginning of each access.
2. BW0 controls writes to DQ0;DQ8.
3. B5 is the expansion address.

16M x 8 SigmaDDR-II SRAM—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{\text{CQ}}$	SA	SA	$\text{R}/\overline{\text{W}}$	$\overline{\text{NW1}}$	$\overline{\text{K}}$	SA	$\overline{\text{LD}}$	SA	SA	CQ
B	NC	NC	NC	SA	NC/SA (288Mb)	K	$\overline{\text{NW0}}$	SA	NC	NC	DQ3
C	NC	NC	NC	V_{SS}	SA	NC	SA	V_{SS}	NC	NC	NC
D	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ4	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	NC	DQ5	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{\text{Doff}}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ1	NC
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	DQ6	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ0
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
N	NC	NC	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
P	NC	NC	DQ7	SA	SA	C	SA	SA	NC	NC	NC
R	TDO	TCK	SA	SA	SA	$\overline{\text{C}}$	SA	SA	SA	TMS	TDI

 11 x 15 Bump BGA—13 x 15 mm² Body—1 mm Bump Pitch

Notes:

1. Unlike the x36 and x18 versions of this device, the x8 and x9 versions do not give the user access to A0 and A1. SA0 and SA1 are set to 0 at the beginning of each access.
2. $\overline{\text{NW0}}$ controls writes to DQ0:DQ3; $\overline{\text{NW1}}$ controls writes to DQ4:DQ7.
3. B5 is the expansion address.

Pin Description Table

Symbol	Description	Type	Comments
SA	Synchronous Address Inputs	Input	—
$R\bar{W}$	Synchronous Read/Write	Input	Read: Active High Write: Active Low
$\bar{B}W0\text{--}\bar{B}W3$	Synchronous Byte Writes	Input	Active Low x18/x36 only
$\bar{N}W0\text{--}\bar{N}W1$	Nybble Write Control Pin	Input	Active Low x8 only
$\bar{L}D$	Synchronous Load Pin	Input	Active Low
K	Input Clock	Input	Active High
\bar{K}	Input Clock	Input	Active Low
C	Output Clock	Input	Active High
\bar{C}	Output Clock	Input	Active Low
TMS	Test Mode Select	Input	—
TDI	Test Data Input	Input	—
TCK	Test Clock Input	Input	—
TDO	Test Data Output	Output	—
V_{REF}	HSTL Input Reference Voltage	Input	—
ZQ	Output Impedance Matching Input	Input	—
MCL	Must Connect Low	—	—
DQ	Data I/O	Input/Output	Three State
$\bar{D}off$	Disable DLL when low	Input	Active Low
CQ	Output Echo Clock	Output	—
$\bar{C}Q$	Output Echo Clock	Output	—
V_{DD}	Power Supply	Supply	1.8 V Nominal
V_{DDQ}	Isolated Output Buffer Supply	Supply	1.8 V or 1.5 V Nominal
V_{SS}	Power Supply: Ground	Supply	—
NC	No Connect	—	—

Notes:

1. NC = Not Connected to die or any other pin
2. C, \bar{C} , K, \bar{K} cannot be set to V_{REF} voltage.
3. When ZQ pin is directly connected to V_{DDQ} , output impedance is set to minimum and it cannot be connected to ground or left unconnected.

Background

Common I/O SRAMs, from a system architecture point of view, are attractive in read dominated or block transfer applications. Therefore, the SigmaDDR-II SRAM interface and truth table are optimized for burst reads and writes. Common I/O SRAMs are unpopular in applications where alternating reads and writes are needed because bus turnaround delays can cut high speed Common I/O SRAM data bandwidth in half.

Burst Operations

Read and write operations are “burst” operations. In every case where a read or write command is accepted by the SRAM, it will respond by issuing or accepting four beats of data, executing a data transfer on subsequent rising edges of K and \bar{K} , as illustrated in the timing diagrams. New addresses can be loaded no more often than every other K clock cycle. Addresses can be loaded less often, if intervening deselect cycles are inserted.

Deselect Cycles

Chip Deselect commands are pipelined to the same degree as read commands. This means that if a deselect command is applied to the SRAM on the next cycle after a read command captured by the SRAM, the device will complete the four beat read data transfer and then execute the deselect command, returning the output drivers to high-Z. A high on the $LD\#$ pin prevents the RAM from loading read or write command inputs and puts the RAM into deselect mode as soon as it completes all outstanding burst transfer operations.

SigmaDDR-II Burst of 4 SRAM Read Cycles

The status of the Address, $LD\#$ and $R/W\#$ pins are evaluated on the rising edge of K . Because the device executes a four beat burst transfer in response to a read command, if the previous command captured was a read or write command, the Address, \bar{LD} and R/\bar{W} pins are ignored. If the previous command captured was a deselect, the control pin status is checked. The SRAM executes pipelined reads. The read command is clocked into the SRAM by a rising edge of K . After the next rising edge of K , the SRAM produces data out in response to the next rising edge of \bar{C} (or the next rising edge of \bar{K} , if C and \bar{C} are tied high). The second beat of data is transferred on the next rising edge of C , then on the next rising edge of \bar{C} and finally on the next rising edge of C , for a total of four transfers per address load.

SigmaDDR-II Burst of 4 SRAM Write Cycles

The status of the Address, \bar{LD} and R/\bar{W} pins are evaluated on the rising edge of K . Because the device executes a four beat burst transfer in response to a write command, if the previous command captured was a read or write command, the Address, \bar{LD} and R/\bar{W} pins are ignored at the next rising edge of K . If the previous command captured was a deselect, the control pin status is checked. The SRAM executes “late write” data transfers. Data in is due at the device inputs on the rising edge of K following the rising edge of K clock used to clock in the write command and the write address. To complete the remaining three beats of the burst of four write transfer the SRAM captures data in on the next rising edge of \bar{K} , the following rising edge of K and finally on the next rising edge of \bar{K} , for a total of four transfers per address load.

Not Recommended for New Design - Discontinued Product

Special Functions

Byte Write and Nybble Write Control

Byte Write Enable pins are sampled at the same time that Data In is sampled. A high on the Byte Write Enable pin associated with a particular byte (e.g., $\overline{BW0}$ controls D0–D8 inputs) will inhibit the storage of that particular byte, leaving whatever data may be stored at the current address at that byte location undisturbed. Any or all of the Byte Write Enable pins may be driven high or low during the data in sample times in a write sequence.

Each write enable command and write address loaded into the RAM provides the base address for a 4 beat data transfer. The x18 version of the RAM, for example, may write 72 bits in association with each address loaded. Any 9-bit byte may be masked in any write sequence.

Nybble Write (4-bit) write control is implemented on the 8-bit-wide version of the device. For the x8 version of the device, “Nybble Write Enable” and “ \overline{NBx} ” may be substituted in all the discussion above.

Example x18 RAM Write Sequence using Byte Write Enables

Data In Sample Time	$\overline{BW0}$	$\overline{BW1}$	D0–D8	D9–D17
Beat 1	0	1	Data In	Don't Care
Beat 2	1	0	Don't Care	Data In
Beat 3	0	0	Data In	Data In
Beat 4	1	0	Don't Care	Data In

Resulting Write Operation

Byte 1 D0–D8	Byte 2 D9–D17	Byte 1 D0–D8	Byte 2 D9–D17	Byte 1 D0–D8	Byte 2 D9–D17	Byte 1 D0–D8	Byte 2 D9–D17
Written	Unchanged	Unchanged	Written	Written	Written	Unchanged	Written
Beat 1		Beat 2		Beat 3		Beat 4	

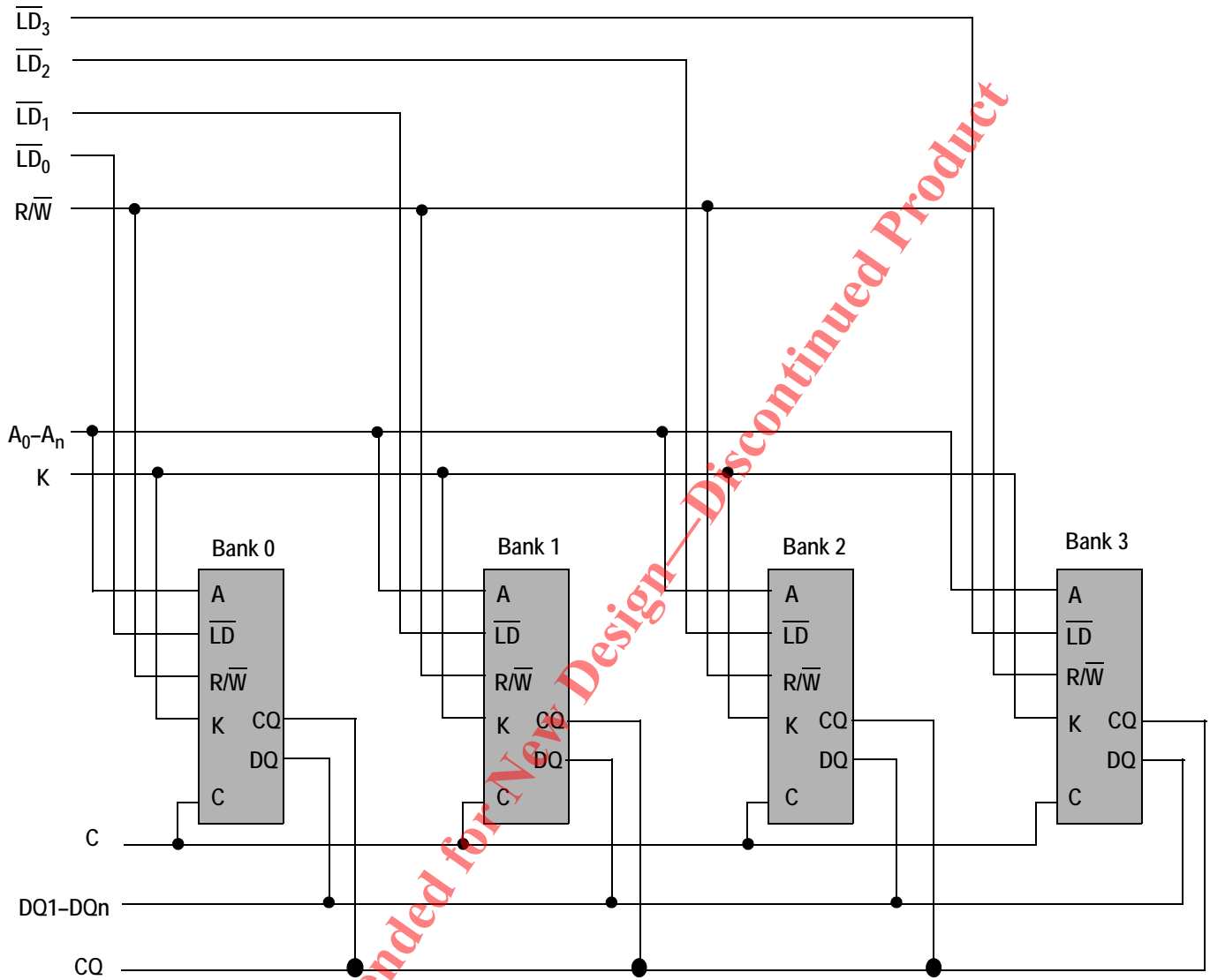
Output Register Control

SigmaDDR-II SRAMs offer two mechanisms for controlling the output data registers. Typically, control is handled by the Output Register Clock inputs, C and \overline{C} . The Output Register Clock inputs can be used to make small phase adjustments in the firing of the output registers by allowing the user to delay driving data out as much as a few nanoseconds beyond the next rising edges of the K and \overline{K} clocks. If the C and \overline{C} clock inputs are tied high, the RAM reverts to K and \overline{K} control of the outputs, allowing the RAM to function as a conventional pipelined read SRAM.

FLXDrive-II Output Driver Impedance Control

HSTL I/O SigmaDDR-II SRAMs are supplied with programmable impedance output drivers. The ZQ pin must be connected to V_{SS} via an external resistor, RQ, to allow the SRAM to monitor and adjust its output driver impedance. The value of RQ must be 5X the value of the desired RAM output impedance at mid-rail. The allowable range of RQ to guarantee impedance matching continuously is between 175Ω and 350Ω. Periodic readjustment of the output driver impedance is necessary as the impedance is affected by drifts in supply voltage and temperature. The SRAM's output impedance circuitry compensates for drifts in supply voltage and temperature. A clock cycle counter periodically triggers an impedance evaluation, resets and counts again. Each impedance evaluation may move the output driver impedance level one step at a time towards the optimum level. The output driver is implemented with discrete binary weighted impedance steps.

Example Four Bank Depth Expansion Schematic



Note:
For simplicity $\overline{\text{B}}\text{W}_n$ (or $\overline{\text{N}}\text{W}_n$), $\overline{\text{K}}$, and C are not shown.

Common I/O SigmaDDR-II Burst of 4 SRAM Truth Table

K_n	\overline{LD}	$R\overline{W}$	DQ				Operation
			A + 0	A + 1	A + 2	A + 3	
\uparrow	1	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Deselect
\uparrow	0	0	$D@K_{n+1}$	$D@K_{n+1}$	$D@K_{n+2}$	$D@K_{n+2}$	Write
\uparrow	0	1	$Q@K_{n+1}$ or C_{n+1}	$Q@K_{n+2}$ or C_{n+2}	$Q@K_{n+2}$ or C_{n+2}	$Q@K_{n+3}$ or C_{n+3}	Read

Note:

Q is controlled by K clocks if C clocks are not used.

Burst of 4 Byte Write Clock Truth Table

\overline{BW}	\overline{BW}	\overline{BW}	\overline{BW}	Current Operation	D	D	D	D
$K \uparrow$ (t_{n+1})	$\overline{K} \uparrow$ ($t_{n+1/2}$)	$K \uparrow$ (t_{n+2})	$\overline{K} \uparrow$ ($t_{n+2/2}$)	$K \uparrow$ (t_n)	$K \uparrow$ (t_{n+1})	$\overline{K} \uparrow$ ($t_{n+1/2}$)	$K \uparrow$ (t_{n+2})	$\overline{K} \uparrow$ ($t_{n+2/2}$)
T	T	T	T	Write Dx stored if $\overline{BW}_n = 0$ in all four data transfers	D0	D2	D3	D4
T	F	F	F	Write Dx stored if $\overline{BW}_n = 0$ in 1st data transfer only	D0	X	X	X
F	T	F	F	Write Dx stored if $\overline{BW}_n = 0$ in 2nd data transfer only	X	D1	X	X
F	F	T	F	Write Dx stored if $\overline{BW}_n = 0$ in 3rd data transfer only	X	X	D2	X
F	F	F	T	Write Dx stored if $\overline{BW}_n = 0$ in 4th data transfer only	X	X	X	D3
F	F	F	F	Write Abort No Dx stored in any of the four data transfers	X	X	X	X

Notes:

- "1" = input "high"; "0" = input "low"; "X" = input "don't care"; "T" = input "true"; "F" = input "false".
- If one or more $\overline{BW}_n = 0$, then $BW = "T"$, else $BW = "F"$.

Burst of 4 Nybble Write Clock Truth Table

\overline{NW}	\overline{NW}	\overline{NW}	\overline{NW}	Current Operation	D	D	D	D
$K \uparrow$ (t_{n+1})	$\overline{K} \uparrow$ ($t_{n+1\frac{1}{2}}$)	$K \uparrow$ (t_{n+2})	$\overline{K} \uparrow$ ($t_{n+2\frac{1}{2}}$)	$K \uparrow$ (t_n)	$K \uparrow$ (t_{n+1})	$\overline{K} \uparrow$ ($t_{n+1\frac{1}{2}}$)	$K \uparrow$ (t_{n+2})	$\overline{K} \uparrow$ ($t_{n+2\frac{1}{2}}$)
T	T	T	T	Write Dx stored if $\overline{NWn} = 0$ in all four data transfers	D0	D2	D3	D4
T	F	F	F	Write Dx stored if $\overline{NWn} = 0$ in 1st data transfer only	D0	X	X	X
F	T	F	F	Write Dx stored if $\overline{NWn} = 0$ in 2nd data transfer only	X	D1	X	X
F	F	T	F	Write Dx stored if $\overline{NWn} = 0$ in 3rd data transfer only	X	X	D2	X
F	F	F	T	Write Dx stored if $\overline{NWn} = 0$ in 4th data transfer only	X	X	X	D3
F	F	F	F	Write Abort No Dx stored in any of the four data transfers	X	X	X	X

Notes:

- "1" = input "high"; "0" = input "low"; "X" = input "don't care"; "T" = input "true"; "F" = input "false".
- If one or more $\overline{NWn} = 0$, then $\overline{NW} = "T"$, else $\overline{NW} = "F"$.

Not Recommended for New Design - Discontinued Product

x36 Byte Write Enable (\overline{BWn}) Truth Table

$\overline{BW0}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	D0–D8	D9–D17	D18–D26	D27–D35
1	1	1	1	Don't Care	Don't Care	Don't Care	Don't Care
0	1	1	1	Data In	Don't Care	Don't Care	Don't Care
1	0	1	1	Don't Care	Data In	Don't Care	Don't Care
0	0	1	1	Data In	Data In	Don't Care	Don't Care
1	1	0	1	Don't Care	Don't Care	Data In	Don't Care
0	1	0	1	Data In	Don't Care	Data In	Don't Care
1	0	0	1	Don't Care	Data In	Data In	Don't Care
0	0	0	1	Data In	Data In	Data In	Don't Care
1	1	1	0	Don't Care	Don't Care	Don't Care	Data In
0	1	1	0	Data In	Don't Care	Don't Care	Data In
1	0	1	0	Don't Care	Data In	Don't Care	Data In
0	0	1	0	Data In	Data In	Don't Care	Data In
1	1	0	0	Don't Care	Don't Care	Data In	Data In
0	1	0	0	Data In	Don't Care	Data In	Data In
1	0	0	0	Don't Care	Data In	Data In	Data In
0	0	0	0	Data In	Data In	Data In	Data In

x18 Byte Write Enable (\overline{BWn}) Truth Table

$\overline{BW0}$	$\overline{BW1}$	D0–D8	D9–D17
1	1	Don't Care	Don't Care
0	1	Data In	Don't Care
1	0	Don't Care	Data In
0	0	Data In	Data In

x8 Nybble Write Enable (\overline{NWn}) Truth Table

$\overline{NW0}$	$\overline{NW1}$	D0–D3	D4–D7
1	1	Don't Care	Don't Care
0	1	Data In	Don't Care
1	0	Don't Care	Data In
0	0	Data In	Data In

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	-0.5 to 2.9	V
V_{DDQ}	Voltage in V_{DDQ} Pins	-0.5 to V_{DD}	V
V_{REF}	Voltage in V_{REF} Pins	-0.5 to V_{DDQ}	V
$V_{I/O}$	Voltage on I/O Pins	-0.5 to $V_{DDQ} + 0.5$ (≤ 2.9 V max.)	V
V_{IN}	Voltage on Other Input Pins	-0.5 to $V_{DDQ} + 0.5$ (≤ 2.9 V max.)	V
I_{IN}	Input Current on Any Pin	+/-100	mA dc
I_{OUT}	Output Current on Any I/O Pin	+/-100	mA dc
T_J	Maximum Junction Temperature	125	$^{\circ}$ C
T_{STG}	Storage Temperature	-55 to 125	$^{\circ}$ C

Note:

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions, for an extended period of time, may affect reliability of this component.

Recommended Operating Conditions

Power Supplies

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	1.7	1.8	1.9	V
I/O Supply Voltage	V_{DDQ}	1.4	—	V_{DD}	V
Reference Voltage	V_{REF}	0.68	—	0.95	V

Note:

The power supplies need to be powered up simultaneously or in the following sequence: V_{DD} , V_{DDQ} , V_{REF} , followed by signal inputs. The power down sequence must be the reverse. V_{DDQ} must not exceed V_{DD} . For more information, read **AN1021 SigmaQuad and SigmaDDR Power-Up**.

Operating Temperature

Parameter	Symbol	Min.	Typ.	Max.	Unit
Junction Temperature (Commercial Range Versions)	T_J	0	25	85	$^{\circ}$ C
Junction Temperature (Industrial Range Versions)*	T_J	-40	25	100	$^{\circ}$ C

Note:

* The part numbers of Industrial Temperature Range versions end with the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.

Thermal Impedance

Package	Test PCB Substrate	θ_{JA} (C°/W) Airflow = 0 m/s	θ_{JA} (C°/W) Airflow = 1 m/s	θ_{JA} (C°/W) Airflow = 2 m/s	θ_{JB} (C°/W)	θ_{JC} (C°/W)
165 BGA	4-layer	16.4	13.4	12.4	8.6	1.2

Notes:

1. Thermal Impedance data is based on a number of samples from multiple lots and should be viewed as a typical number.
2. Please refer to JEDEC standard JESD51-6.
3. The characteristics of the test fixture PCB influence reported thermal characteristics of the device. Be advised that a good thermal path to the PCB can result in cooling or heating of the RAM depending on PCB temperature.

HSTL I/O DC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
DC Input Logic High	V_{IH} (dc)	$V_{REF} + 0.10$	$V_{DDQ} + 0.3 V$	V	1
DC Input Logic Low	V_{IL} (dc)	-0.3 V	$V_{REF} - 0.10$	V	1

Notes:

1. Compatible with both 1.8 V and 1.5 V I/O drivers
2. These are DC test criteria. DC design criteria is $V_{REF} \pm 50$ mV. The AC V_{IH}/V_{IL} levels are defined separately for measuring timing parameters.
3. V_{IL} (Min) DC = -0.3 V, V_{IL} (Min) AC = -1.5 V (pulse width ≤ 3 ns).
4. V_{IH} (Max) DC = $V_{DDQ} + 0.3 V$, V_{IH} (Max) AC = $V_{DDQ} + 0.85 V$ (pulse width ≤ 3 ns).

HSTL I/O AC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
AC Input Logic High	V_{IH} (ac)	$V_{REF} + 0.20$	—	V	2,3
AC Input Logic Low	V_{IL} (ac)	—	$V_{REF} - 0.20$	V	2,3
V_{REF} Peak-to-Peak AC Voltage	V_{REF} (ac)	—	5% V_{REF} (DC)	V	1

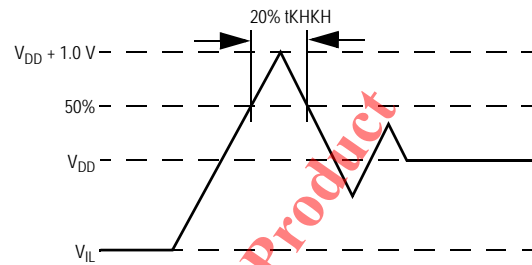
Notes:

1. The peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF} .
2. To guarantee AC characteristics, V_{IH} , V_{IL} , T_{rise} , and T_{fall} of inputs and clocks must be within 10% of each other.
3. For devices supplied with HSTL I/O input buffers. Compatible with both 1.8 V and 1.5 V I/O drivers.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{DD} = 1.8\text{ V}$)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0\text{ V}$	4	5	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0\text{ V}$	6	7	pF
Clock Capacitance	C_{CLK}		5	6	pF

Note:

This parameter is sample tested.

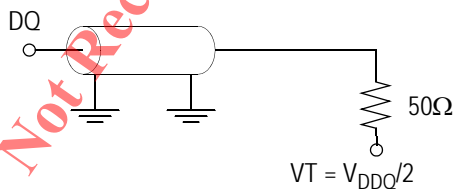
AC Test Conditions

Parameter	Conditions
Input high level	V_{DDQ}
Input low level	0 V
Max. input slew rate	2 V/ns
Input reference level	$V_{DDQ}/2$
Output reference level	$V_{DDQ}/2$

Note:

Test conditions as specified with output loading as shown unless otherwise noted.

AC Test Load Diagram



$R_Q = 250\ \Omega$ (HSTL I/O)
 $V_{REF} = 0.75\text{ V}$

Input and Output Leakage Characteristics

Parameter	Symbol	Test Conditions	Min.	Max
Input Leakage Current (except mode pins)	I_{IL}	$V_{IN} = 0$ to V_{DD}	-2 μ A	2 μ A
$\overline{\text{Doff}}$	$I_{IL\overline{\text{DOFF}}}$	$V_{IN} = 0$ to V_{DD}	-2 μ A	100 μ A
Output Leakage Current	I_{OL}	Output Disable, $V_{OUT} = 0$ to V_{DDQ}	-2 μ A	2 μ A

Programmable Impedance HSTL Output Driver DC Electrical Characteristics

Parameter	Symbol	Min	Max.	Units	Notes
Output High Voltage	V_{OH1}	$V_{DDQ}/2$	V_{DDQ}	V	1, 3
Output Low Voltage	V_{OL1}	V_{SS}	$V_{DDQ}/2$	V	2, 3
Output High Voltage	V_{OH2}	$V_{DDQ} - 0.2$	V_{DDQ}	V	4, 5
Output Low Voltage	V_{OL2}	V_{SS}	0.2	V	4, 6

Notes:

- $I_{OH} = (V_{DDQ}/2) / (RQ/5) \pm 15\%$ @ $V_{OH} = V_{DDQ}/2$ (for: $175\Omega \leq RQ \leq 350\Omega$).
- $I_{OL} = (V_{DDQ}/2) / (RQ/5) \pm 15\%$ @ $V_{OL} = V_{DDQ}/2$ (for: $175\Omega \leq RQ \leq 350\Omega$).
- Parameter tested with $RQ = 250\Omega$ and $V_{DDQ} = 1.5$ V or 1.8 V
- $0\Omega \leq RQ \leq \infty\Omega$
- $I_{OH} = -1.0$ mA
- $I_{OL} = 1.0$ mA

Not Recommended for New Design - Discontinued Product

