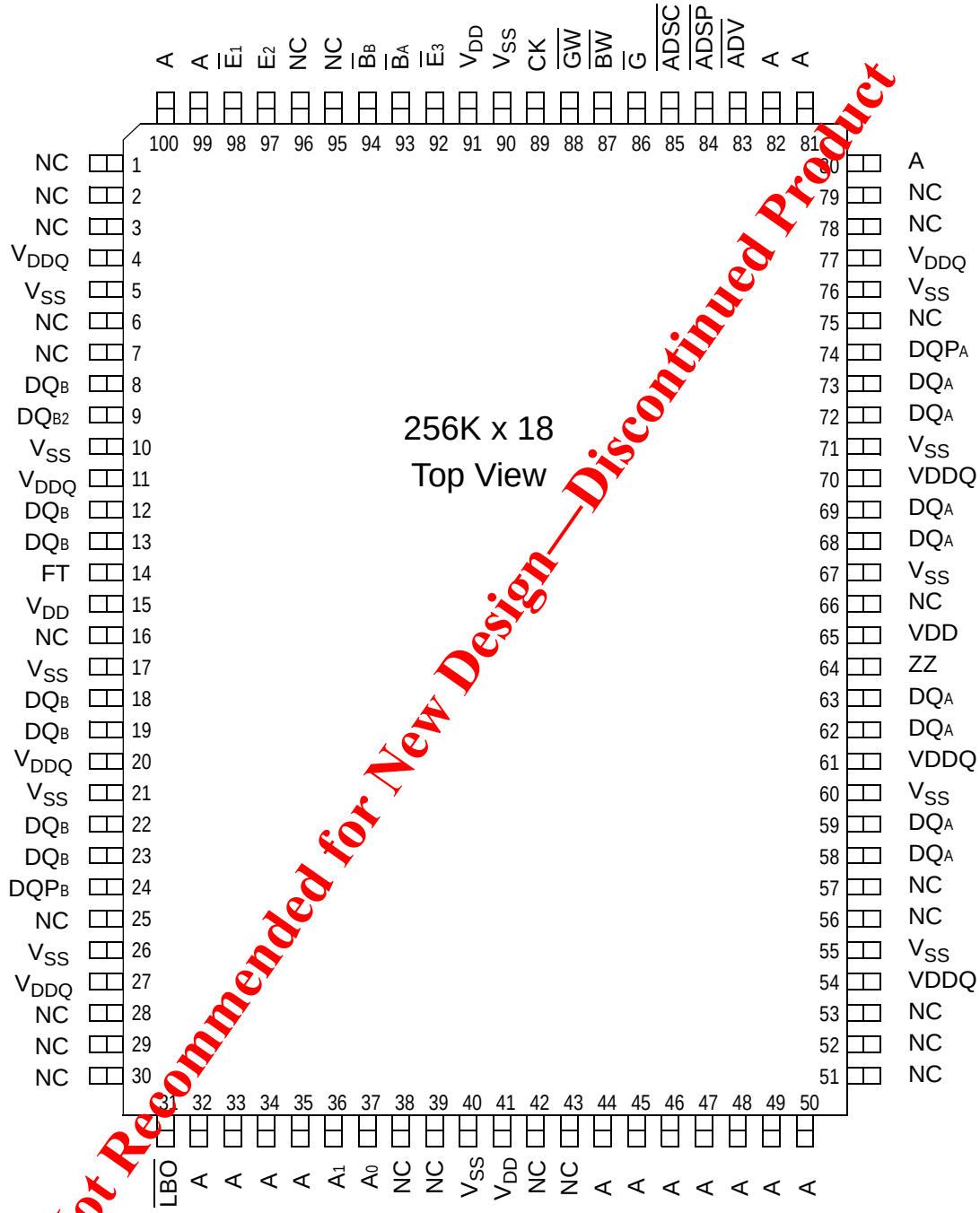
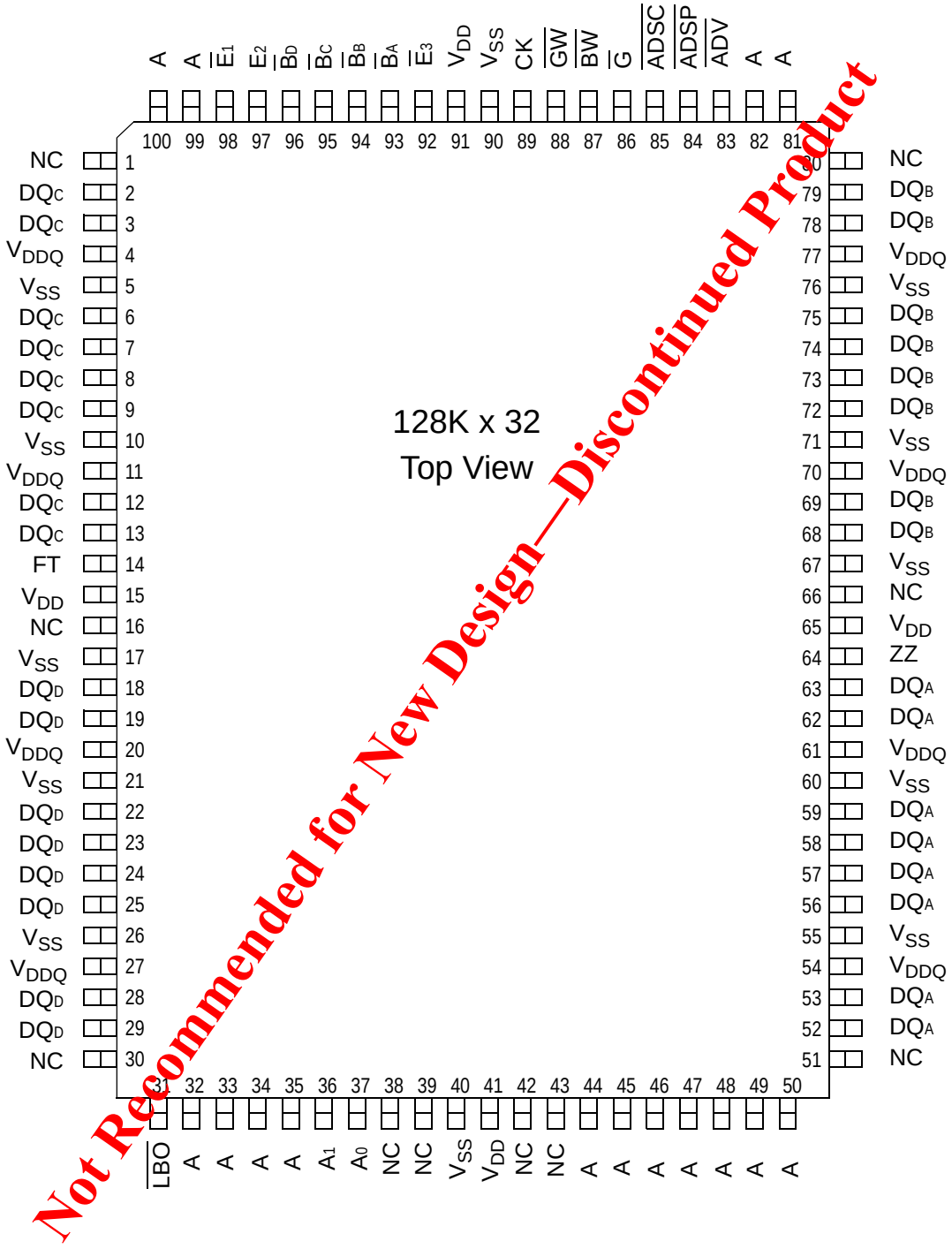
GS840E18A 100-Pin TQFP Pinout (Package T)



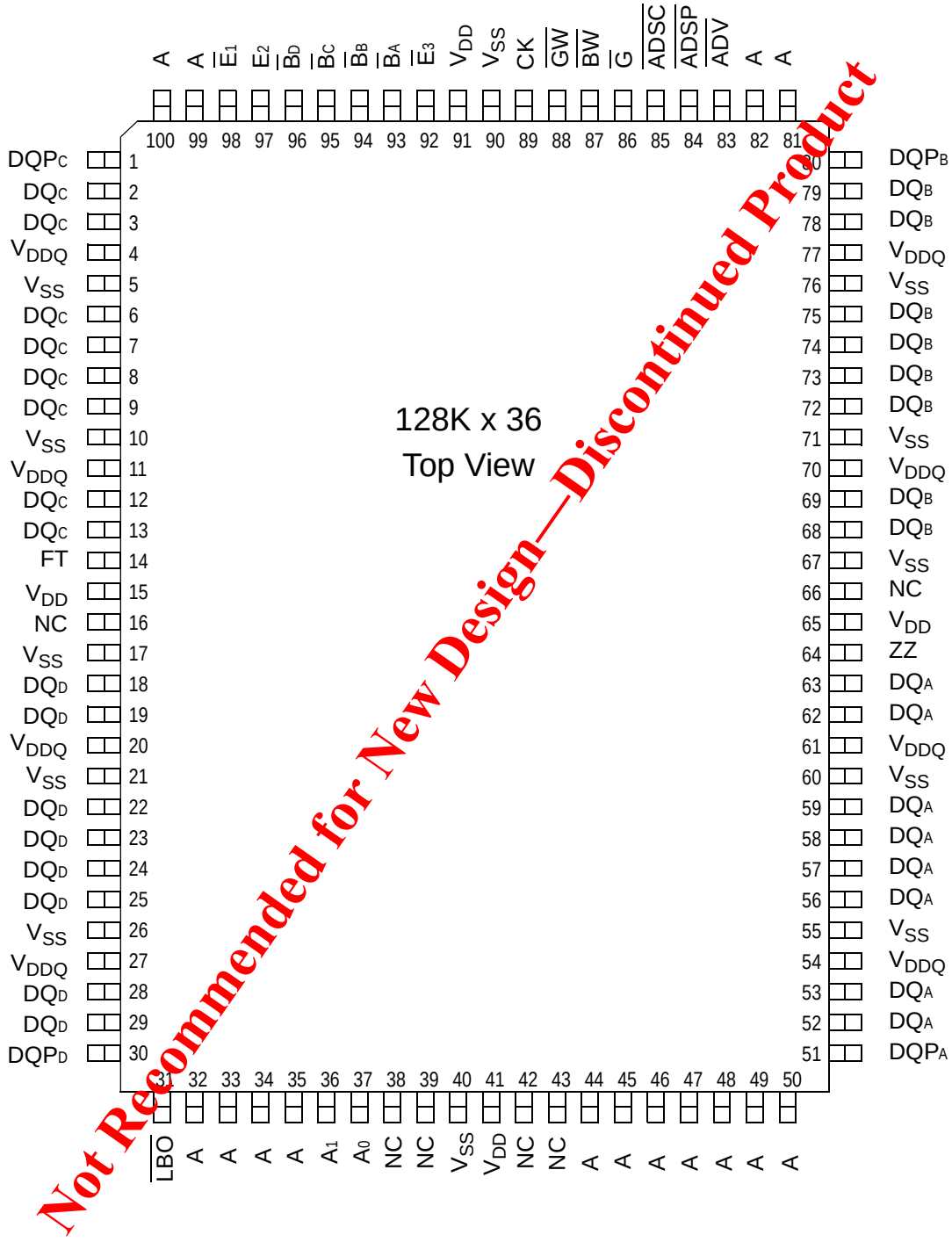
Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

GS840E32A 100-Pin TQFP Pinout (Package T)



Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

GS840E36A 100-Pin TQFP Pinout (Package T)



Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

TQFP Pin Description

Symbol	Type	Description
A_0, A_1	I	Address field LSBs and Address Counter preset Inputs
A	I	Address Inputs
$\overline{B}_A$	In	Byte Write signal for data inputs DQ_A; active low
$\overline{B}_B$	In	Byte Write signal for data inputs DQ_B; active low
$\overline{B}_C$	In	Byte Write signal for data inputs DQ_C; active low
$\overline{B}_D$	In	Byte Write signal for data inputs DQ_D; active low
$\overline{BW}$	I	Byte Write—Writes all enabled bytes; active low
CK	I	Clock Input Signal; active high
$\overline{GW}$	I	Global Write Enable—Writes all bytes; active low
$\overline{E}_1$, $\overline{E}_3$	I	Chip Enable; active low
E_2	I	Chip Enable; active high
$\overline{G}$	I	Output Enable; active low
$\overline{ADV}$	I	Burst address counter advance enable; active low
$\overline{ADSP}$, $\overline{ADSC}$	I	Address Strobe (Processor, Cache Controller); active low
DQ_A	I/O	Byte A Data Input and Output pins
DQ_B	I/O	Byte B Data Input and Output pins
DQ	I/O	Byte C Data Input and Output pins
DQ_D	I/O	Byte D Data Input and Output pins
DQP_A	I/O	9th Data I/O Pin; Byte A
DQP_B	I/O	9th Data I/O Pin; Byte B
DQP_C	I/O	9th Data I/O Pin; Byte C
DQP_D	I/O	9th Data I/O Pin; Byte D
ZZ	I	Sleep Mode control; active high
$\overline{FT}$	I	Flow Through or Pipeline mode; active low
$\overline{LBO}$	I	Linear Burst Order mode; active low
V_{DD}	I	Core power supply
V_{SS}	I	I/O and Core Ground
V_{DDQ}	I	Output driver power supply
NC	-	No Connect

