GeneSiC SEMICONDUCTOR

GA05JT12-263

Normally – OFF Silicon Carbide Junction Transistor

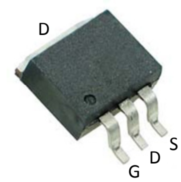
V_{DS}	=	1200 V
$R_{DS(ON)}$	=	260 mΩ
I_D	=	5 A

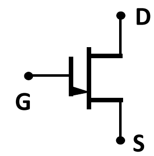
Features

- 175 °C maximum operating temperature
- Temperature independent switching performance
- Gate oxide free SiC switch
- Suitable for connecting an anti-parallel diode
- Positive temperature coefficient for easy paralleling
- Low gate charge
- Low intrinsic output capacitance

Package

- RoHS Compliant





TO-263

Advantages

- SiC transistor most compatible with existing Si gate-drivers
- Low switching losses
- Higher efficiency
- High temperature operation
- High short circuit withstand capability

Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Value	Unit	Notes
Drain – Source Voltage	V_{DS}	V_{GS} = 0 V	1200	V	
Continuous Drain Current	I_D	T_C = 150°C	5	A	Fig. 19
Gate Peak Current	I_{GM}		5	A	
Turn-Off Safe Operating Area	RBSOA	T_{VJ} = 175 °C, I_G = 0.25 A, Clamped Inductive Load	$I_{D,max}$ = 5 @ $V_{DS} \leq V_{DSmax}$	A	Fig. 16
Short Circuit Safe Operating Area	SCSOA	T_{VJ} = 175 °C, I_G = 1.5 A, V_{DS} = 70 V, Non Repetitive	20	µs	
Reverse Gate – Source Voltage	V_{SG}		30	V	
Reverse Drain – Source Voltage	V_{SD}		25	V	
Power Dissipation	P_{tot}	T_C = 150 °C	17.7	W	Fig. 14
Storage Temperature	T_{stg}		-55 to 175	°C	

Electrical Characteristics

Parameter	Symbol	Conditions	Value Min.	Value Typical	Value Max.	Unit	Notes
On State Characteristics							
Drain – Source On Resistance	$R_{DS(ON)}$	I_D = 5 A, T_j = 25 °C I_D = 5 A, T_j = 125 °C I_D = 5 A, T_j = 175 °C		260 368 455		mΩ	Fig. 5
Gate Forward Voltage	$V_{GS(FWD)}$	I_G = 500 mA, T_j = 25 °C I_G = 500 mA, T_j = 175 °C		3.06 2.79		V	Fig. 4
DC Current Gain	β	V_{DS} = 5 V, I_D = 5 A, T_j = 25 °C V_{DS} = 5 V, I_D = 5 A, T_j = 125 °C V_{DS} = 5 V, I_D = 5 A, T_j = 175 °C		80 60 55		–	Fig. 5
Off State Characteristics							
Drain Leakage Current	I_{DSS}	V_R = 1200 V, V_{GS} = 0 V, T_j = 25 °C V_R = 1200 V, V_{GS} = 0 V, T_j = 125 °C V_R = 1200 V, V_{GS} = 0 V, T_j = 175 °C		<1 1 2		µA	Fig. 6
Gate Leakage Current	I_{SG}	V_{SG} = 20 V, T_j = 25 °C		20		nA	

Electrical Characteristics

Parameter	Symbol	Conditions	Value Min.	Value Typical	Value Max.	Unit	Notes
Capacitance Characteristics							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_D = 300 V, *f* = 1 MHz		527		pF	Fig. 7
Reverse Transfer/Output Capacitance	C_{rss}/C_{oss}	V_D = 300 V, *f* = 1 MHz		24		pF	Fig. 7
Output Capacitance Stored Energy	E_{OSS}	V_{GS} = 0 V, V_D = 300 V, *f* = 1 MHz		1.1		µJ	Fig. 8
Switching Characteristics[1]							
Gate Resistance, Internal	$R_{G(INT)}$	*f* = 1 MHz, V_{AC} = 25 mV, T_j = 175 ºC		14.5		Ω	
Turn On Delay Time	$t_{d(on)}$	T_j = 25 ºC, V_{DS} = 200 V, I_D = 5 A, $R_{G(EXT)}$ = 100 Ω, C_G = 10 nF, V_G = 20/-5 V, Load = 40 Ω Refer to Fig. 16 for I_G Waveform		13.0		ns	
Fall Time, V_{DS}	t_f			12.4		ns	Fig. 9, 11
Turn Off Delay Time	$t_{d(off)}$			12.0		ns	
Rise Time, V_{DS}	t_r			6.6		ns	Fig. 10, 12
Turn On Delay Time	$t_{d(on)}$	T_j = 175 ºC, V_{DS} = 200 V, I_D = 5 A, $R_{G(EXT)}$ = 100 Ω, C_G = 10 nF, V_G = 20/-5 V, Load = 40 Ω Refer to Fig. 16 for I_G Waveform		7.0		ns	
Fall Time, V_{DS}	t_f			12.2		ns	Fig. 9
Turn Off Delay Time	$t_{d(off)}$			30.0		ns	
Rise Time, V_{DS}	t_r			6.9		ns	Fig. 10
Turn-On Energy Per Pulse	E_{on}	T_j = 25 ºC, V_{DS} = 200 V, I_D = 5 A, $R_{G(EXT)}$ = 100 Ω, C_G = 10 nF, V_G = 20/-5 V, Load = 287 µH		20.6		µJ	Fig. 9, 11
Turn-Off Energy Per Pulse	E_{off}			1.0		µJ	Fig. 10, 12
Total Switching Energy	E_{tot}			21.6		µJ	
Turn-On Energy Per Pulse	E_{on}	T_j = 175 ºC, V_{DS} = 200 V, I_D = 5 A, $R_{G(EXT)}$ = 100 Ω, C_G = 10 nF, V_G = 20/-5 V, Load = 287 µH		18.4		µJ	Fig. 9
Turn-Off Energy Per Pulse	E_{off}			0.6		µJ	Fig. 10
Total Switching Energy	E_{tot}			19.0		µJ	

[1] – All times are relative to the Drain-Source Voltage V_{DS}

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typical	Max.	Unit	Notes
Thermal resistance, junction - case	R_{thJC}			1.41		°C/W	Fig. 17

Figures

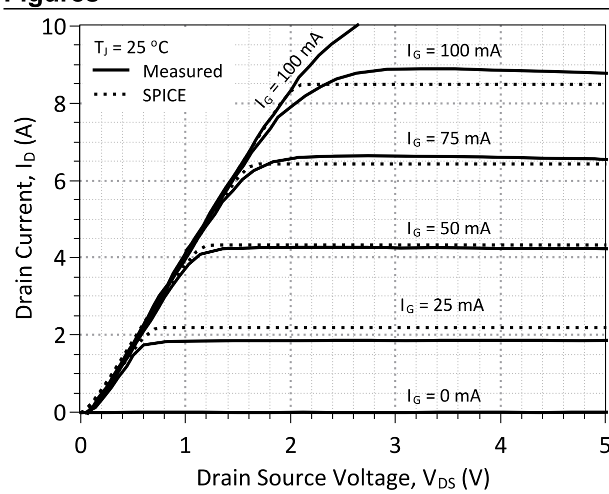


Figure 1: Typical Output Characteristics at 25 °C

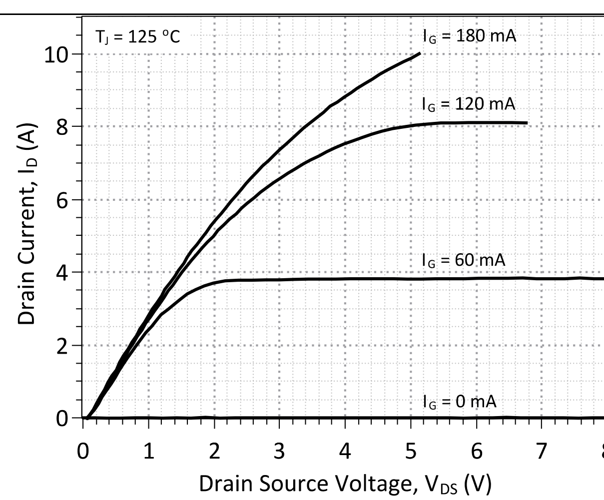


Figure 2: Typical Output Characteristics at 125 °C

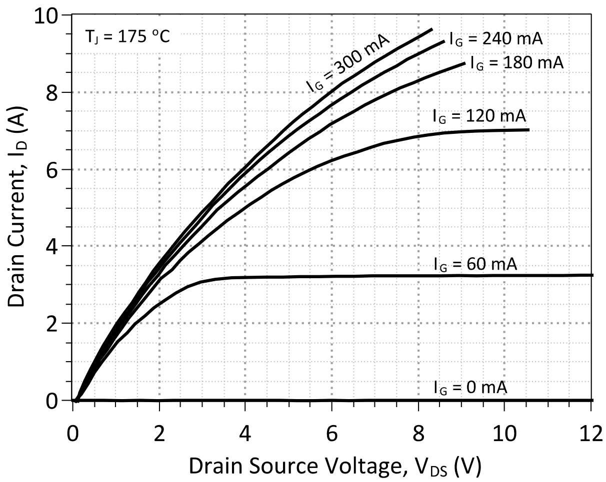


Figure 3: Typical Output Characteristics at 175 °C

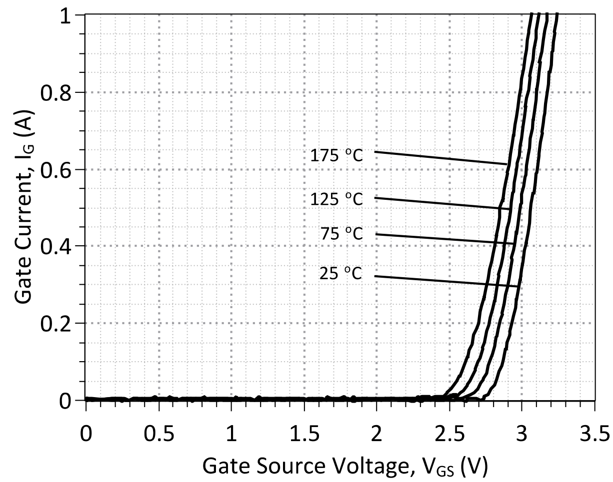


Figure 4: Typical Gate Source I-V Characteristics vs. Temperature

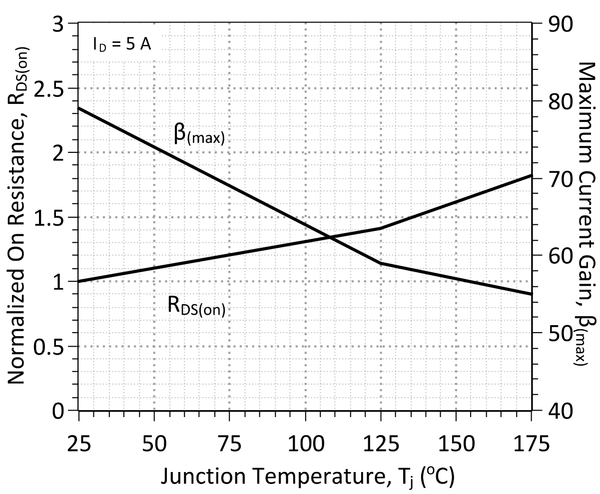


Figure 5: Normalized On-Resistance and Current Gain vs. Temperature

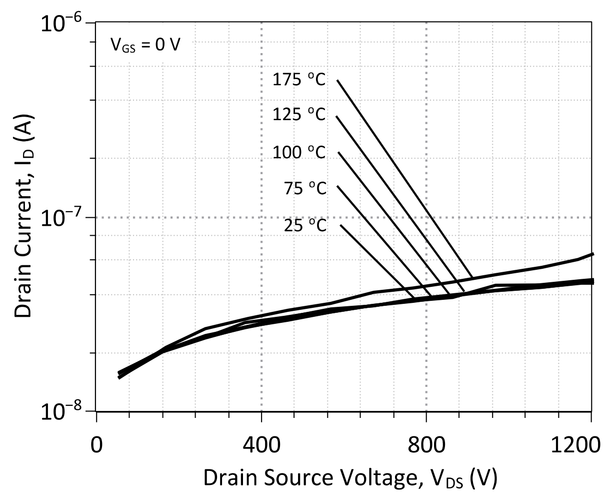


Figure 6: Typical Blocking Characteristics

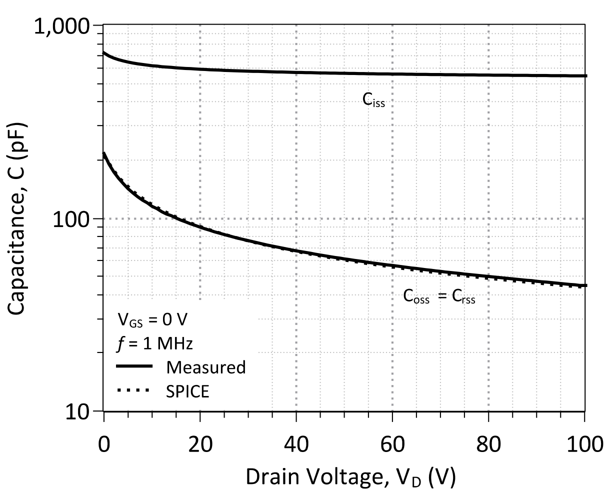


Figure 7: Input, Output, and Reverse Transfer Capacitance

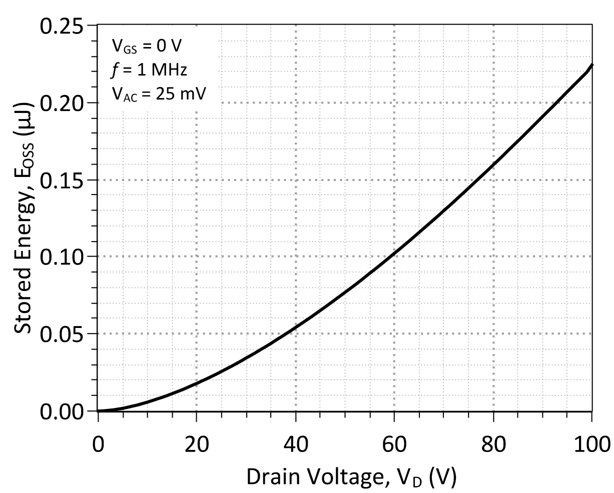


Figure 8: Output Capacitance Stored Energy

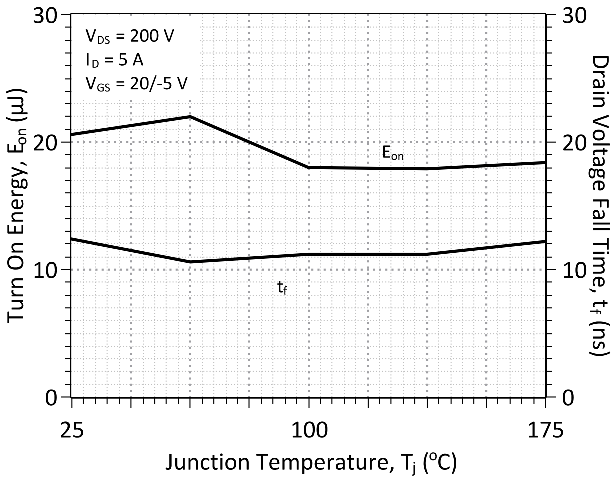


Figure 9: Typical Turn On Energy Losses and Switching Times vs. Temperature

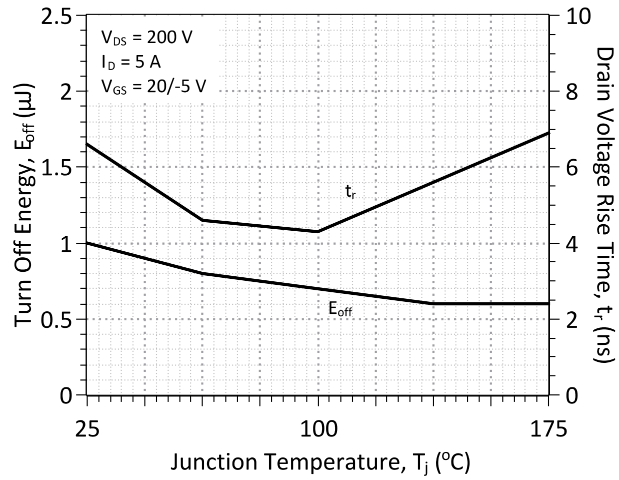


Figure 10: Typical Turn Off Energy Losses and Switching Times vs. Temperature

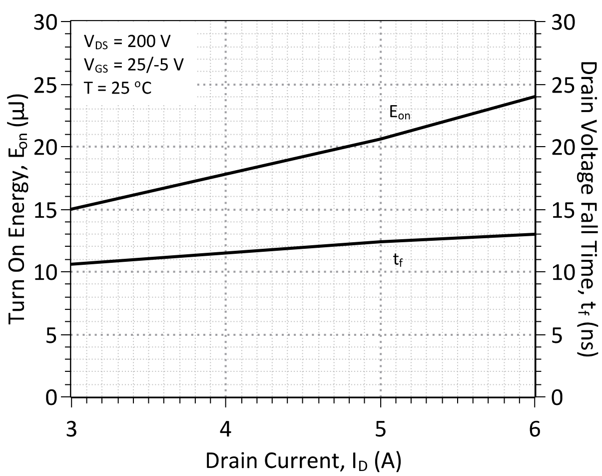


Figure 11: Typical Turn On Energy Losses and Switching Times vs. Drain Current

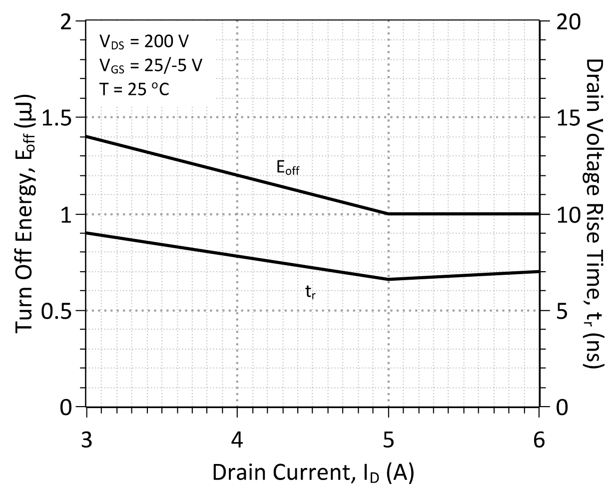


Figure 12: Typical Turn Off Energy Losses and Switching Times vs. Drain Current

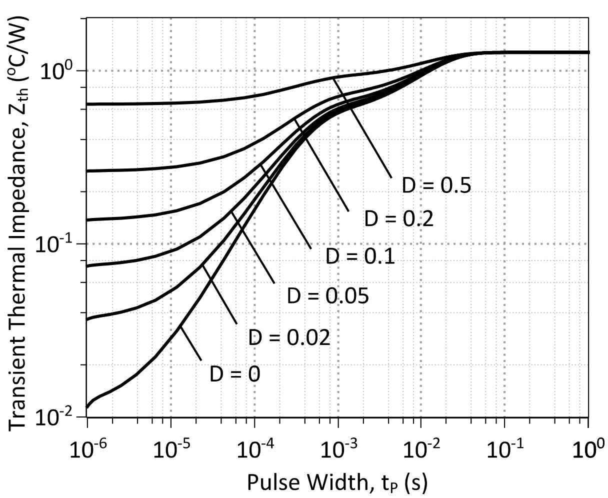


Figure 13: Transient Thermal Impedance

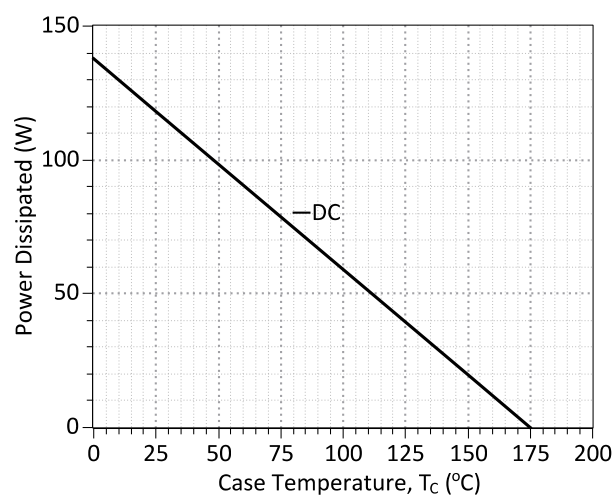


Figure 14: Power Derating Curve

[2] – Representative values based on device conduction and switching loss. Actual losses will depend on gate drive conditions, device load, and circuit topology.

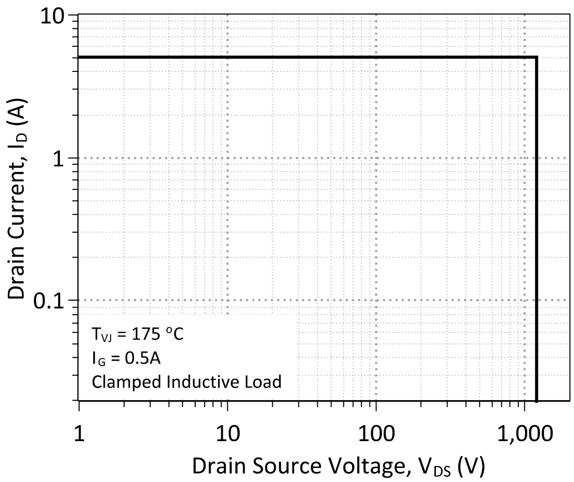


Figure 15: Turn-Off Safe Operating Area

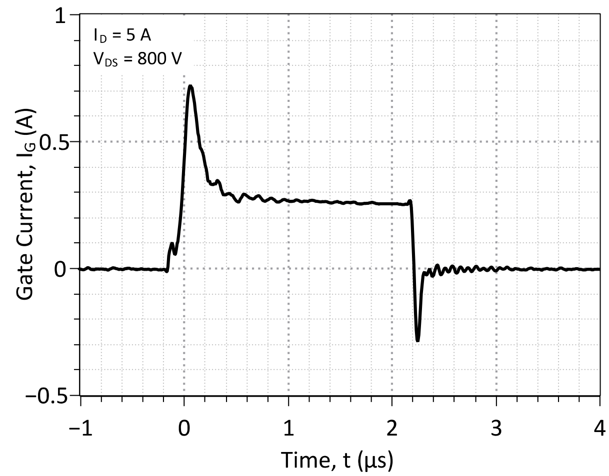


Figure 16: Typical Gate Current Waveform

Commercial Gate Drivers Compatible with GA05JT12-263

Manufacturer	Part Number	Features				
		Optical Signal Isolation	Desaturation Detection	Active Miller Gate Clamping[3]	High Side Capability	Number of Outputs
IXYS	IX2204	–	✓	–	✓	2
Avago Tech.	HCPL-316J	✓	✓	–	✓	1
Avago Tech.	HCPL-322J	✓	✓	✓	✓	1
Concept	1SC2060P	✓[4]	✓	✓	✓[4]	1
IXYS	IXD_604	–	–	–	✓	2
IXYS	IXD_614	–	–	–	✓	1
IXYS	IXD_630	–	–	–	✓	1
IXYS	IRFD630	–	–	–	✓	1
Micrel	MIC4452YN	–	–	–	✓	1
Microsemi	LX4510	–	–	–	✓	1
Texas Instruments	UCC27322	–	–	–	✓	1

[3] – Active Miller Gate Clamping recommended for V_{EE} = GND switching applications as SJT and/or output BJT secondary gate discharge path.
[4] – Features built-in galvanic signal and supply voltage isolation, replaces optical isolation on signal.
[5] – Specialized for high-temperature operation of gate drive circuitry.

Silicon IGBT/MOSFET gate drivers (see partial list above) typically offer sufficient gate currents to drive the GA05JT12-263. Specific product information should be obtained from the individual product manufacturers.

The GA05JT12-263 can be driven similar to silicon IGBTs or MOSFETs in which a gate driver IC is used to supply positive gate current peaks to the device at turn-on and negative current peaks at turn-off. Unlike the IGBT or MOSFET, the GA05JT12-263 also requires a continuous gate current for the device to remain on after the initial current peak. An example gate current waveform for the GA05JT12-263 is shown in Fig. 16.

Single-Level SJT Gate Drive

Producing the necessary gate current peaks and continuous currents can be accomplished by using a gate drive circuit shown in Fig. 17. The gate driver output node is connected to an optional NPN/PNP silicon BJT pair in a totem pole configuration which may provide higher gate current to the SJT gate. The NPN/PNP pair are controlled by the gate drive IC connected through base resistor R_b. The pair's output at node N_1 is connected to gate resistor $R_{G(EXT)}$ and capacitor C_G located in parallel and connected to the SJT gate terminal. The gate resistor determines the continuous gate current. The gate capacitor produces positive and negative current peaks, which enable fast charging and discharging of the SJT's terminal capacitances. Additional detail on the single-level SJT gate driving technique is discussed in GeneSiC Semiconductor Application Note AN-10A. (http://www.genesicsemi.com/references/product-notes)

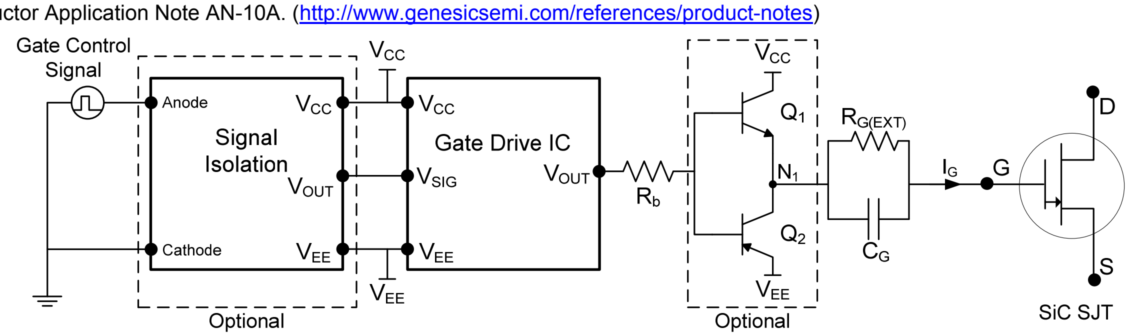


Figure 17: Single-Level SJT Gate Diver Configuration (External signal isolation recommended for non-isolated gate driver ICs.)

Single-Level Gate Drive Conditions

Parameter	Symbol	Conditions	Values			Units
			Range	Typical	Peak SJT Performance[6]	
Supply Voltage	V_{CC}		6 – 30	15 – 18	≥ 25	V
Negative Supply Voltage	V_{EE}		-10 – GND	-5	≤ -5	V
Output Current, Peak	$I_{OUT,\,pk}$	Package Limited	0.7 – 3	0.75	≥ 1	A
Output Current, Continuous	I_{OUT}	Package Limited, T = 175°C	0.1 – 1.0	0.25	≥ 0.3	A
Output Gate Components						
Gate Resistance, External	$R_{G(EXT)}$	V_{CC} = 20 V, I_G ≈ 0.5 A, T = 175°C		20	≤ 20	Ω
Gate Capacitance	C_G	V_{CC} = 20 V, $I_{G,pk}$ ≈ 2.0 A, T = 175°C	5 – 30	10	≥ 10	nF
Output BJT Buffer (Optional)	Q_1, Q_2	2N6107/2N6292 pair or equivalent[7]				

[6] – Achieves lowest SJT device energy losses (E_{tot}) and fastest switching times (t_r, t_f).
[7] – Representative complimentary BJT pair with I_C ≥ 5 A and V_{CEO} ≥ 60 V.

Two-Level SJT Gate Drive

The GA05JT12-263 can also be driven with a gate drive circuit shown in Fig. 22, in which two gate drive ICs and NPN/PNP pairs are operated with different supply voltage levels (V_{GH}, V_{GL}) in order to minimize gate drive losses. By using a separate lower voltage output gate driver IC connected to gate resistor $R_{G(EXT)}$, the power consumption of the continuous current is reduced. Additional detail on the two-level SJT gate driving technique is discussed in GeneSiC Semiconductor Application Note AN-10B. (http://www.genesicsemi.com/references/product-notes)

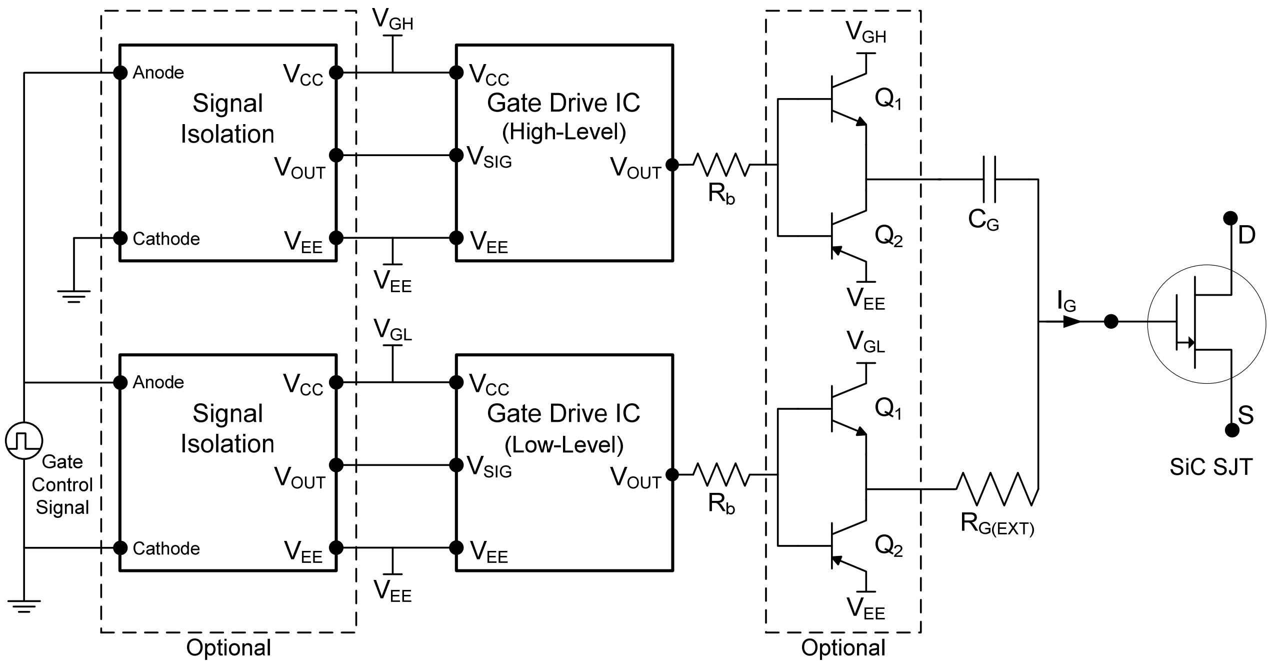


Figure 22: Two-Level SJT Gate Diver Configuration for Reduced Drive Losses (External signal isolation recommended for non-isolated gate driver ICs.)

Two-Level Gate Drive Conditions

Parameter	Symbol	Conditions	Values			Units
			Range	Typical	Peak SJT Performance[8]	
Supply Voltage, High Level Driver	V_{CC} (V_{GH}[9])		10 – 30	15 – 18	≥ 20	V
Supply Voltage, Low Level Driver	V_{CC}(V_{GL}[9])		5 – 8	6.0	≥ 6.5	V
Negative Supply Voltage	V_{EE}		-10 – GND	-5	≤ -5	V
Output Current, Peak	$I_{OUT,\ pk}$	Package Limited	0.7 – 3	2.0	≥ 2.0	A
Output Current, Continuous	I_{OUT}	Package Limited, T = 175 °C		0.5	≥ 0.5	A
Output Gate Components						
Gate Resistance, External	$R_{G(EXT)}$	V_{GL} = 6.0 V, I_G ≈ 0.5 A, T = 175 °C		1.0	≤ 1.0	Ω
Gate Capacitance	C_G	V_{GH} = 20 V, $I_{G,pk}$ ≈ 2.0 A, T = 175 °C	5 – 30	10	≥ 10	nF
Output BJT Buffer (Optional)	Q_1, Q_2	2N6107/2N6292 pair or equivalent[10]				

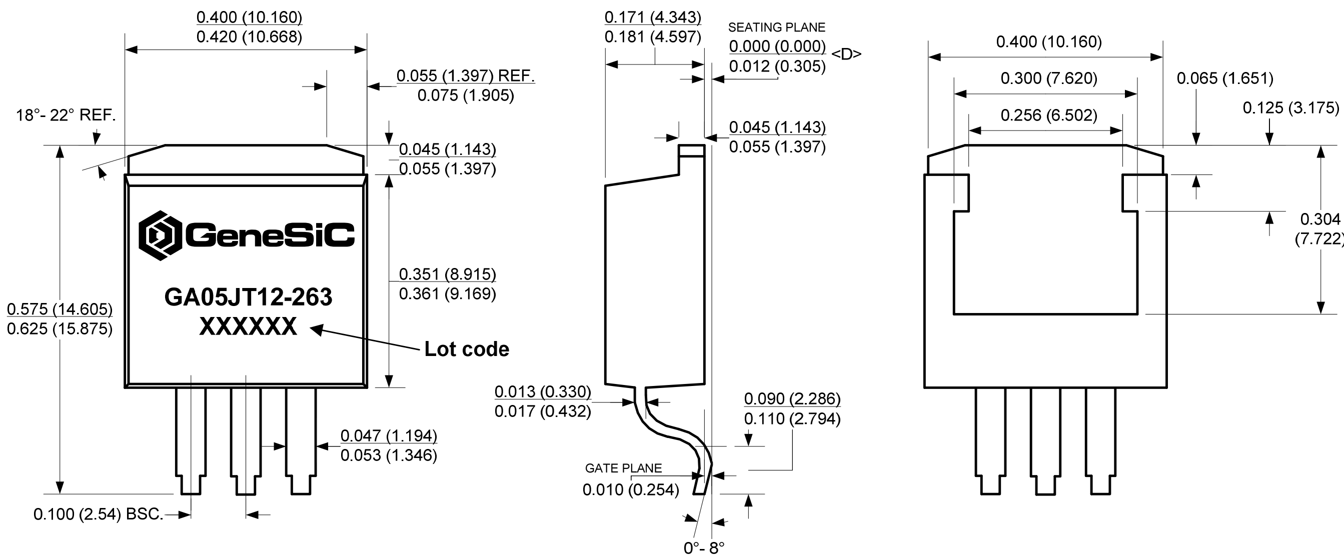
[8] – Achieves lowest SJT device energy losses (E_{tot}) and fastest switching times (t_r, t_f).

[9] – Consult application note AN-10B for more information on parameters V_{GH} and V_{GL}.

[10] – Complimentary BJT pair with I_C ≥ 5 A and V_{CEO} ≥ 60 V

Package Dimensions:

TO-263 PACKAGE OUTLINE



NOTE
1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

Revision History			
Date	Revision	Comments	Supersedes
2014/06/20	0	Initial release	

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SPICE Model Parameters

This is a secure document. Please copy this code from the SPICE model PDF file on our website (www.genesicsemi.com/images/products_sic/sjt/GA05JT12-263_SPICE.pdf) into LTSPICE (version 4) software for simulation of the GA05JT12-263.

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*     MODEL OF GeneSiC Semiconductor Inc.
*
*     $Revision:   1.0           $
*     $Date:   20-JUN-2014       $
*
*     GeneSiC Semiconductor Inc.
*     43670 Trade Center Place Ste. 155
*     Dulles, VA 20166
*
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* OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
* TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
* PARTICULAR PURPOSE."
* Models accurate up to 2 times rated drain current.
*
.model GA05JT12 NPN
+ IS       5.0E-47
+ ISE      1.25E-28
+ EG       3.2
+ BF       80
+ BR       0.55
+ IKF      200
+ NF       1
+ NE       2
+ RB       14.5
+ RE       0.01
+ RC       0.23
+ CJC      2.16E-10
+ VJC      3.656
+ MJC      0.4717
+ CJE      5.021E-10
+ VJE      2.95
+ MJE      0.4867
+ XTI      3
+ XTB      -1.0
+ TRC1     1.050E-2
+ VCEO     1200
+ ICRATING 5
+ MFG      GeneSiC_Semiconductor
*
* End of GA05JT12 SPICE Model
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