Silicon Carbide Junction Transistor/Schottky Diode Co-pack

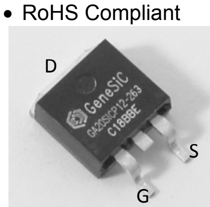
V_{DS}	=	1200 V
$R_{DS(ON)}$	=	60 mΩ
$I_{D\ (Tc\ =\ 25°C)}$	=	45 A
$h_{FE\ (Tc\ =\ 25°C)}$		60

Features

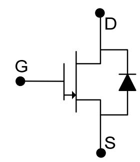
- 175°C Maximum Operating Temperature
- Gate Oxide free SiC switch
- Exceptional Safe Operating Area
- Integrated SiC Schottky Rectifier
- Excellent Gain Linearity
- Temperature Independent Switching Performance
- Low output capacitance
- Positive temperature co-efficient of $R_{DS,ON}$
- Suitable for connecting an anti-parallel diode

Package

- RoHS Compliant



TO-263



Advantages

- Compatible with Si MOSFET/IGBT Gate Drive ICs
- > 20 µs Short-Circuit Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal distortion
- High Amplifier Bandwidth
- Reduced cooling requirements
- Reduced system size

Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Values	Unit
SiC Junction Transistor				
Drain – Source Voltage	V_{DS}	V_{GS} = 0 V	1200	V
Continuous Drain Current	I_D	95 °C < T_C < 135 °C	20	A
Gate Peak Current	I_{GM}		10	A
Turn-Off Safe Operating Area	RBSOA	T_{VJ} = 175 °C, I_G = 1 A, Clamped Inductive Load	$I_{D,max}$ = 20 @ $V_{DS} \leq V_{DSmax}$	A
Short Circuit Safe Operating Area	SCSOA	T_{VJ} = 175 °C, I_G = 1 A, V_{DS} = 800 V, Non Repetitive	20	µs
Reverse Gate – Source Voltage	V_{SG}		30	V
Reverse Drain – Source Voltage	V_{SD}		25	V
Power Dissipation	P_{tot}	T_C = 95 °C	131	W
Storage Temperature	T_{stg}		-55 to 175	°C
Free-wheeling Silicon Carbide diode				
DC-Forward Current	I_F	$T_C \leq$ 150 °C	20	A
Non Repetitive Peak Forward Current	I_{FM}	T_C = 25 °C, t_P = 10 µs	280	A
Surge Non Repetitive Forward Current	$I_{F,SM}$	t_P = 10 ms, half sine, T_C = 25 °C	65	A

Thermal Characteristics

Thermal resistance, junction - case	R_{thJC}	SiC Junction Transistor	0.61	°C/W
Thermal resistance, junction - case	R_{thJC}	SiC Diode	0.82	°C/W

Electrical Characteristics

Parameter	Symbol	Conditions	Values min.	Values typ.	Values max.	Unit
SJT On-State Characteristics						
Drain – Source On Resistance	$R_{DS(ON)}$	I_D = 20 A, I_G = 1000 mA, T_j = 25 °C I_D = 20 A, I_G = 1000 mA, T_j = 125 °C I_D = 20 A, I_G = 1000 mA, T_j = 175 °C		60 90 136		mΩ
Gate Forward Voltage	$V_{GS(FWD)}$	I_G = 1000 mA, T_j = 25 °C I_G = 1000 mA, T_j = 175 °C		3.1 2.9		V
DC Current Gain	h_{FE}	V_{DS} = 5 V, I_D = 20 A, T_j = 25 °C V_{DS} = 5 V, I_D = 20 A, T_j = 175 °C		60 37		
SJT Off-State Characteristics						
Drain Leakage Current	I_{DSS}	V_R = 1200 V, V_{GS} = 0 V, T_j = 25 °C V_R = 1200 V, V_{GS} = 0 V, T_j = 125 °C V_R = 1200 V, V_{GS} = 0 V, T_j = 175 °C		0.1 0.2 0.5	1.0 1.0 1.0	mA
Gate Leakage Current	I_{SG}	V_{SG} = 20 V, T_j = 25 °C		20		nA
SJT Capacitance Characteristics						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_D = 1 V, *f* = 1 MHz		482		pF
Output Capacitance	C_{oss}	V_D = 100 V,00 *f* = 1 MHz		220		pF
Reverse Transfer Capacitance	C_{rss}	V_D = 100 V, *f* = 1 MHz		106		pF
Output Capacitance Stored Energy	E_{OSS}	V_{GS} = 0 V, V_D = 100 V, *f* = 1 MHz		1.1		µJ
SJT Switching Characteristics[1]						
Gate Resistance, Internal	$R_{G(INT)}$	*f* = 1 MHz, V_{AC} = 25 mV, T_j = 175 ºC		2.6		Ω
Turn On Delay Time	$t_{d(on)}$	V_{DD} = 800 V, I_D = 20 A, R_G = 1.53 Ω, C_G = 9.0 nF FWD = GA20SICP12, T_j = 25 ºC Refer to Figure 15 for gate current waveform		15		ns
Rise Time	t_r			20		ns
Turn Off Delay Time	$t_{d(off)}$			30		ns
Fall Time	t_f			50		ns
Turn-On Energy Per Pulse	E_{on}			475		µJ
Turn-Off Energy Per Pulse	E_{off}			300		µJ
Total Switching Energy	E_{ts}			780		µJ
Turn On Delay Time	$t_{d(on)}$	V_{DD} = 800 V, I_D = 20 A, R_G = 1.53 Ω, C_G = 9.0 nF FWD = GA20SICP12, T_j = 175 ºC Refer to Figure 15 for gate current waveform		15		ns
Rise Time	t_r			20		ns
Turn Off Delay Time	$t_{d(off)}$			35		ns
Fall Time	t_f			45		ns
Turn-On Energy Per Pulse	E_{on}			515		µJ
Turn-Off Energy Per Pulse	E_{off}			290		µJ
Total Switching Energy	E_{ts}			805		µJ
Free-Wheeling Silicon Carbide Schottky Diode (FWD) Switching Characteristics[1]						
Forward Voltage	V_F	I_F = 20 A, V_{GE} = 0 V, T_j = 25 ºC (175 ºC)		1.9(3.3)		V
Diode Knee Voltage	$V_{D(knee)}$	T_j = 25 ºC, I_F = 1 mA		0.8		V
Peak Reverse Recovery Current	I_{rrm}	I_F = 20 A, V_{GE} = 0 V, V_R = 800 V, $-dI_F/dt$ = 1060 A/µs, T_j = 25 ºC		9.8		A
Reverse Recovery Time	t_{rr}			30		ns
Rise Time	t_r	V_F= 800 V, I_F = 20 A, R_G = 1.53 Ω, C_G = 9.0 nF, T_j= 25 ºC		60		ns
Fall Time	t_f			20		ns
Turn-On Energy Loss Per Pulse	E_{on}			70		µJ
Turn-Off Energy Loss Per Pulse	E_{off}			50		µJ
Reverse Recovery Charge	Q_{rr}			165		nC
Rise Time	t_r	V_F= 800 V, I_F = 20 A, R_G = 1.53 Ω, C_G = 9.0 nF, T_j= 175 ºC		50		ns
Fall Time	t_f			20		ns
Turn-On Energy Loss Per Pulse	E_{on}			75		µJ
Turn-Off Energy Loss Per Pulse	E_{off}			50		µJ
Reverse Recovery Charge	Q_{rr}			180		nC

[1] – Times measured of co-pack currents I_D and I_F.

Figures

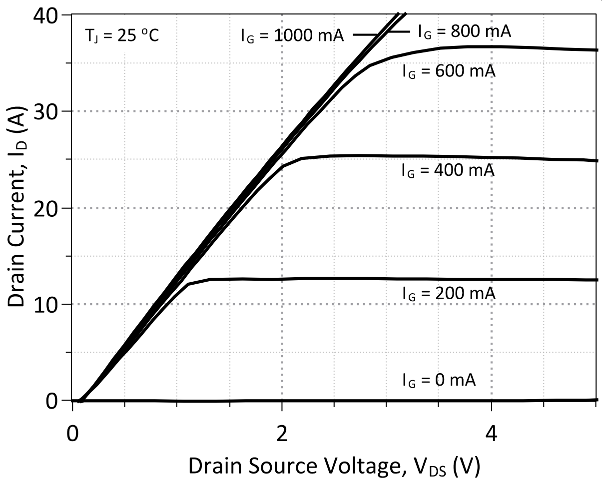


Figure 1: Typical Output Characteristics at 25 °C

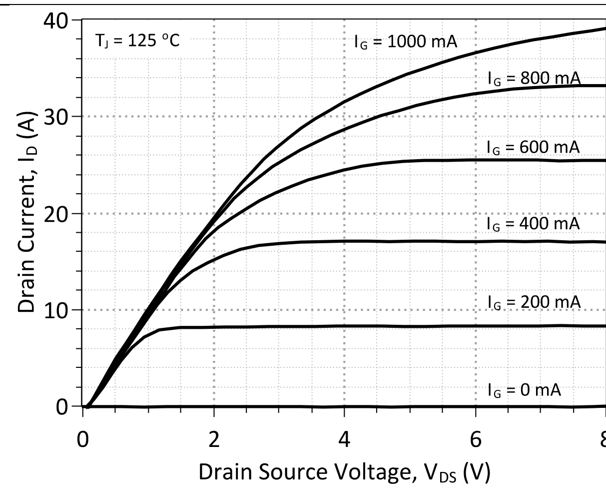


Figure 2: Typical Output Characteristics at 125 °C

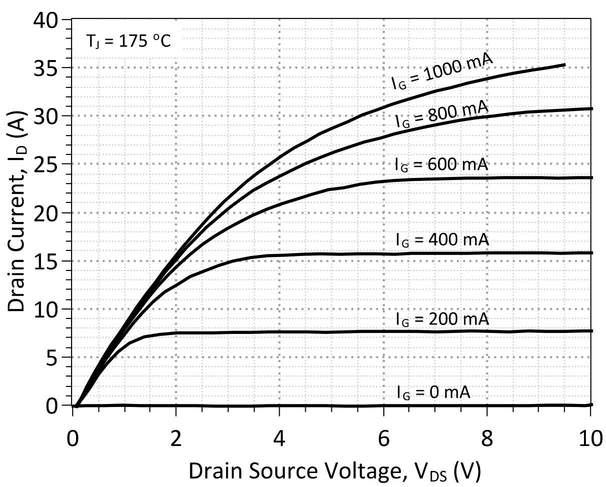


Figure 3: Typical Output Characteristics at 175 °C

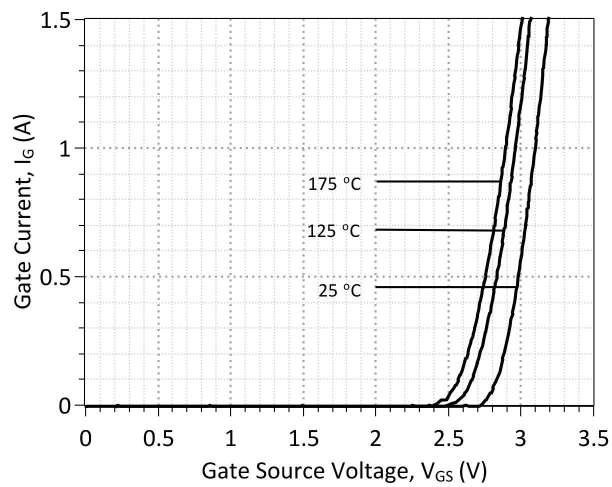


Figure 4: Typical Gate Source I-V Characteristics vs. Temperature

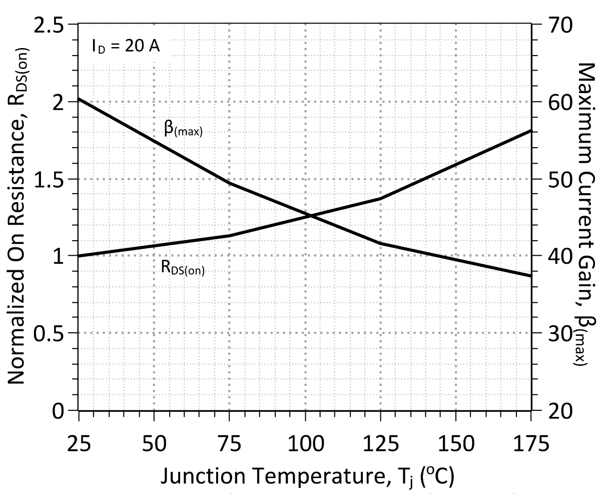


Figure 5: Normalized On-Resistance and Current Gain vs. Temperature

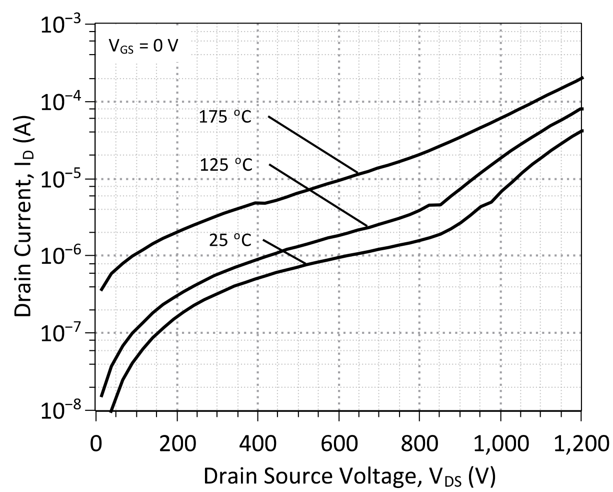


Figure 6: Typical Blocking Characteristics

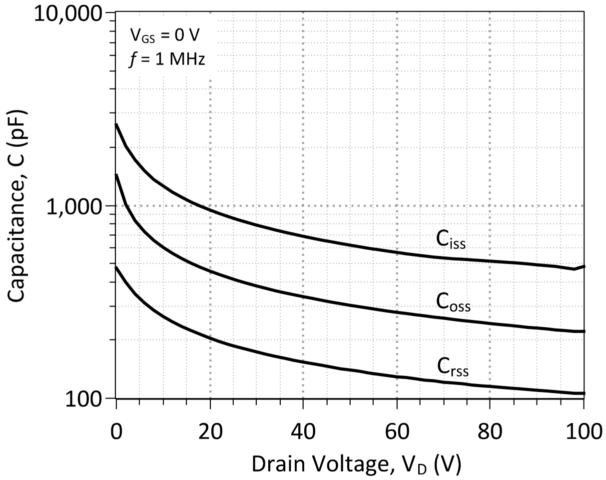


Figure 7: Capacitance Characteristics

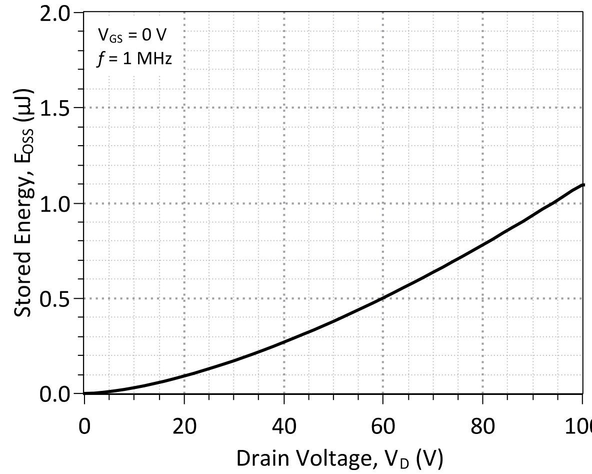


Figure 8: Output Capacitance Stored Energy

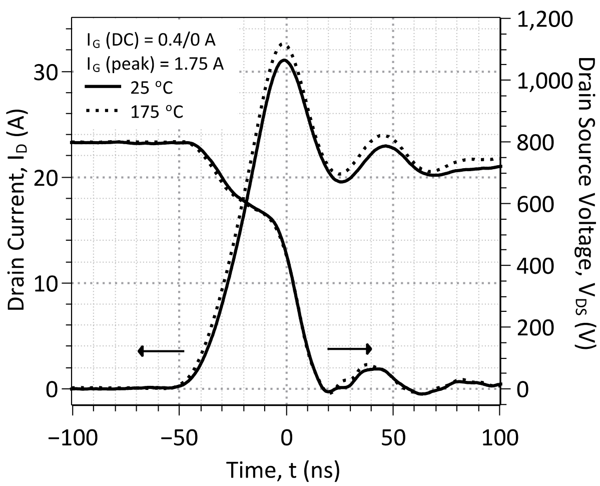


Figure 9: Typical Hard-switched Turn On Waveforms

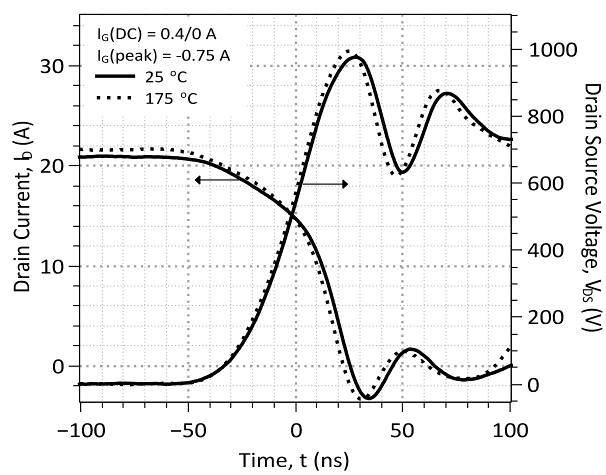


Figure 10: Typical Hard-switched Turn Off Waveforms

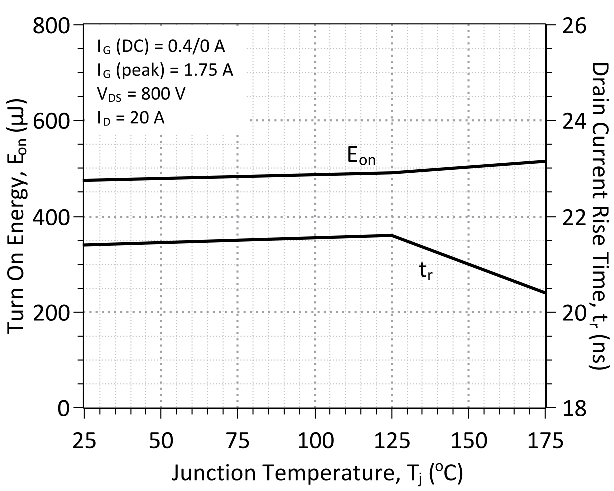


Figure 11: Typical Turn On Energy Losses and Switching Times vs. Temperature

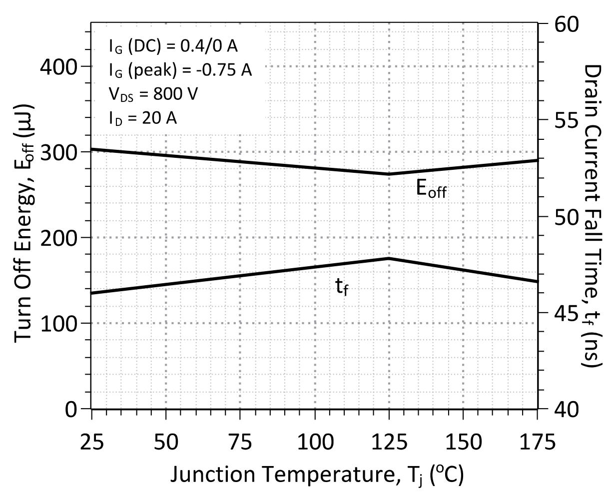


Figure 12: Typical Turn Off Energy Losses and Switching Times vs. Temperature

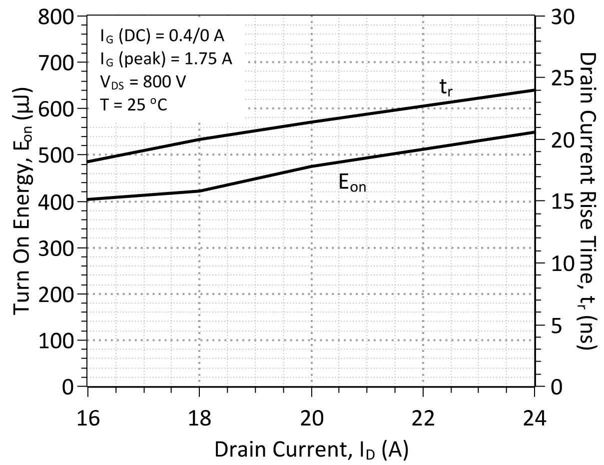


Figure 13: Typical Turn On Energy Losses vs. Drain Current

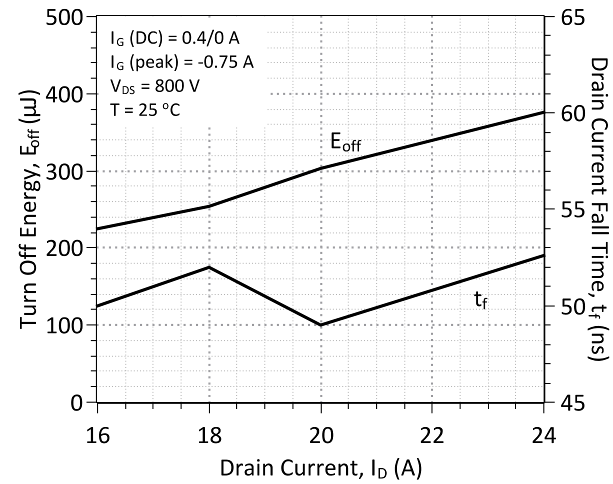


Figure 14: Typical Turn Off Energy Losses vs. Drain Current

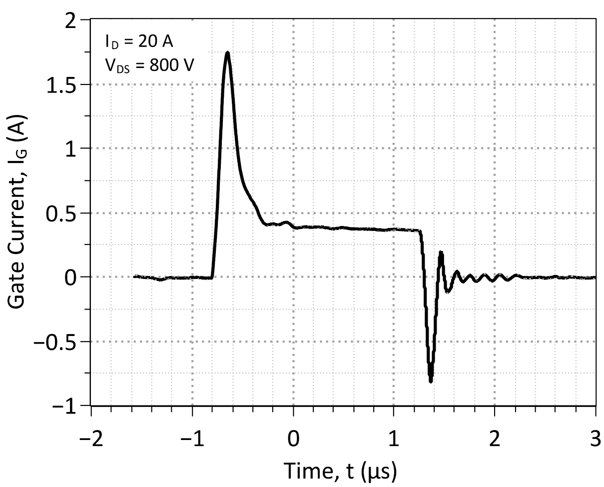


Figure 15: Typical Gate Current Waveform

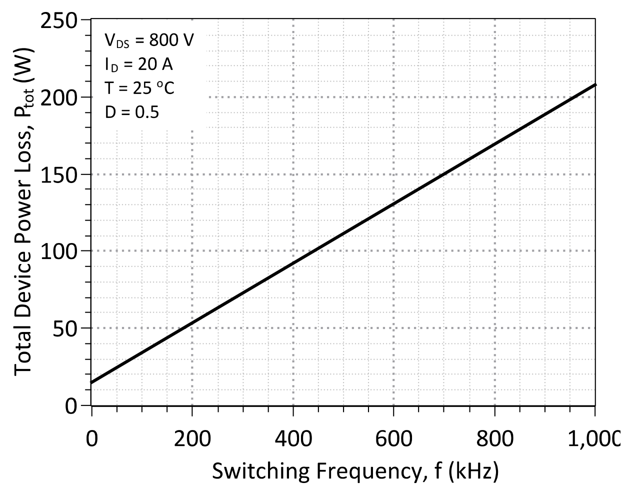


Figure 16: Typical Hard Switched Device Power Loss vs. Switching Frequency [2]

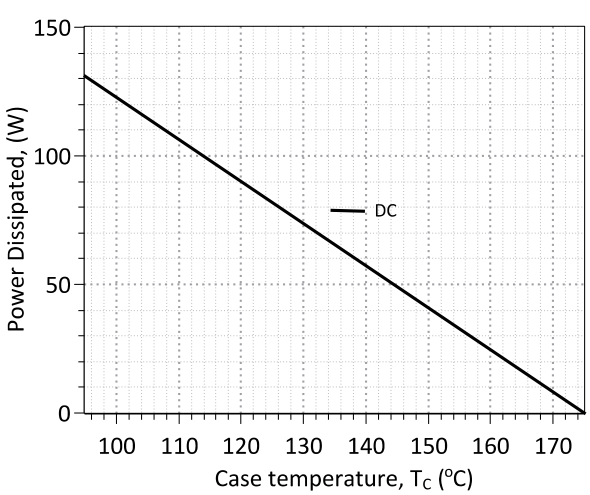


Figure 17: Power Derating Curve

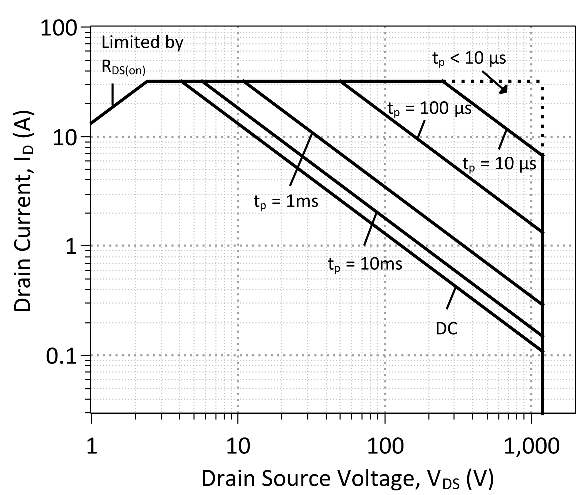


Figure 18: Forward Bias Safe Operating Area at T_c = 95 °C

[2] – Representative values based on device switching energy loss. Actual losses will depend on gate drive conditions, device load, and circuit topology.

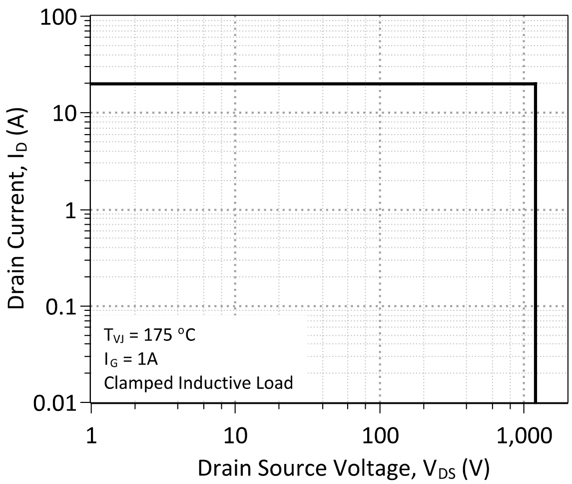


Figure 19: Turn-Off Safe Operating Area

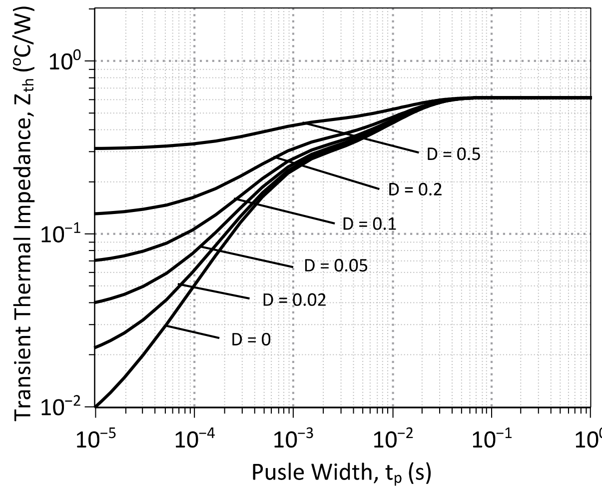


Figure 20: Transient Thermal Impedance (SiC Junction Transistor)

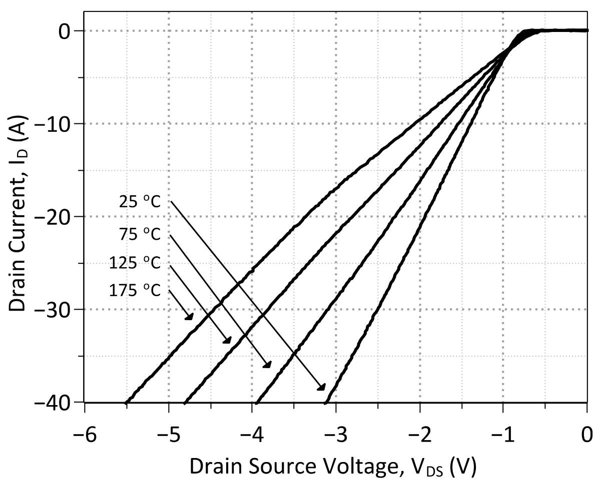


Figure 21: Typical SiC FWD Forward Characteristics

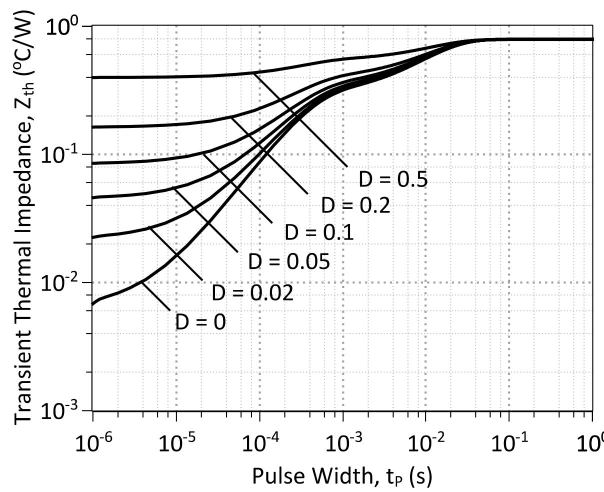


Fig. 22: Transient Thermal Impedance Characteristics (FWD)

Gate Drive Theory of Operation for the GA20SICP12-263

The SJT transistor is a current controlled transistor which requires a positive gate current for turn-on as well as to remain in on-state. An ideal gate current waveform for ultra-fast switching of the SJT, while maintaining low gate drive losses, is shown in Figure 23.

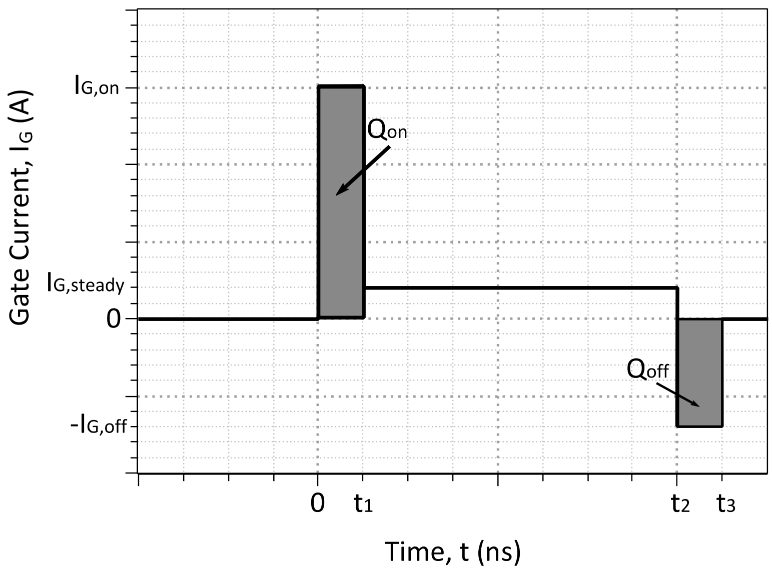


Figure 23: Idealized Gate Current Waveform

Gate Currents, $I_{G,pk}$/-$I_{G,pk}$ and Voltages during Turn-On and Turn-Off

An SJT is rapidly switched from its blocking state to on-state, when the necessary gate charge, Q_G, for turn-on is supplied by a burst of high gate current, $I_{G,on}$, until the gate-source capacitance, C_{GS}, and gate-drain capacitance, C_{GD}, are fully charged.

$$I_{G,on} * t_1 \geq Q_{gs} + Q_{gd}$$

The $I_{G,pon}$ pulse should ideally terminate, when the drain voltage falls to its on-state value, in order to avoid unnecessary drive losses during the steady on-state. In practice, the rise time of the $I_{G,on}$ pulse is affected by the parasitic inductances, L_{par} in the module and drive circuit. A voltage developed across the parasitic inductance in the source path, L_s, can de-bias the gate-source junction, when high drain currents begin to flow through the device. The applied gate voltage should be maintained high enough, above the $V_{GS,ON}$ level to counter these effects.

A high negative peak current, -$I_{G,off}$ is recommended at the start of the turn-off transition, in order to rapidly sweep out the injected carriers from the gate, and achieve rapid turn-off. While satisfactory turn off can be achieved with V_{GS} = 0 V, a negative gate voltage V_{GS} may be used in order to speed up the turn-off transition.

Steady On-State

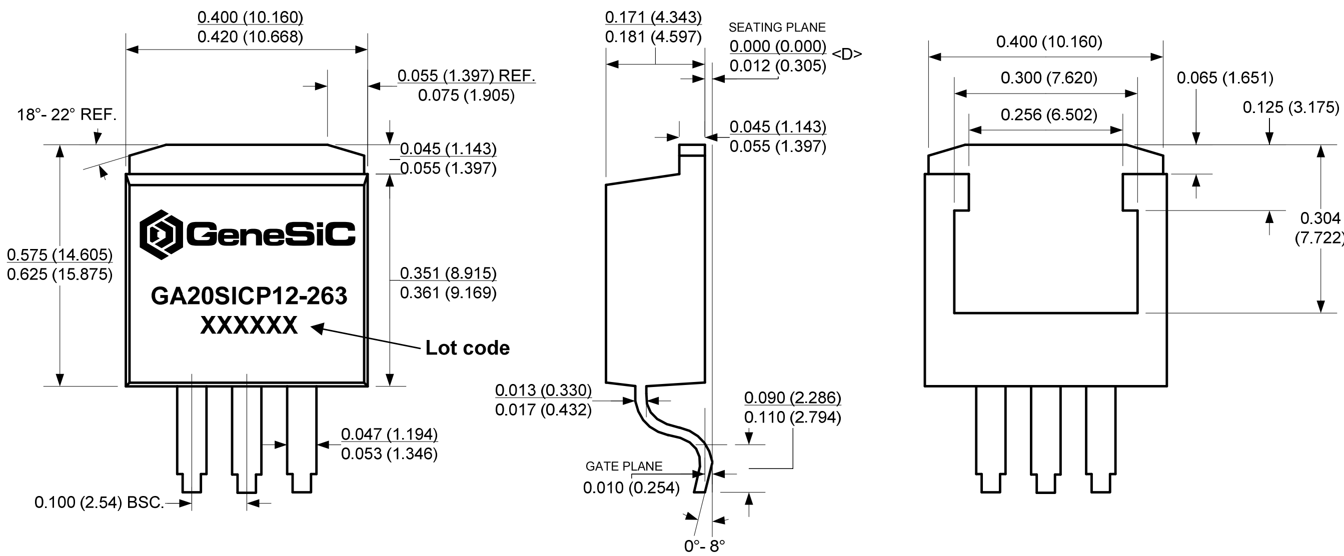
After the device is turned on, I_G may be advantageously lowered to $I_{G,steady}$ for reducing unnecessary gate drive losses. The $I_{G,steady}$ is determined by noting the DC current gain, h_{FE}, of the device

The desired $I_{G,steady}$ is determined by the peak device junction temperature T_J during operation, drain current I_D, DC current gain h_{FE}, and a 50 % safety margin to ensure operating the device in the saturation region with low on-state voltage drop by the equation:

$$I_{G,steady} \approx \frac{I_D}{h_{FE}(T, I_D)} * 1.5$$

Package Dimensions:

TO-263 **PACKAGE OUTLINE**



NOTE
1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

Revision History			
Date	Revision	Comments	Supersedes
2014/08/25	2	Gate Drive Theory Update	
2014/06/23	1	Updated Characteristics	
2013/12/11	0	Initial release	

Published by
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Dulles, VA 20166

SPICE Model Parameters

This is a secure document. Please copy this code from the SPICE model PDF file on our website (http://www.genesicsemi.com/images/products_sic/igbt_copack/GA20SICP12-263_spice.pdf) into LTSPICE (version 4) software for simulation of the GA20SICP12-263.

```
*     MODEL OF GeneSiC Semiconductor Inc.
*
*     $Revision:   1.2           $
*     $Date:   23-JUN-2014       $
*
*     GeneSiC Semiconductor Inc.
*     43670 Trade Center Place Ste. 155
*     Dulles, VA 20166
*
*     COPYRIGHT (C) 2014 GeneSiC Semiconductor Inc.
*     ALL RIGHTS RESERVED
*
* These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
* OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
* TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
* PARTICULAR PURPOSE."
* Models accurate up to 2 times rated drain current.
*
* Start of GA20SICP12-263 SPICE Model
*
.SUBCKT GA20SIPC12 DRAIN GATE SOURCE
Q1 DRAIN GATE SOURCE GA20SIPC12_Q
D1 SOURCE DRAIN GA20SIPC12_D1
D2 SOURCE DRAIN GA20SIPC12_D2
*
.model GA20SIPC12_Q NPN
+ IS        5.00E-47         ISE        1.26E-28        EG          3.23
+ BF        65               BR         0.55            IKF         700
+ NF        1                NE         2               RB          2.60
+ RC        0.045            TRC1       8.50E-03        RE          0.01
+ XTB       -1.2             CJC        6.98E-10        VJC         3
+ MJC       0.5              CJE        2.22E-09        VJE         3
+ MJE       0.5              XTI        3               MFG    GeneSiC_Semi
.MODEL GA20SIPC12_D1 D
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+ IKF       1000             EG         1.2             XTI         -2
+ TRS1      0.008            TRS2       2.71739E-05     CJO         6.40E-10
+ VJ        0.469            M          1.508           FC          0.5
+ TT        1.00E-10
.MODEL GA20SIPC12_D2 D
+ IS        1.54E-22         RS         0.19            TRS1        -0.004
+ N         3.941            EG         3.23            IKF         19
+ XTI       0                FC         0.5             TT     0
.ENDS
* End of GA20SICP12-263 SPICE Model
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