FUJITSU
MICROELECTRONICS, INC.

MB8464

MB8464
MB8464-L

PRELIMINARY

Note: This is not a final specification.
Some parametric limits are subject to change.

CMOS 65,536-BIT STATIC RANDOM ACCESS MEMORY

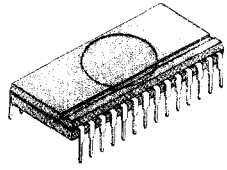
8464LCC

DESCRIPTION

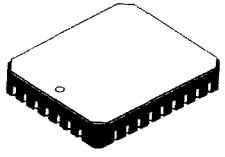
The Fujitsu MB8464 is a 8192 word by 8-bit static random access memory. This device is fabricated using a combination of Fujitsu's high-speed N-Channel MOS silicon-gate technology and the low power consumptive complementary MOS silicon-gate technology.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All inputs and output pins are TTL compatible, and a single +5V power supply is used. It is possible to retain data at low power supply voltage.

The MB8464 can be used for high performance applications such as microcomputer systems where fast access times and ease of use are required. Output Enable $\overline{G}$ input permits the disable of all outputs when outputs are OR-tied. The MB8464 is packaged in an industry standard 28-pin dual in-line package and is also available in a 32-pin leadless chip carrier.



PLASTIC PACKAGE
DIP-28P-M02

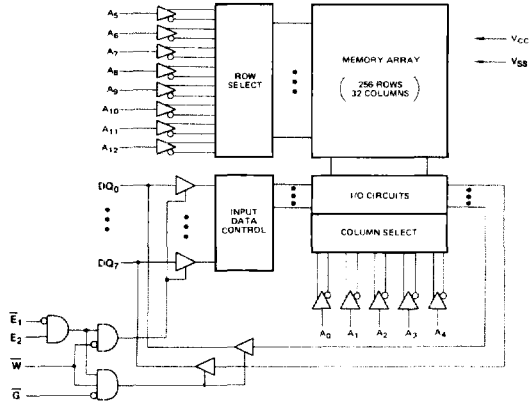


LEADLESS CHIP CARRIER
LCC-32C-A02

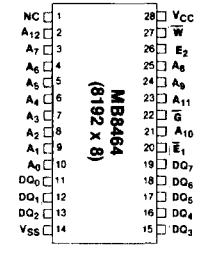
FEATURES

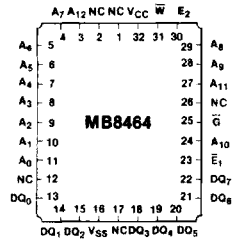
- **Organized as 8192 words by 8-bits**
- **Fast access times:**
  MB8464-12/-12L: 120 ns Max.,
  MB8464-15/-15L: 150 ns Max.
- **Low Power Consumption:**
  MB8464-12/-15: 500 mW Max. (Active)
  MB8464-12L/-15L: 330 mW Max. (Active)
  MB8464-12/-15: 11 mW Max. (Standby)
  MB8464-12L/-15L: 0.55 mW Max.(Standby)
- **Completely static operation: no clock or refresh needed**
- **Single +5V supply voltage, ±10% tolerance**
- **Common data inputs and outputs**
- **TTL compatible inputs and outputs**
- **Low data retention voltage: 2.0V min.**
- **Standard 28-pin DIP and 32-pin leadless chip carrier**

MB8464 BLOCK DIAGRAM



PIN ASSIGNMENTS





TRUTH TABLE

$\overline{E}_1$	E_2	$\overline{G}$	$\overline{W}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	Not Selected	I_{SB}	High-Z
X	L	X	X	Not Selected	I_{SB}	High-Z
L	H	H	H	D_{OUT} Disable	I_{CC}	High-Z
L	H	L	H	Read	I_{CC}	D_{OUT}
L	H	X	L	Write	I_{CC}	D_{IN}

8464LCC

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Storage Temperature	Cerdip	T_{stg}	−65 to +150	°C
	Plastic		−40 to +125	°C
Temperature Under Bias		T_{bias}	−10 to +85	°C
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage		V_{IN}	−0.5 to V_{CC} + 0.5	V
Output Voltage		$V_{I/O}$	−0.5 to V_{CC} + 0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the *operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields.* However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to 70°C
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}**	−0.3	—	0.8	V	

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Min	Max	Unit	Condition
Input Capacitance	C_{IN}	—	7	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (V_{IN} = V_{SS} to V_{CC})		I_{LI}	—	±10	μA
Output Leakage Current ($\overline{E}_1$ = V_{IH} OR E_2 = V_{IL} OR $\overline{G}$ = V_{IH} OR $\overline{W}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC})		I_{LO}	—	±10	μA
Standby Power Supply Current ($-0.2V \le E_2 \le 0.2V$ OR $V_{CC}-0.2V \le \overline{E}_1 \le V_{CC}+0.2V$ $V_{CC}-0.2V \le E_2 \le V_{CC}+0.2V$)	Standard	I_{SB1}	—	2	mA
	L-Version		—	0.1	mA
Standby Power Supply Current ($\overline{E}_1$ = V_{IH} OR E_2 = V_{IL})	Standard	I_{SB2}	—	5	mA
	L-Version		—	3	mA
Active Power Supply Current ($\overline{E}_1$ = V_{IL}, E_2 = V_{IH} V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0)	Standard	I_{CC1}	—	30	mA
	L-Version		—	25	mA
Active Power Supply Current (Cycle = Min., Duty = 100% I_{OUT} = 0)	Standard	I_{CC2}	—	90	mA
	L-Version		—	60	mA
Output High Voltage (I_{OH} = −1.0mA)		V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 2.1mA)		V_{OL}	—	0.4	V

****V_{IL}(min) = −0.3V for DC level, V_{IL}(min) = −3.0V, for ≤50 nsec pulse.**

AC TEST CONDITIONS

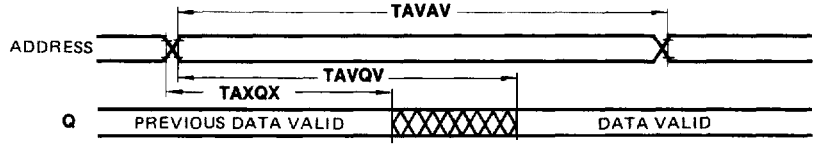
Input Pulse Levels:	**0.6V to 2.4 V**
Input Pulse Rise and Fall Times:	**5 ns**
Timing Reference Level:	**Input = 0.8 V, 2.2 V**
	Output = 0.8V, 2.0 V
Output Load:	**1 TTL gate + 5pF (including scope & jig) for TGHQZ, TWLQZ, TEHQZ, TWHQX, TGLQX and TEHQX**
	1 TTL gate + 100pF for all others.

AC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

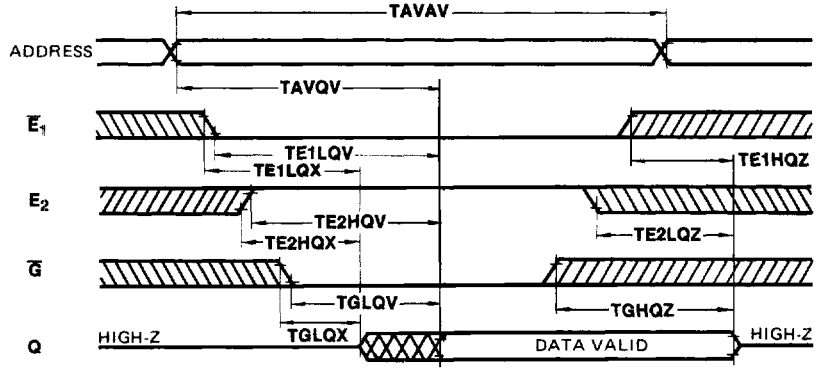
READ CYCLE

Parameter	Symbol	MB8464-12/12L		MB8464-15/15L		Unit
		Min	Max	Min	Max	
Read Cycle Time	TAVAV	120		150		ns
Address Access Time	TAVQV		120		150	ns
$\overline{E}_1$ Access Time	TE1LQV		120		150	ns
E_2 Access Time	TE2HQV		120		150	ns
Output Enable to Output Valid	TGLQV		50		60	ns
Output Hold from Address Change	TAXQX	10		10		ns
Chip Enable to Output Low-Z	TE1LQX, TE2HQX	10		10		ns
Output Enable to Output Low-Z	TGLQX	5		5		ns
Chip Enable to Output High-Z	TE1HQZ, TE2HQZ		40		50	ns
Output Enable to Output High-Z	TGHQZ		40		50	ns

READ CYCLE No. 1[1) 2)]



READ CYCLE No. 2[1)]



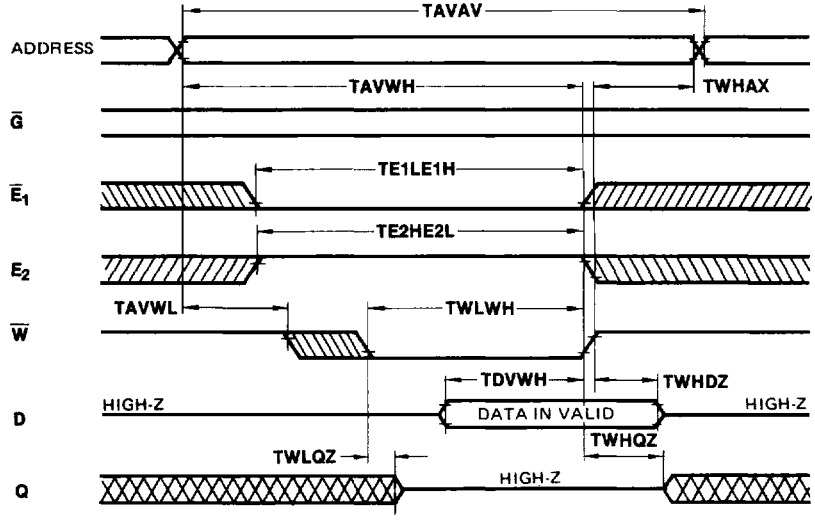
Note: 1) $\overline{W}$ is high for Read Cycle.
2) Device is continuosly selected, $\overline{E}_1 = \overline{G} = V_{IL}$, $E_2 = V_{IH}$.

WRITE CYCLE

Parameter	Symbol	MB8464-12/12L		MB8464-15/15L		Unit
		Min	Max	Min	Max	
Write Cycle Time	TAVAV	120		150		ns
Address Valid to End of Write	TAVWH, TAVE1H, TAVE2L	85	—	100	—	ns
Chip Enable to End of Write	TE1LE1H, TE2HE2L	85	—	100	—	ns
Data Valid to End of Write	TDVWH, TDVE1H, TDVE2L	40	—	50	—	ns
Data Hold Time	TWHDZ, TE1HDZ, TE2LDZ	0	—	0	—	ns
Write Pulse Width	TWLWH	70	—	90	—	ns
Address Setup Time	TAVWL, TAVE1L, TAVE2H	0	—	0	—	ns
Write Recovery Time	TWHAX, TE1HAX, TE2LAX	5	—	5	—	ns
Chip Enable to Output Low-Z	TE1LQX, TE2HQX	5	—	5	—	ns
Write Enable to Output Low-Z	TWHQX	5	—	5	—	ns
Write Enable to Output High-Z	TWLQZ	—	40	—	50	ns

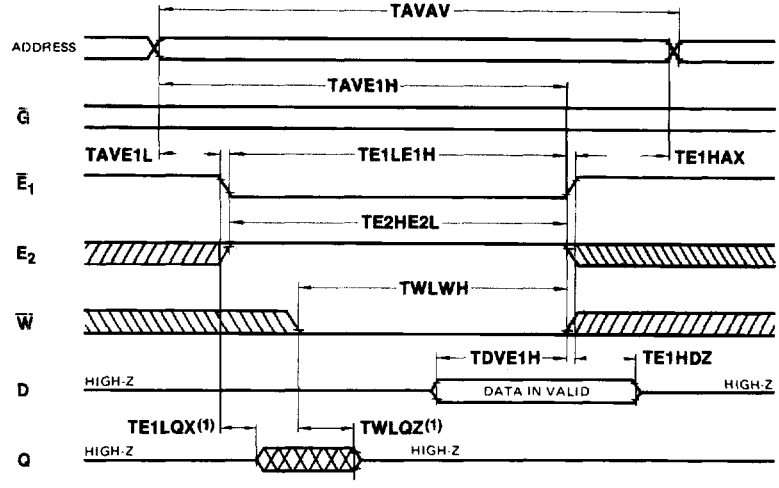
WRITE CYCLE TIMING DIAGRAMS

WRITE CYCLE NO. 1 ($\overline{W}$ Controlled)

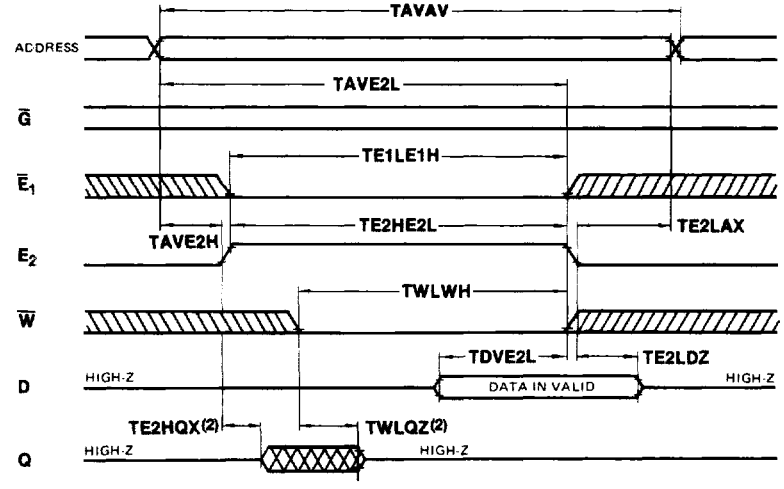


Note: 1) IF $\overline{G}$, $\overline{E}_1$, and E_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

WRITE CYCLE NO. 2 ($\overline{E}_1$ Controlled)



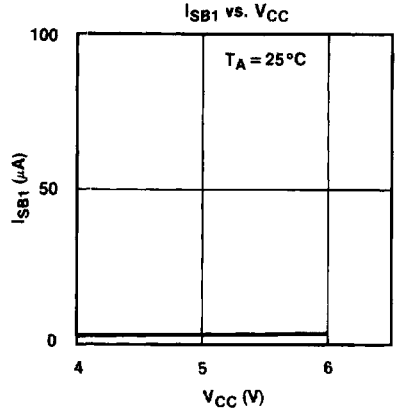
WRITE CYCLE NO. 3 (E_2 Controlled)

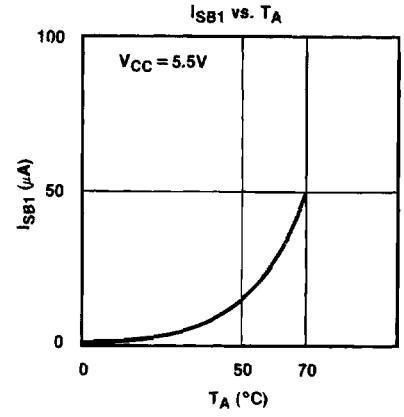


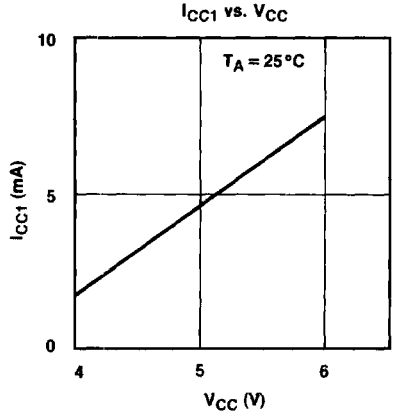
Note: 1) If $\overline{G}$, E_2 and $\overline{W}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

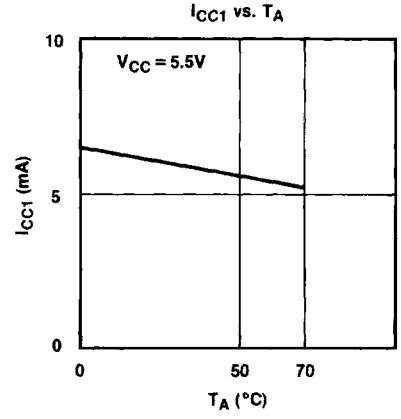
2) If $\overline{G}$, $\overline{E}_1$ and $\overline{W}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

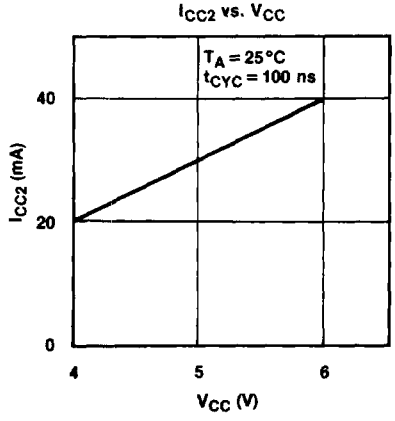
TYPICAL CHARACTERISTICS CURVES

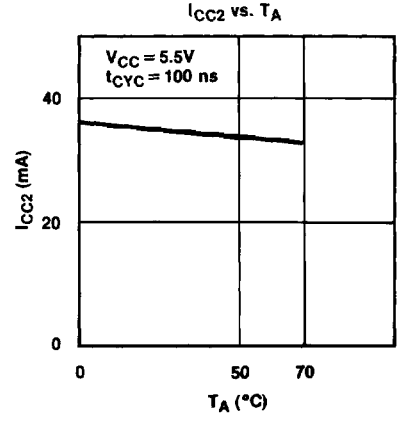












DATA RETENTION CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Notes		Symbol	Min	Max	Unit
Data Retention Supply Voltage	1		VDR	2.0	5.5	V
Data Retention Supply Current	2	L-Version	IDR	—	0.1	mA
		Standard			50	μA
Data Retention Set Up Time	3		TE2LVL, TE1HVL	0		ns
Recovery Time	3		TVHE1L, TVHE2H	TAVAV		ns

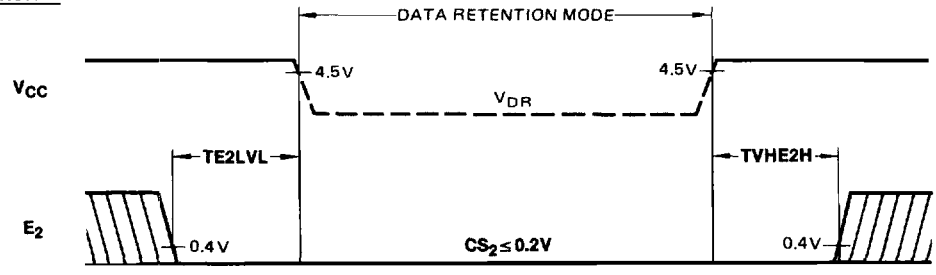
Note 1: E_2 controlled: $E_2 \leq 0.2V$
E_1 controlled: $E_1 \geq V_{DR} - 0.2V$ ($E_2 \leq 0.2V$ or $E_2 \geq V_{DR} - 0.2V$)

Note 2: E_2 controlled: $V_{DR} = 3.0V$, $E_2 \leq 0.2V$
E_1 controlled: $V_{DR} = 3.0V$, $E_1 \geq V_{DR} - 0.2V$ ($E_2 \leq 0.2V$ or $E_2 \geq V_{DR} - 0.2V$)

Note 3: $V_L = 4.5V$ on falling transition, $V_H = 4.5V$ on rising transition.

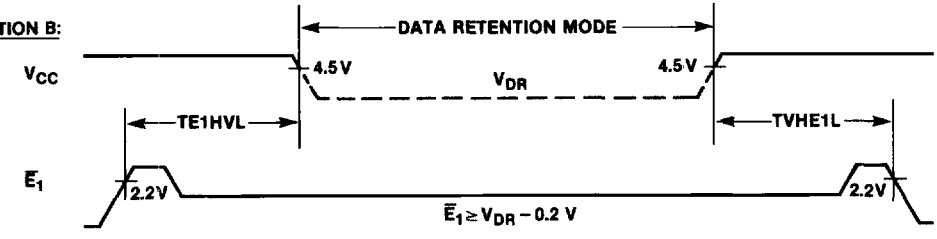
DATA RETENTION TIMING

CONDITION A:



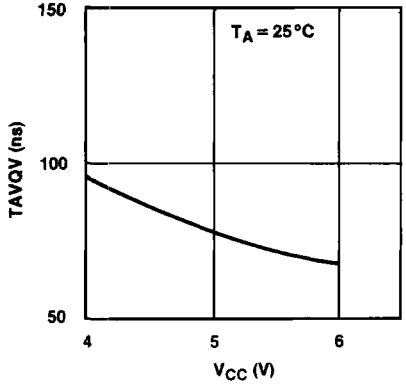
OR

CONDITION B:

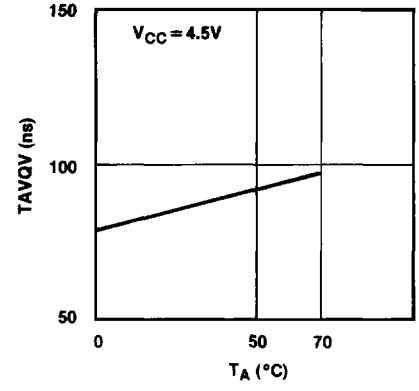


TYPICAL CHARACTERISTICS CURVES (Continued)

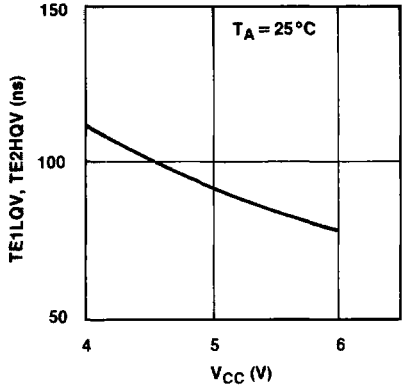
I_{SB1} vs. T_A



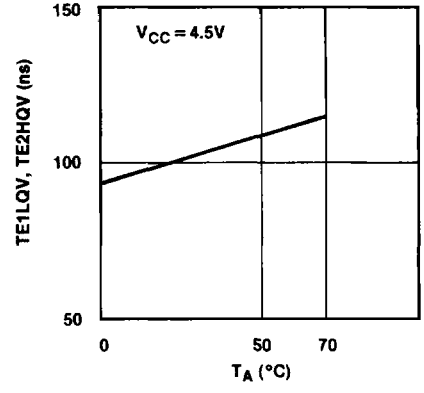
t_{AA} vs. T_A



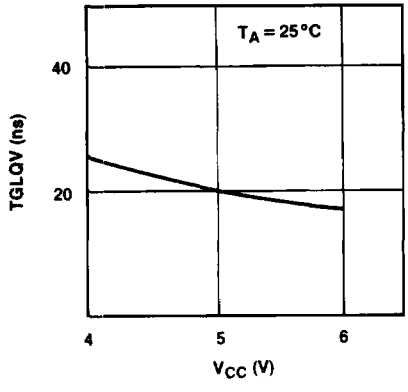
TE1LQV, TE2HQV vs. V_{CC}



TE1LQV, TE2HQV vs. T_A



TGLQV vs. V_{CC}



TGLQV vs. T_A