FUJITSU
MICROELECTRONICS, INC.

MB8265

MB8265-15
MB8265-20

NMOS 65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

8265LCC

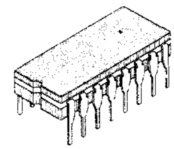
DESCRIPTION

The Fujitsu MB8265 is a fully decoded, dynamic NMOS random access memory organized as 65536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

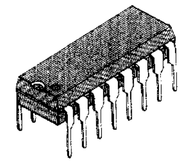
Multiplexed row and column address inputs permit the MB8265 to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out.

The MB8265 is fabricated using silicon gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.



CERAMIC PACKAGE
CERDIP
DIP-16C-C04



PLASTIC PACKAGE
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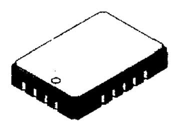
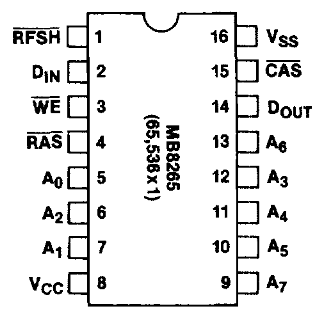


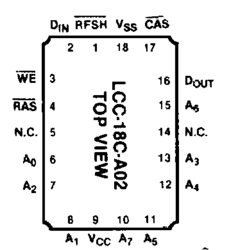
CERAMIC LCC
LCC-18C-A02

FEATURES

- **65,536 x 1 RAM, 16 pin package**
- **Silicon-gate, Double Poly NMOS, single transistor cell**
- **Row access time:**
  - **150ns Max (MB8265-15)**
  - **200ns Max (MB8265-20)**
- **Cycle time:**
  - **270ns Min (MB8265-15)**
  - **330ns Min (MB8265-20)**
- **Low power:**
  - **275 mW Active, (MB8265-15)**
  - **248 mW Active, (MB8265-20)**
  - **28 mW Standby (Max)**
- **+5V Supply, ±10% tolerance**
- **On chip substrate bias generator for high performance**
- **Three-state TTL compatible output**
- **All inputs TTL compatible, low capacitive load**
- **"Gated" $\overline{CAS}$**
- **128 refresh cycles**
- **Pin 1 Refresh capability**
- **Common I/O capability using "Early Write" operation**
- **Output unlatched at cycle end allows extended page boundary and two-dimensional chip select**
- **Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability**
- **On-chip latches for Addresses and Data-in**
- **Offers two variations of hidden refresh**

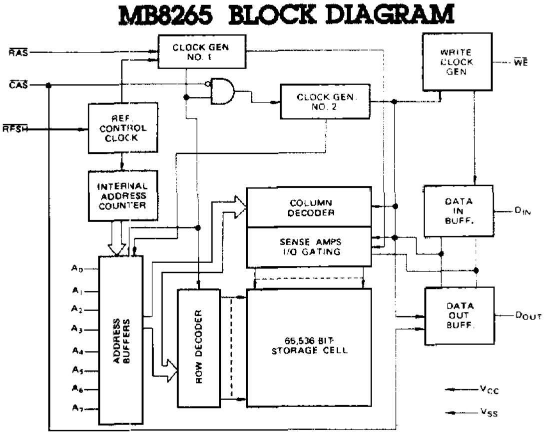
PIN ASSIGNMENTS





8265LCC

MB8265 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7.0	V
Storage Temperature	Cerdip	T_{stg}	−55 to +150	°C
	Plastic		−55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance $A_0 \sim A_7$, D_{IN}	C_{IN1}	—	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{RFSH}$	C_{IN2}	—	—	8	pF
Output Capacitance D_{OUT}	C_{OUT}	—	—	7	pF

STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB8265-20	I_{CC1}		45	mA
	MB8265-15		—	50	mA
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{RFSH}$ = V_{IH})		I_{CC2}	—	5	mA
REFRESH CURRENT 1 Average power current ($\overline{RAS}$ cycling $\overline{CAS}$ = $\overline{RFSH}$ = V_{IH}; t_{RC} = min)	MB8265-20	I_{CC3}	—	36	mA
	MB8265-15			42	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = min)		I_{CC4}	—	34	mA
REFRESH CURRENT 2 Average power supply current ($\overline{RFSH}$ cycling; $\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, t_{FC} = min)		I_{CC5}	—	46	mA
INPUT LEAKAGE CURRENT Input leakage current, any input ($0V \leq V_{IN} \leq 5.5V$) Input pins not under test = 0V, V_{CC} = 5.5V, V_{SS} = 0V		I_{IL}	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)		I_{OL}	−10	10	μA
OUTPUT LEVEL Output low voltage (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V
OUTPUT LEVEL Output high voltage (I_{OH} = −5mA)		V_{OH}	2.4	—	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

R45

DYNAMIC CHARACTERISTICS Notes [1, 2, 3]

(Recommended operating conditions unless otherwise noted.)

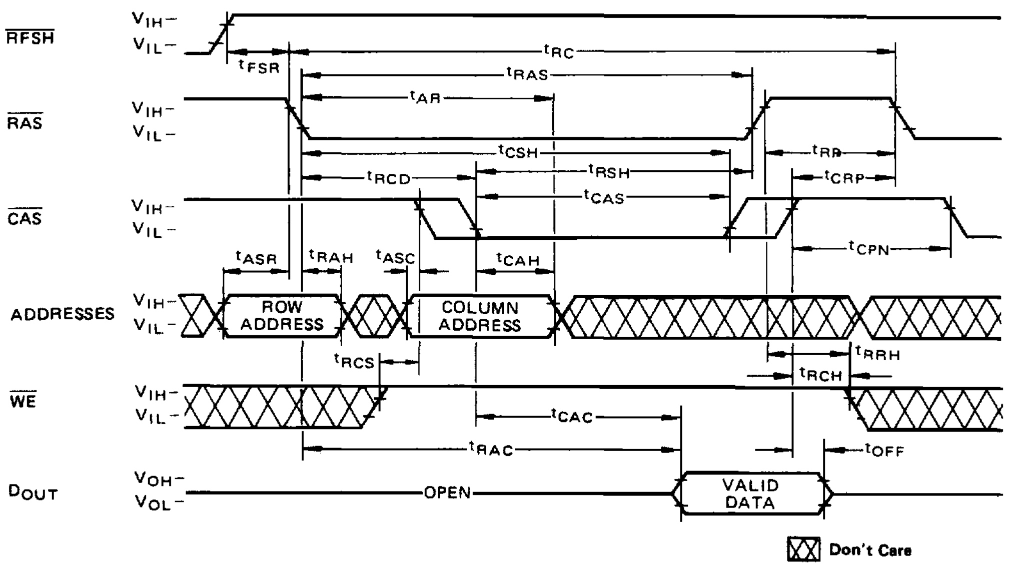
Parameter	Notes	Symbol	MB8265-20 Min	MB8265-20 Typ	MB8265-20 Max	MB8265-15 Min	MB8265-15 Typ	MB8265-15 Max	Unit
Time between Refresh		t_{REF}	—	—	2	—	—	2	ms
Random Read/Write Cycle Time		t_{RC}	330	—	—	270	—	—	ns
Read-Write Cycle Time		t_{RWC}	375	—	—	300	—	—	ns
Page Mode Cycle Time		t_{PC}	225	—	—	170	—	—	ns
Access Time from $\overline{RAS}$	[4] [6]	t_{RAC}	—	—	200	—	—	150	ns
Access Time from $\overline{CAS}$	[5] [6]	t_{CAC}	—	—	135	—	—	100	ns
Output Buffer Turn Off Delay		t_{OFF}	0	—	50	0	—	40	ns
Transition Time		t_T	3	—	50	3	—	35	ns
$\overline{RAS}$ Precharge Time		t_{RP}	120	—	—	100	—	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	200	—	10000	150	—	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	135	—	—	100	—	—	ns
$\overline{CAS}$ Precharge Time (Page Mode Only)		t_{CP}	80	—	—	60	—	—	ns
$\overline{CAS}$ Precharge Time (All Cycles Except Page Mode)		t_{CPN}	30	—	—	25	—	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	135	—	10000	100	—	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	200	—	—	150	—	—	ns
$\overline{RAS}$ to CAS Delay Time	[7] [8]	t_{RCD}	30	—	65	25	—	50	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	—	0	—	—	ns
Row Address Set Up Time		t_{ASR}	0	—	—	0	—	—	ns
Row Address Hold Time		t_{RAH}	20	—	—	15	—	—	ns
Column Address Set Up Time		t_{ASC}	0	—	—	0	—	—	ns
Column Address Hold Time		t_{CAH}	55	—	—	45	—	—	ns
Column Address Hold Time Referenced to $\overline{RAS}$		t_{AR}	120	—	—	95	—	—	ns
Read Command Set Up Time		t_{RCS}	0	—	—	0	—	—	ns
Read Command Hold Time	[10]	t_{RCH}	0	—	—	0	—	—	ns
Write Command Set Up Time	[9]	t_{WCS}	−10	—	—	−10	—	—	ns
Write Command Hold Time		t_{WCH}	55	—	—	45	—	—	ns
Write Command Hold Time Referenced to $\overline{RAS}$		t_{WCR}	120	—	—	95	—	—	ns
Write Command Pulse Width		t_{WP}	55	—	—	45	—	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	80	—	—	60	—	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	80	—	—	60	—	—	ns
Data In Set Up Time		t_{DS}	0	—	—	0	—	—	ns
Data In Hold Time		t_{DH}	55	—	—	45	—	—	ns
Data In Hold Time Referenced to $\overline{RAS}$		t_{DHR}	120	—	—	95	—	—	ns
$\overline{CAS}$ to $\overline{WE}$ Delay	[9]	t_{CWD}	95	—	—	70	—	—	ns
$\overline{RAS}$ to $\overline{WE}$ Delay	[9]	t_{RWD}	160	—	—	120	—	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$	[10]	t_{RRH}	25	—	—	20	—	—	ns
$\overline{RFSH}$ Set Up Time Referenced to $\overline{RAS}$		t_{FSR}	120	—	—	100	—	—	ns
$\overline{RAS}$ to $\overline{RFSH}$ Delay		t_{RFD}	120	—	—	100	—	—	ns
$\overline{RFSH}$ Cycle Time		t_{FC}	330	—	—	270	—	—	ns
$\overline{RFSH}$ Pulse Width		t_{FP}	200	—	—	150	—	—	ns
$\overline{RFSH}$ Inactive Time		t_{FI}	120	—	—	100	—	—	ns
$\overline{RFSH}$ to $\overline{RAS}$ Delay	[11]	t_{FRD}	50	—	—	40	—	—	ns
$\overline{RFSH}$ Hold Time	[11]	t_{FSH}	20	—	—	15	—	—	ns
$\overline{RFSH}$ Address Set Up Time	[11]	t_{ASF}	0	—	—	0	—	—	ns
$\overline{RFSH}$ Set Up Time Referenced to $\overline{CAS}$	[11]	t_{FSC}	50	—	—	40	—	—	ns

Notes:

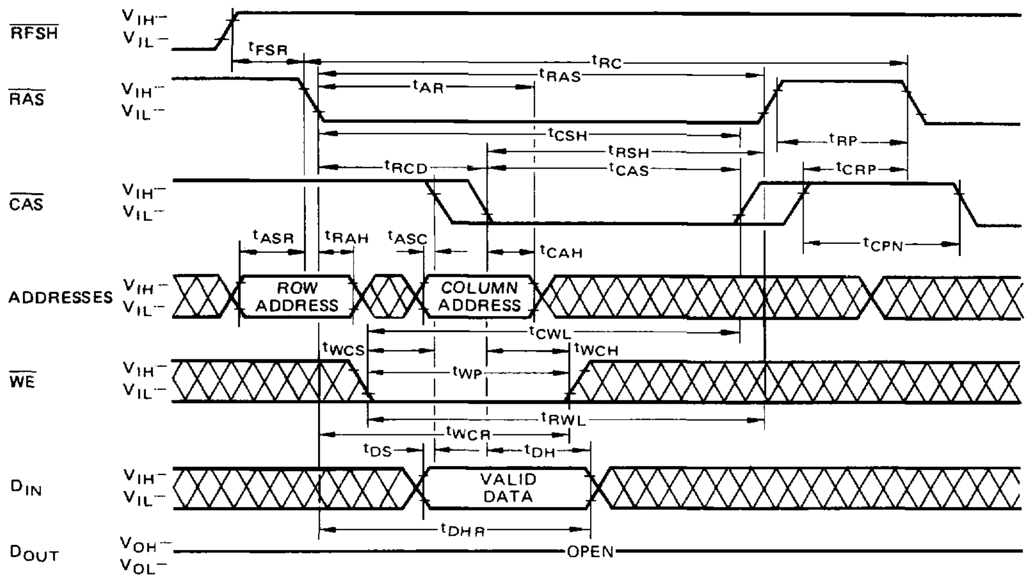
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. If internal refresh counter is to be effective, a minimum of 8 active $\overline{RFSH}$ initialization cycles required. The internal refresh counter must be activated a minimum of 128 times every 2ms if the $\overline{RFSH}$ refresh function is used. The $\overline{RFSH}$ must be held at V_{IH} if the $\overline{RFSH}$ function is not used.
2. Dynamic measurements assume t_T = 5ns.
3. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH}(min) and V_{IL}(max).
4. Assumes that $t_{RCD} \le t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \ge t_{RCD}$(max).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD}(min) = t_{RAH}(min) + $2t_T$ (t_T = 5ns) + t_{ASC}(min).
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \ge t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.
   If $t_{CWD} \ge t_{CWD}$(min) and $t_{RWD} \ge t_{RWD}$(min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. $\overline{RFSH}$ counter test read/write cycle only.

TIMING DIAGRAMS

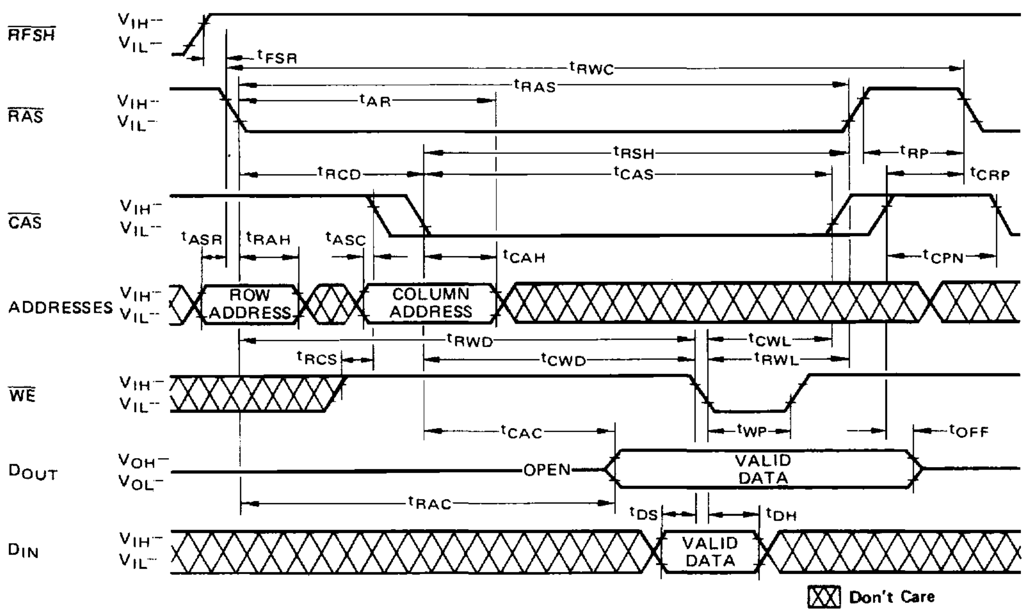
READ CYCLE



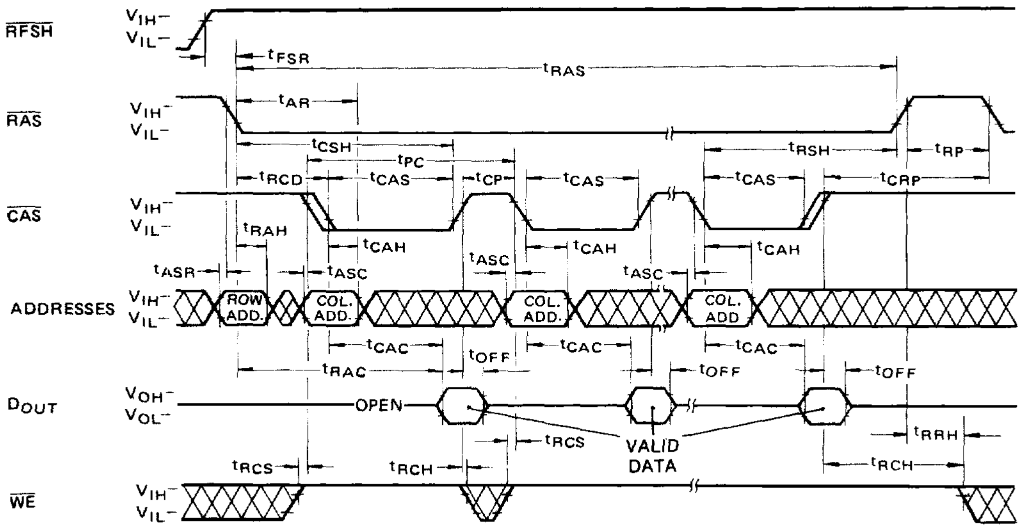
WRITE CYCLE (EARLY WRITE)



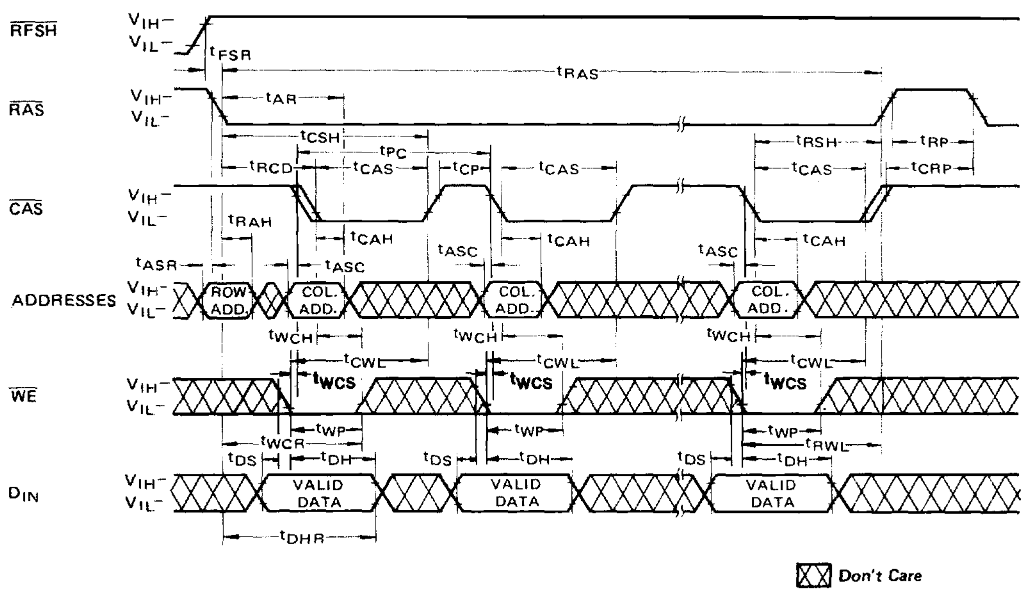
READ-WRITE / READ-MODIFY-WRITE CYCLE



PAGE-MODE READ CYCLE

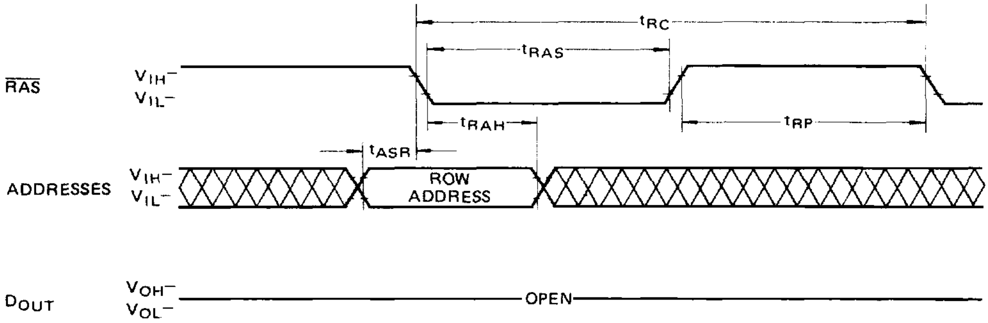


PAGE-MODE WRITE CYCLE



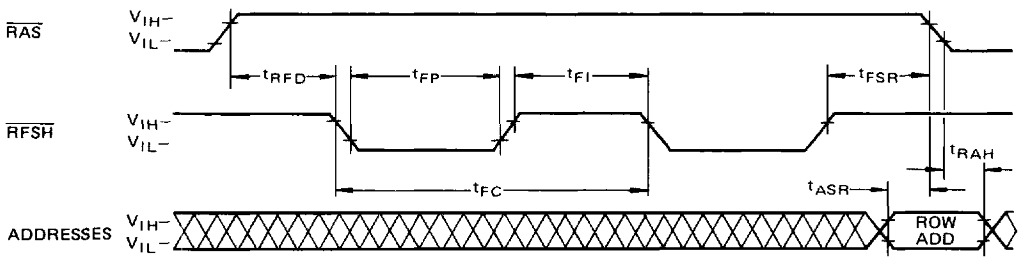
"$\overline{RAS}$-ONLY" REFRESH CYCLE

NOTE: $\overline{RFSH} = V_{IH}$, $\overline{CAS} = V_{IH}$, $\overline{WE}$ = Don't Care

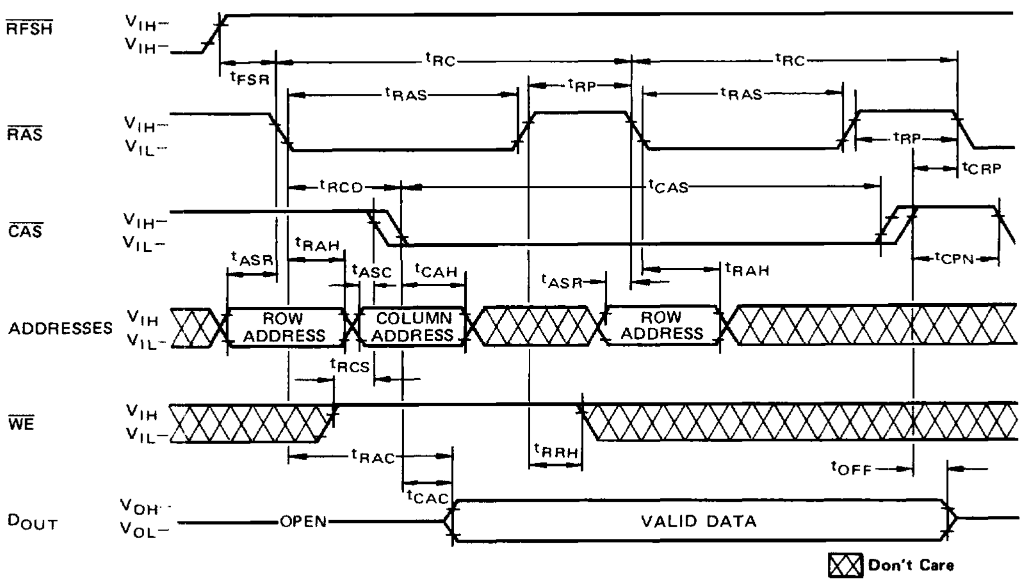


$\overline{RFSH}$ REFRESH CYCLE

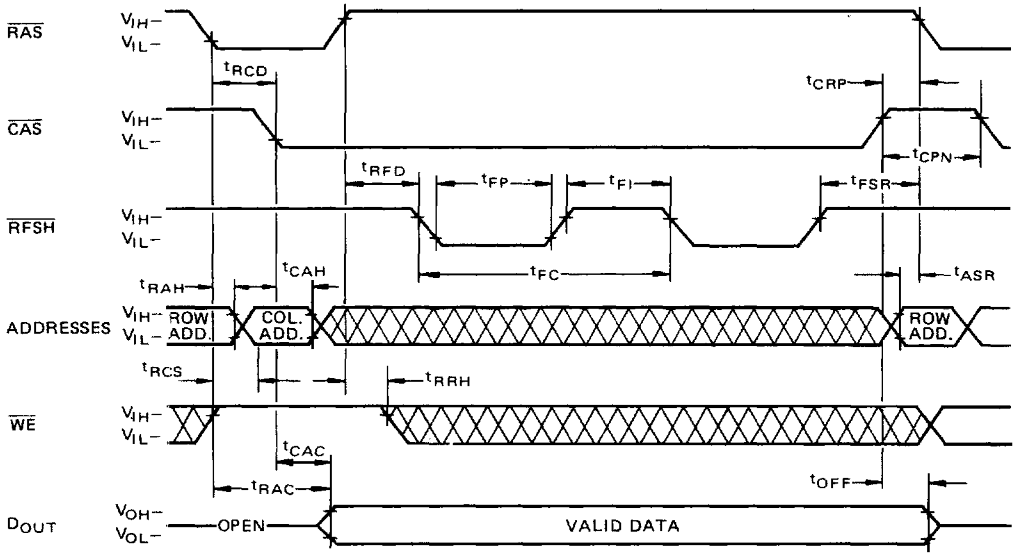
NOTE: $\overline{CAS} = V_{IH}$, $\overline{WE}$ = Don't Care



HIDDEN "$\overline{RAS}$-ONLY" REFRESH CYCLE

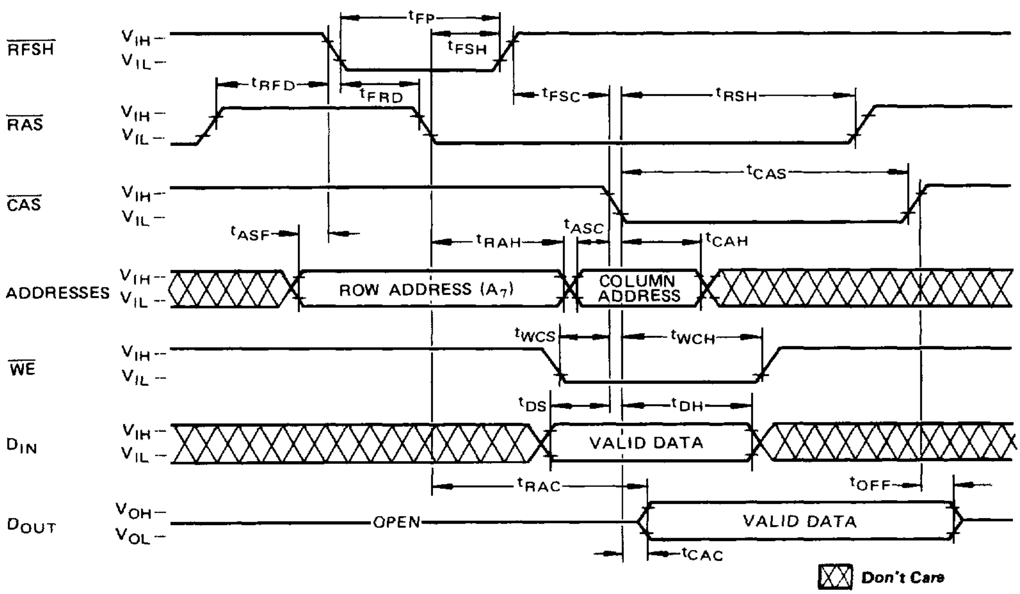


HIDDEN RFSH REFRESH CYCLE



RFSH COUNTER TEST READ/WRITE CYCLE

Note: D_{OUT} is the waveform in Read-Modify-Write Cycles



DESCRIPTION

Address Inputs

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MB8265. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{\text{RAS}}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{\text{CAS}}$). All input addresses must be stable on or before the falling edge of $\overline{\text{RAS}}$. $\overline{\text{CAS}}$ is internally inhibited (or "gated") by $\overline{\text{RAS}}$ to permit triggering of $\overline{\text{CAS}}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read mode or write mode is selected with the $\overline{\text{WE}}$ input. A logic high (1) on $\overline{\text{WE}}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input

Data written into the MB8265 during a write or read-write cycle. The last falling-edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{\text{WE}}$ is brought low (write mode) before $\overline{\text{CAS}}$, D_{IN} is strobed by $\overline{\text{CAS}}$, and the set-up and hold times are referenced to $\overline{\text{CAS}}$. In a read-write cycle, $\overline{\text{WE}}$ will be delayed until $\overline{\text{CAS}}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{\text{WE}}$, and set-up and hold times are referenced to $\overline{\text{WE}}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{\text{CAS}}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{\text{RAS}}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{\text{CAS}}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{\text{CAS}}$ is returned to ahigh level. In a write cycle the identical sequence occurs, but data is not valid.

Page-Mode

Page-mode operation permits strobing the row-address into the MB8265 while maintaining $\overline{\text{RAS}}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{\text{RAS}}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{\text{RAS}}$-Only Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{\text{RAS}}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{\text{CAS}}$ is brought low. Strobing each of 128 row-addresses with $\overline{\text{RAS}}$ will cause all bits in each row to be refreshed. Further $\overline{\text{RAS}}$-only refresh results in a substantial reduction in power dissipation.

$\overline{\text{RFSH}}$ Refresh

$\overline{\text{RFSH}}$ type refreshing available on the MB8265 offers an alternate refresh method: (1) When $\overline{\text{RFSH}}$ (pin 1) is brought low (active) during $\overline{\text{RAS}}$ (Pin 4) is high (inactive), on-chip refresh control clock generators and a refresh address counter are enabled and an internal refresh operation takes place. (2) When $\overline{\text{RFSH}}$ is brought high (inactive), the internal refresh address counter is automatically incremented in preparation for the next $\overline{\text{RFSH}}$ refresh cycle. Only $\overline{\text{RFSH}}$ activated cycles affect the internal refresh address counter.
The use of $\overline{\text{RFSH}}$ type refreshing eliminates the need of providing additional external devices to generate refresh addresses.

Hidden Refresh

Hidden Refresh Cycle may take place while maintaining latest valid data at the output by extending $\overline{\text{CAS}}$ active time from the previous memory read cycle.

The MB8265 offers two types of Hidden Refresh. They are referred to as Hidden $\overline{\text{RAS}}$-Only Refresh and Hidden $\overline{\text{RFSH}}$ Refresh.

1) Hidden $\overline{\text{RAS}}$-Only Refresh
Hidden $\overline{\text{RAS}}$-Only Refresh is performed by holding $\overline{\text{CAS}}$ at V_{IL} and taking $\overline{\text{RAS}}$ high and after a specified precharge period (t_{RP}), executing "$\overline{\text{RAS}}$-Only" refresh, but with $\overline{\text{CAS}}$ held low. $\overline{\text{RFSH}}$ has to be held at V_{IH}.

2) Hidden $\overline{\text{RFSH}}$ Refresh
Hidden $\overline{\text{RFSH}}$ Refresh is performed by holding $\overline{\text{CAS}}$ at V_{IL} and taking $\overline{\text{RAS}}$ high and after a specified precharge period (t_{RFD}), executing $\overline{\text{RFSH}}$ refresh, but with $\overline{\text{CAS}}$ held low.

A specified precharge period (t_{CPN}) is required before normal memory Read, Write or Read-Modify-Write cycle after performing either type of Hidden Refresh.

Refresh Counter Test Cycle

A special timing sequence provides a convenient method of verifying the functionality of the $\overline{\text{RFSH}}$ activated circuitry.

(A) $\overline{\text{RFSH}}$ Test Read/Write Cycle

When $\overline{\text{RFSH}}$ is given a signal in timing as shown in timing diagram of $\overline{\text{RFSH}}$ counter Test Read/Write Cycle, Read/Write Operation is enabled. A memory cell address (consisting of a row address (8 bits) and a column address (8 bits)) to be accessed can be defined as follows:

- A ROW ADDRESS — Bits $A_0 \sim A_6$ are defined when contents of the internal address counter are latched. The other bit A_7 is defined by latching a level on A_7 pin during $\overline{\text{RFSH}}$ = "L" and $\overline{\text{RAS}}$ = "H" (t_{RFD}).
- A COLUMN ADDRESS — All the bits $A_0 \sim A_7$ are defined by latching levels on $A_0 \sim A_7$ pins in a high-to-low transition of $\overline{\text{CAS}}$.

DESCRIPTION (Continued)

By using a 16-bit address latched into the on-chip address buffers by means of the above operation, any of 64K memory cells can be read/written into/from.

(B) $\overline{RFSH}$ Test Read-Modify-Write Cycle

Also, Read-Modify-Write Operation (not only the above normal Read/Write Operations) can be used in this $\overline{RFSH}$ Counter Test Cycle.

(C) Example of Refresh Counter Test Procedure

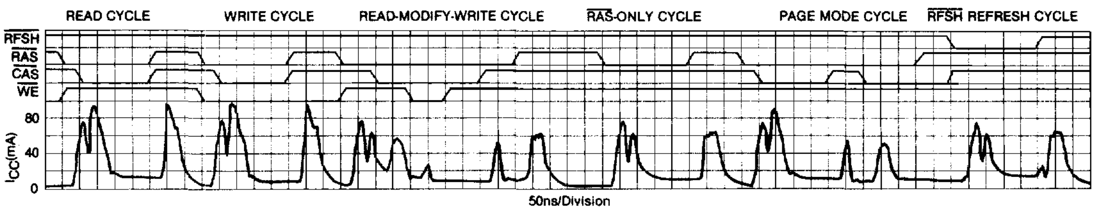
(1) Initialize the internal refresh counter. For this operation, 8 $\overline{RFSH}$ cycles are required.

(2) Write a test pattern of "0"s into the memory cells at a single column address and 128 row addresses by using 128 RFSH Test Write Cycle or RFSH Test Read-Modify-Write Cycle. (At this time, A_7 (row) must be fixed at "H" or "L".).

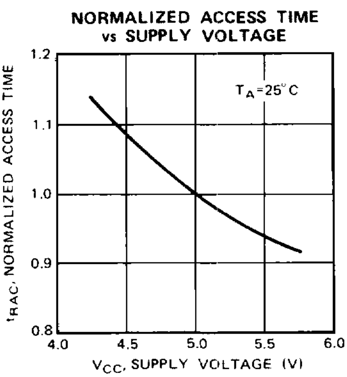
(3) Verify the data written into the memory cells in the above step (2) by using the column address used in step (2) and sequence through 128 row address combinations (A_0 ~ A_6) by means of normal Read Cycle. (At this time, A_7 (row) must be fixed at the same level as the above step (3).)

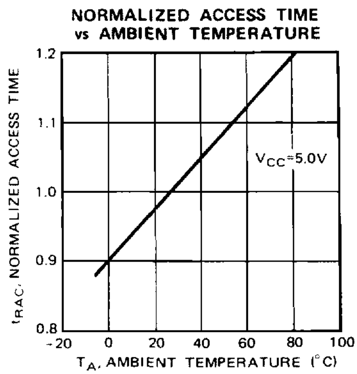
(4) Compliment the test pattern and repeat steps (2) and (3).

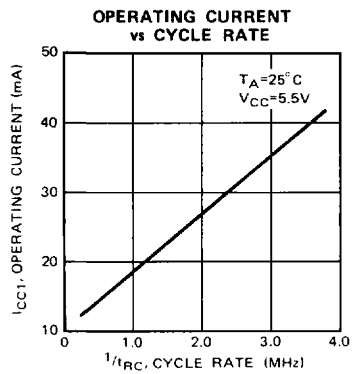
CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25 °C)



TYPICAL CHARACTERISTICS CURVES

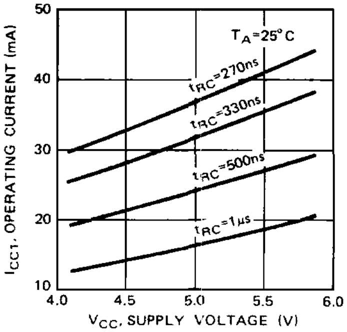




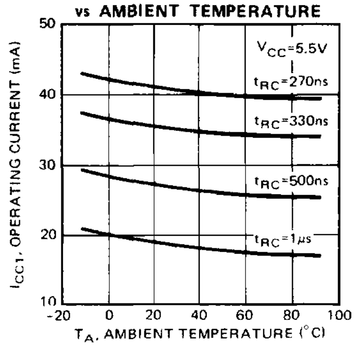


TYPICAL CHARACTERISTICS CURVES (Continued)

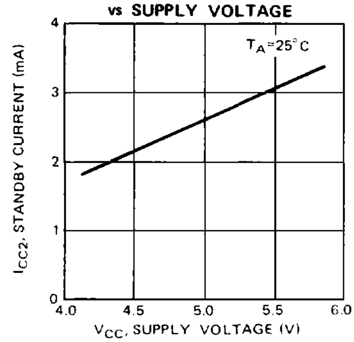
OPERATING CURRENT vs SUPPLY VOLTAGE



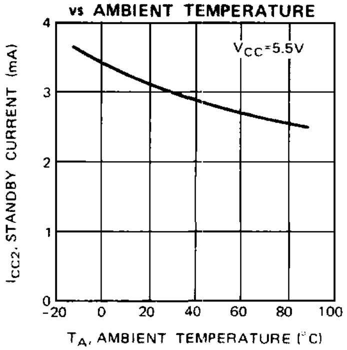
OPERATING CURRENT vs AMBIENT TEMPERATURE



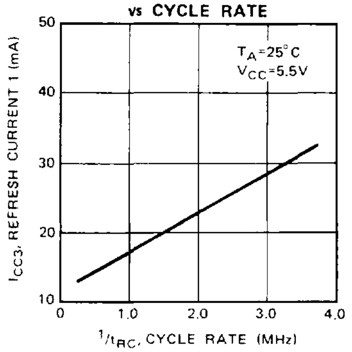
STANDBY CURRENT vs SUPPLY VOLTAGE



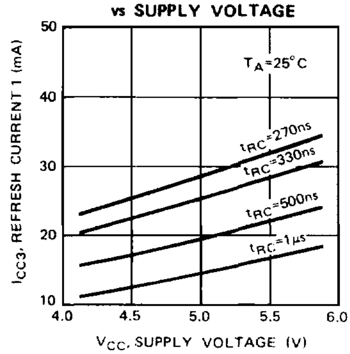
STANDBY CURRENT vs AMBIENT TEMPERATURE



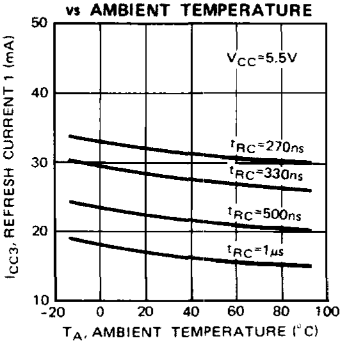
REFRESH CURRENT 1 vs CYCLE RATE



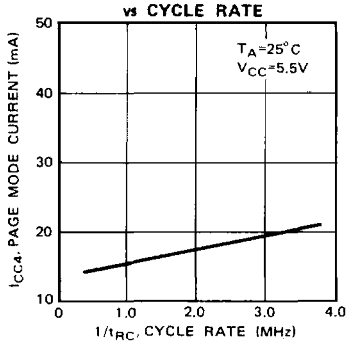
REFRESH CURRENT 1 vs SUPPLY VOLTAGE



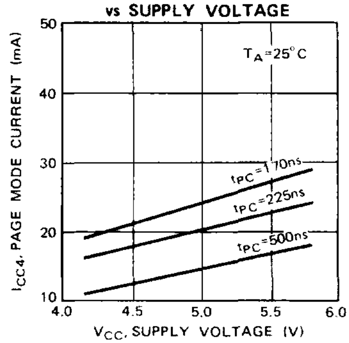
REFRESH CURRENT 1 vs AMBIENT TEMPERATURE



PAGE MODE CURRENT vs CYCLE RATE

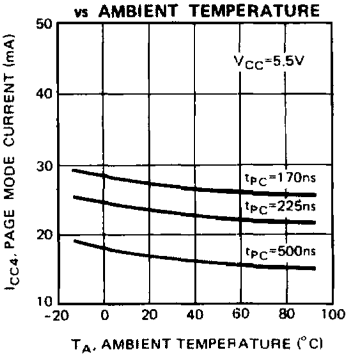


PAGE MODE CURRENT vs SUPPLY VOLTAGE

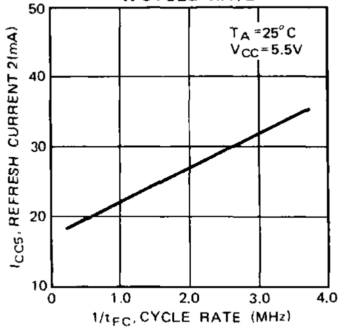


TYPICAL CHARACTERISTICS CURVES (Continued)

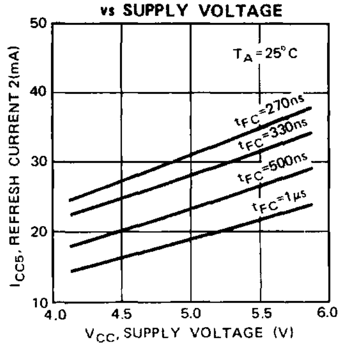
PAGE MODE CURRENT vs AMBIENT TEMPERATURE



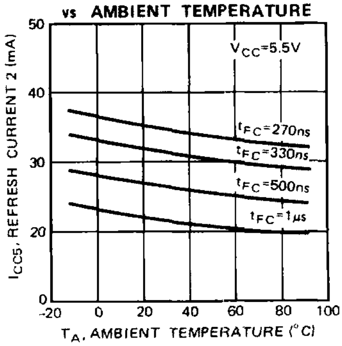
REFRESH CURRENT 2 vs CYCLE RATE



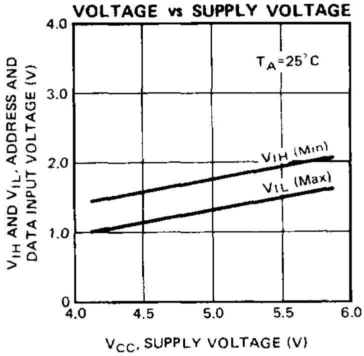
REFRESH CURRENT 2 vs SUPPLY VOLTAGE



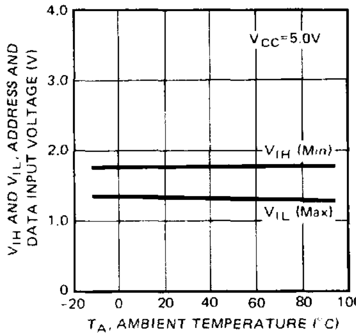
REFRESH CURRENT 2 vs AMBIENT TEMPERATURE



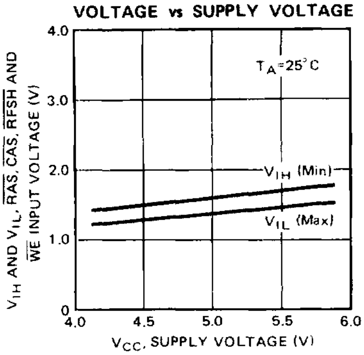
ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE



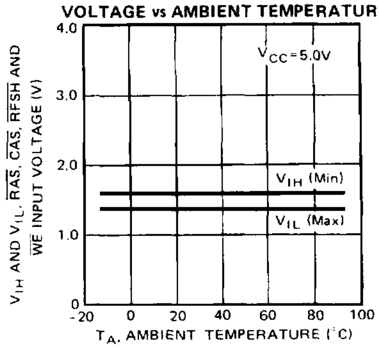
ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE



$\overline{RAS}$, $\overline{CAS}$, $\overline{RFSH}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

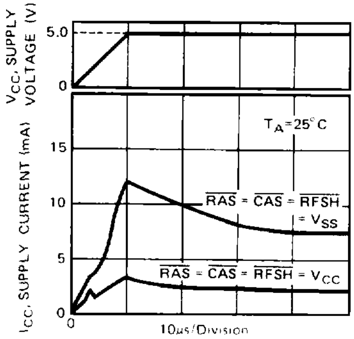


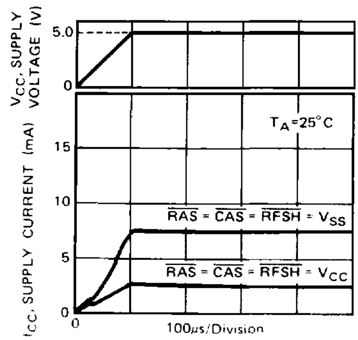
$\overline{RAS}$, $\overline{CAS}$, $\overline{RFSH}$ AND $\overline{WE}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE



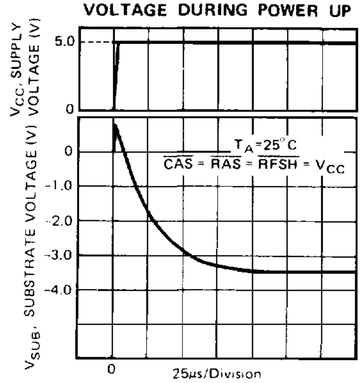
TYPICAL CHARACTERISTICS CURVES (Continued)

TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE DURING POWER UP





SUBSTRATE VOLTAGE vs SUPPLY VOLTAGE DURING POWER UP



SUPPLY CURRENT vs SUPPLY VOLTAGE DURING POWER UP (ON MEMORY BOARD)