Freescale Semiconductor
Data Sheet: Technical Data

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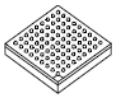
P1023

P1023 QorIQ Integrated Processor Data Sheet



WB-TePBGA I
19 mm x 19 mm

The following list provides an overview of the chip's feature set:

- High-performance 32-bit Book E-enhanced cores that implement the Power Architecture® technology:
  - Two cores
  - 36-bit physical addressing
  - Double-precision floating-point support
  - 32 KB L1 instruction cache and 32 KB L1 data cache for each core
  - 800 MHz maximum clock frequency in single-core mode and 500 MHz dual-core mode
- 256 KB L2 cache with ECC. Also configurable as SRAM and stashing memory.
- Two 10/100/1000 Mbps three-speed Ethernet controllers (TSECs)
  - IEEE® 1588 support
  - RGMII on TSEC2 and RGMII/RMII @ 2.5 V on TSEC1
  - MACSEC only on TSEC1
  - SGMII on both TSEC
- High-speed interfaces supporting various multiplexing options:
  - Three SerDes to 2.5 GHz
  - Three PCI Express interfaces
- High-Speed USB controller (USB 2.0)
  - Host and device support
  - ULPI interface to PHY
- Enhanced Serial peripheral interface (eSPI)
- Integrated security engine
  - Protocol support includes 3DES, AES, RSA/ECC, RNG, single-pass SSL/TLS
- 32-bit DDR3 and DDR3L SDRAM memory controller
- Programmable interrupt controller (PIC) compliant with OpenPIC standard
- Two four-channel DMA controller
- Two I^2C controllers, DUART, timers
- Enhanced local bus controller (eLBC)
- 16 general-purpose I/O signals
- 19 × 19 mm 457-pin WB-TePBGA I

Table of Contents

1 Block Diagram

The following figure shows the major functional units within the chip.

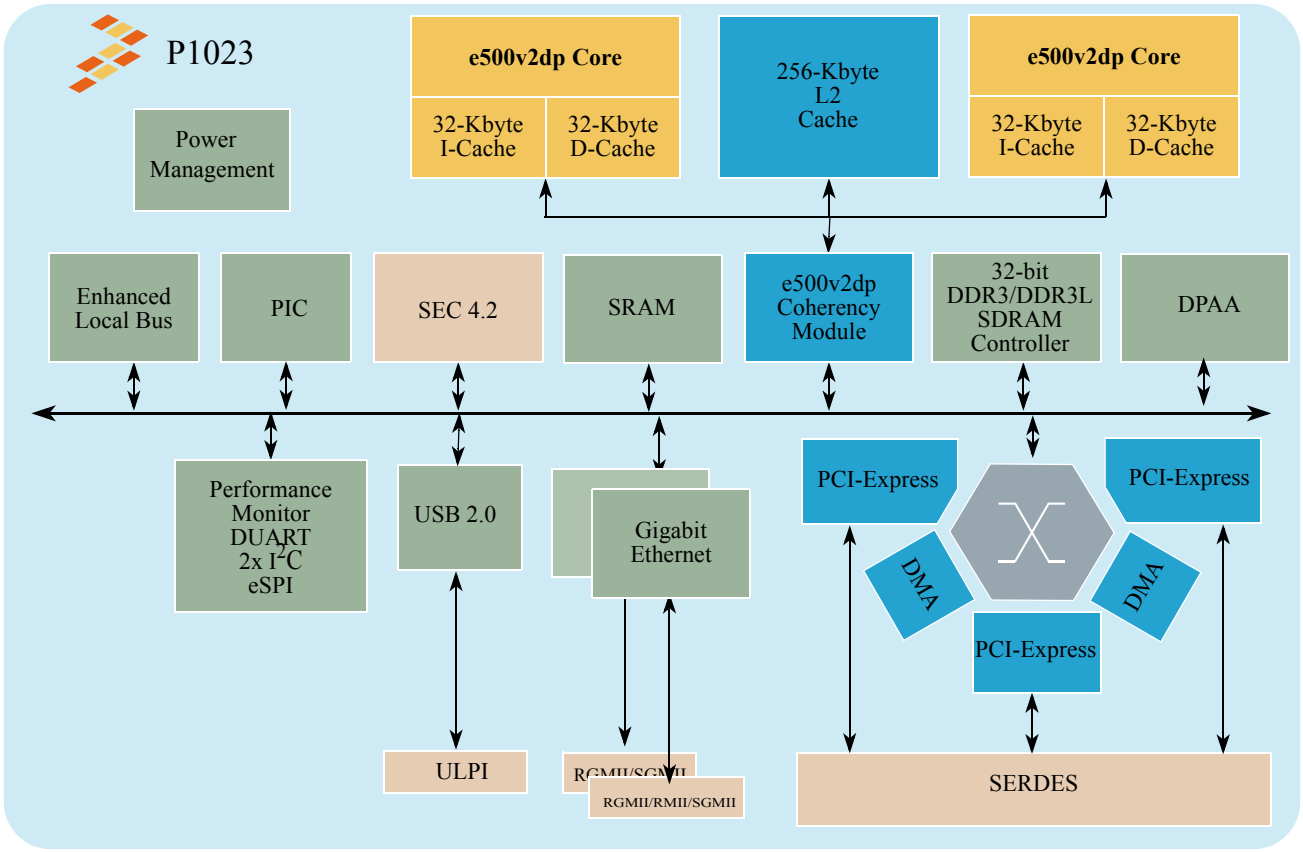


Figure 1. Block Diagram

2 Pin Assignments and Reset States

2.1 Ball Layout Diagram

The following figures show the chip's 457-pin BGA ball map.

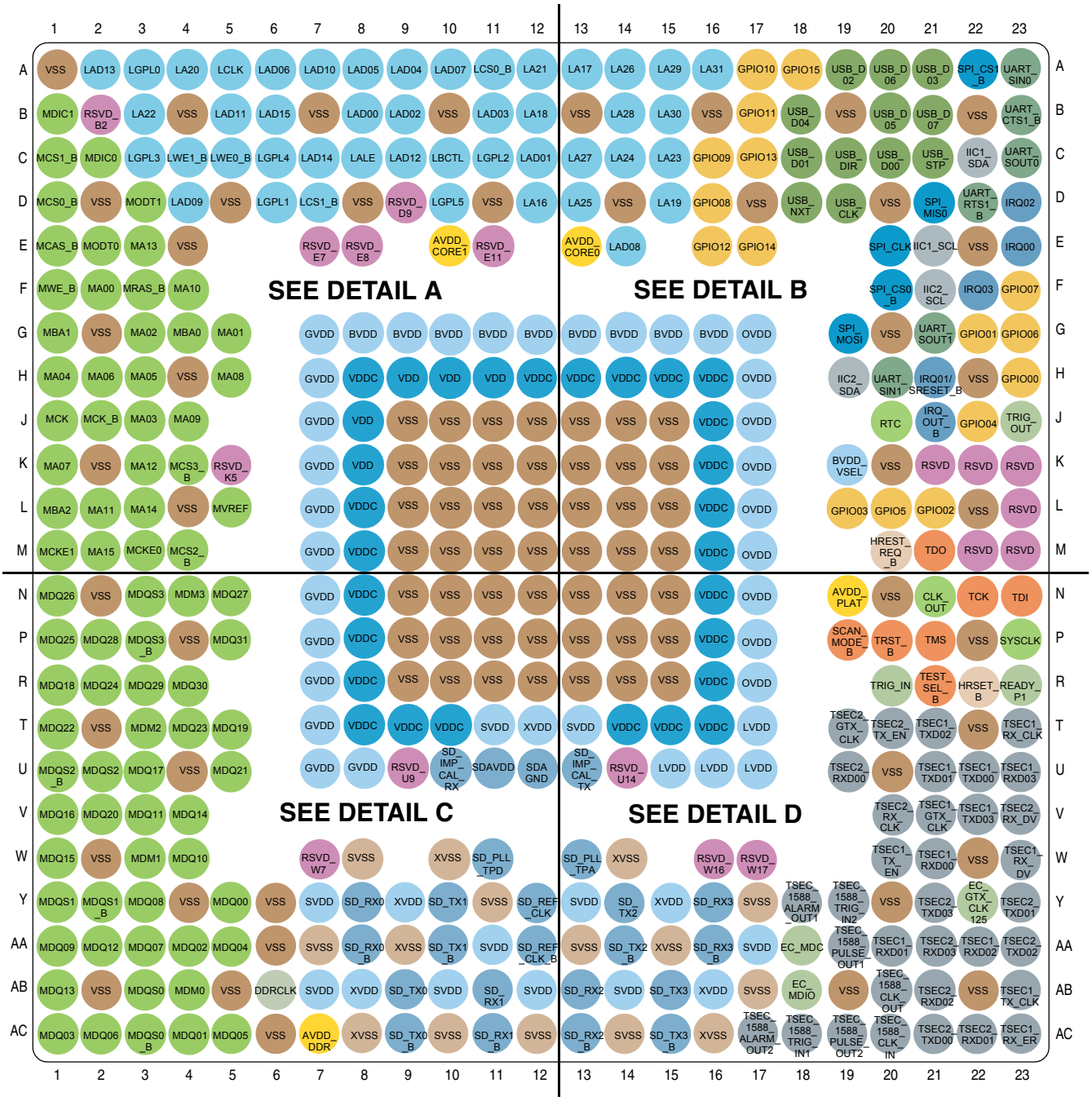


Figure 2. Top View Ballmap

DETAIL A

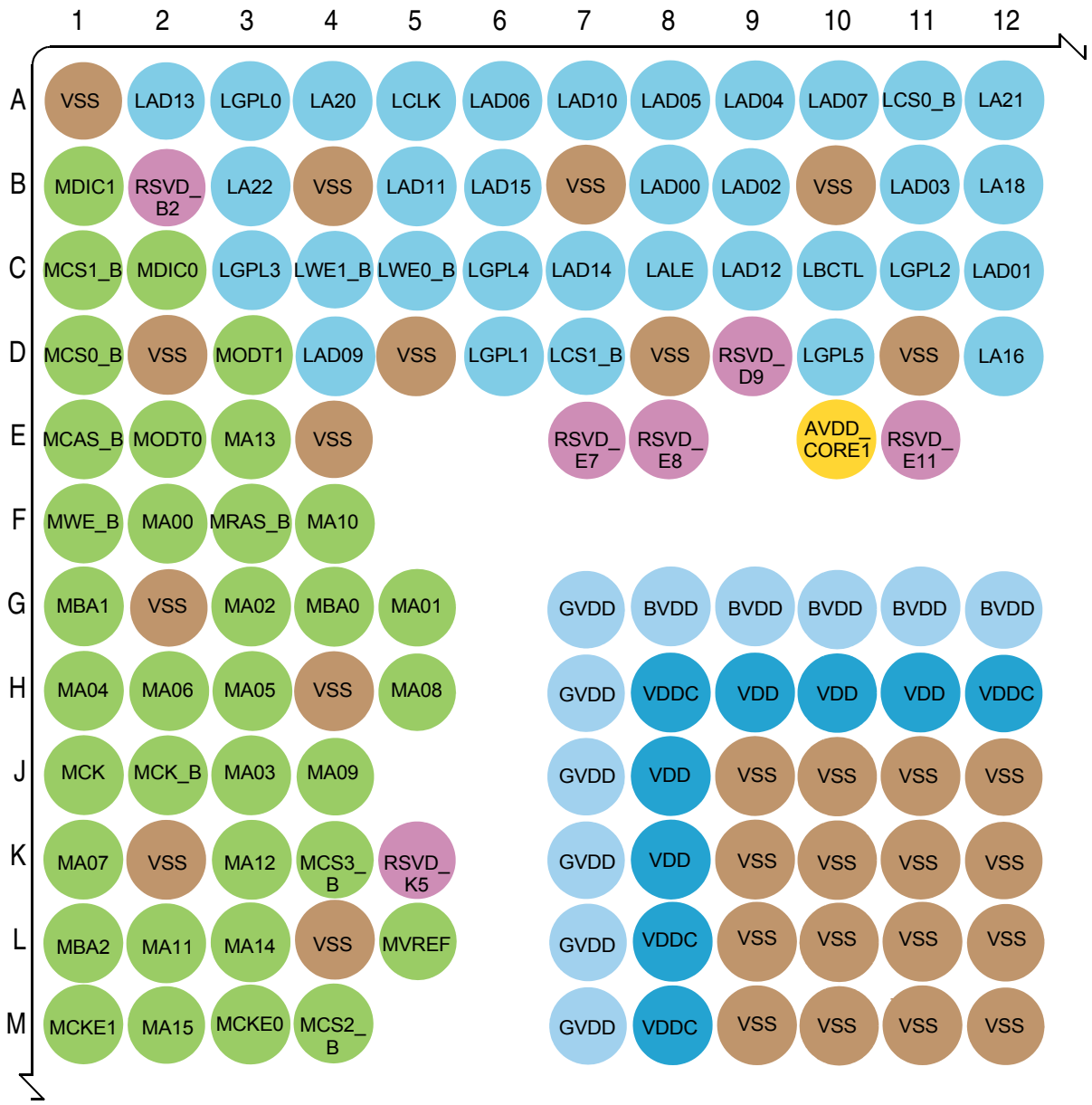


Figure 3. Ball Map—Detail A

DETAIL B

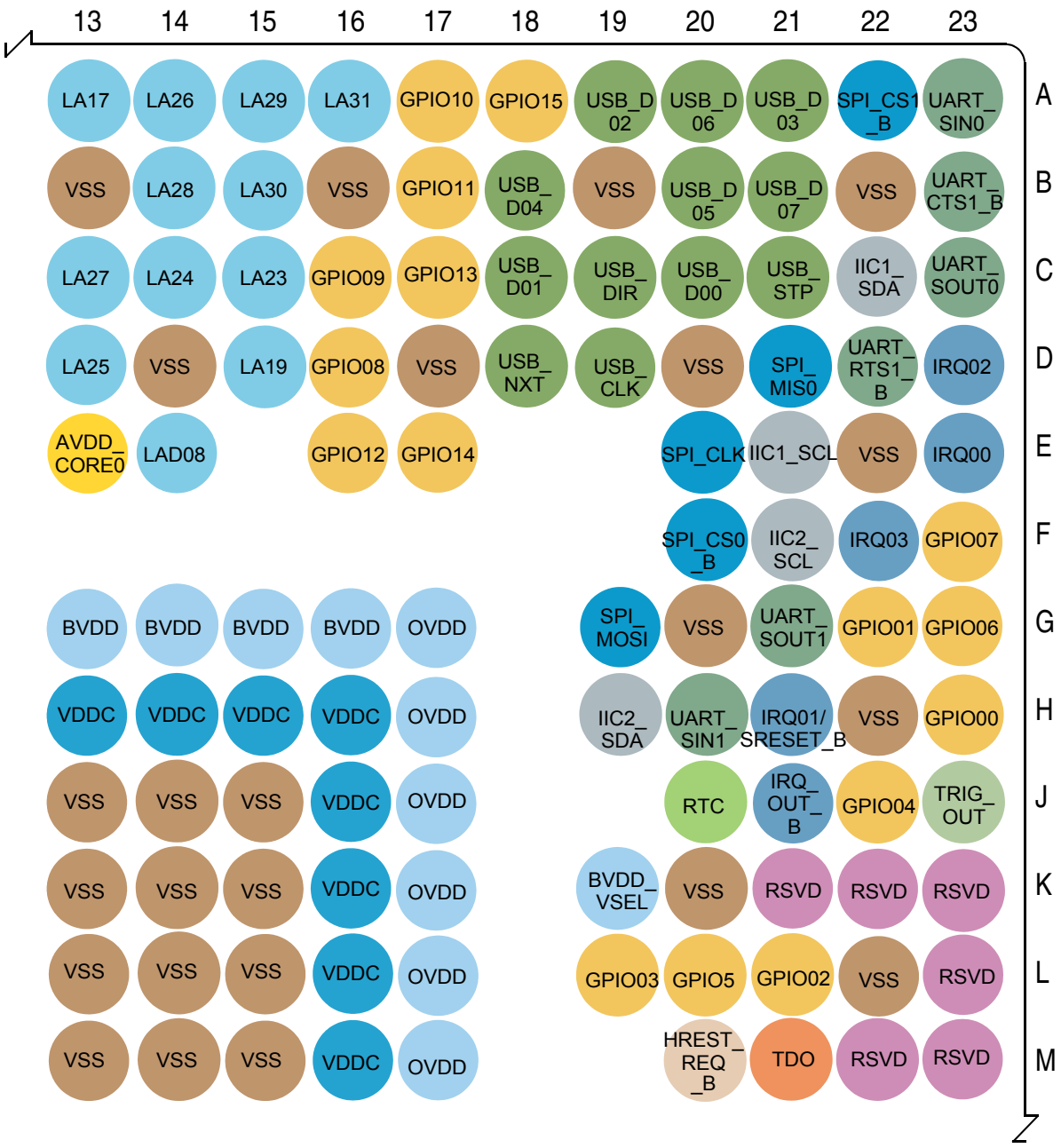


Figure 4. Ball Map—Detail B

DETAIL C

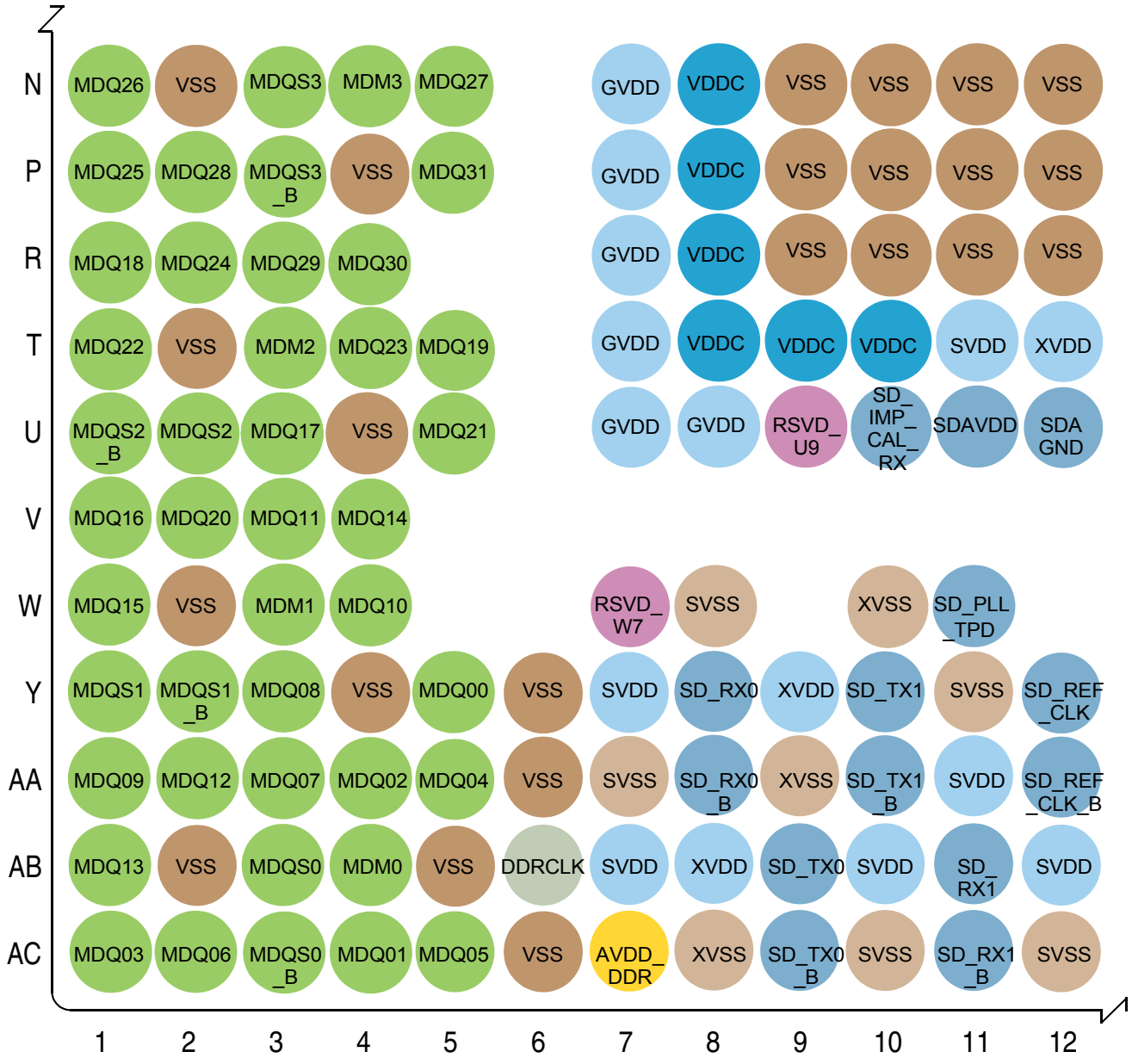


Figure 5. Ball Map—Detail C

DETAIL D

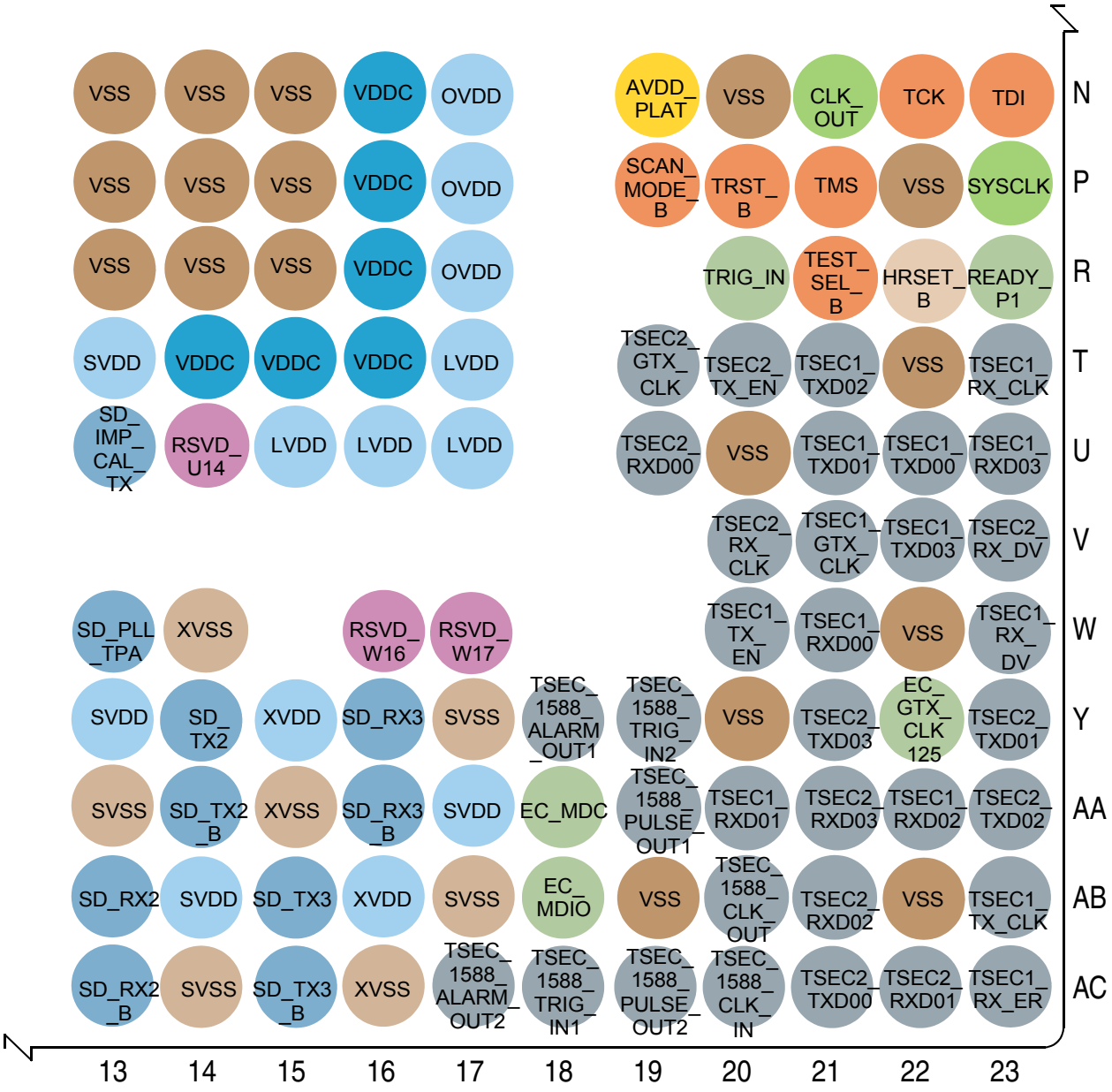


Figure 6. Ball Map—Detail D

2.2 Pinout Assignments

The following table provides the pinout listing for the chip.

Table 1. Pinout Listing

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface					
MDQ00	Data	Y5	I/O	GV_{DD}	—
MDQ01	Data	AC4	I/O	GV_{DD}	—
MDQ02	Data	AA4	I/O	GV_{DD}	—
MDQ03	Data	AC1	I/O	GV_{DD}	—
MDQ04	Data	AA5	I/O	GV_{DD}	—
MDQ05	Data	AC5	I/O	GV_{DD}	—
MDQ06	Data	AC2	I/O	GV_{DD}	—
MDQ07	Data	AA3	I/O	GV_{DD}	—
MDQ08	Data	Y3	I/O	GV_{DD}	—
MDQ09	Data	AA1	I/O	GV_{DD}	—
MDQ10	Data	W4	I/O	GV_{DD}	—
MDQ11	Data	V3	I/O	GV_{DD}	—
MDQ12	Data	AA2	I/O	GV_{DD}	—
MDQ13	Data	AB1	I/O	GV_{DD}	—
MDQ14	Data	V4	I/O	GV_{DD}	—
MDQ15	Data	W1	I/O	GV_{DD}	—
MDQ16	Data	V1	I/O	GV_{DD}	—
MDQ17	Data	U3	I/O	GV_{DD}	—
MDQ18	Data	R1	I/O	GV_{DD}	—
MDQ19	Data	T5	I/O	GV_{DD}	—
MDQ20	Data	V2	I/O	GV_{DD}	—
MDQ21	Data	U5	I/O	GV_{DD}	—
MDQ22	Data	T1	I/O	GV_{DD}	—
MDQ23	Data	T4	I/O	GV_{DD}	—
MDQ24	Data	R2	I/O	GV_{DD}	—
MDQ25	Data	P1	I/O	GV_{DD}	—
MDQ26	Data	N1	I/O	GV_{DD}	—
MDQ27	Data	N5	I/O	GV_{DD}	—
MDQ28	Data	P2	I/O	GV_{DD}	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
MDQ29	Data	R3	I/O	GV_{DD}	—
MDQ30	Data	R4	I/O	GV_{DD}	—
MDQ31	Data	P5	I/O	GV_{DD}	—
MDM0	Data Mask	AB4	O	GV_{DD}	—
MDM1	Data Mask	W3	O	GV_{DD}	—
MDM2	Data Mask	T3	O	GV_{DD}	—
MDM3	Data Mask	N4	O	GV_{DD}	—
MDQS0	Data Strobe	AB3	I/O	GV_{DD}	—
MDQS1	Data Strobe	Y1	I/O	GV_{DD}	—
MDQS2	Data Strobe	U2	I/O	GV_{DD}	—
MDQS3	Data Strobe	N3	I/O	GV_{DD}	—
MDQS0_B	Data Strobe	AC3	I/O	GV_{DD}	—
MDQS1_B	Data Strobe	Y2	I/O	GV_{DD}	—
MDQS2_B	Data Strobe	U1	I/O	GV_{DD}	—
MDQS3_B	Data Strobe	P3	I/O	GV_{DD}	—
MBA0	Bank Select	G4	O	GV_{DD}	—
MBA1	Bank Select	G1	O	GV_{DD}	—
MBA2	Bank Select	L1	O	GV_{DD}	—
MA00	Address	F2	O	GV_{DD}	—
MA01	Address	G5	O	GV_{DD}	—
MA02	Address	G3	O	GV_{DD}	—
MA03	Address	J3	O	GV_{DD}	—
MA04	Address	H1	O	GV_{DD}	—
MA05	Address	H3	O	GV_{DD}	—
MA06	Address	H2	O	GV_{DD}	—
MA07	Address	K1	O	GV_{DD}	—
MA08	Address	H5	O	GV_{DD}	—
MA09	Address	J4	O	GV_{DD}	—
MA10	Address	F4	O	GV_{DD}	—
MA11	Address	L2	O	GV_{DD}	—
MA12	Address	K3	O	GV_{DD}	—
MA13	Address	E3	O	GV_{DD}	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
MA14	Address	L3	O	GV_{DD}	—
MA15	Address	M2	O	GV_{DD}	—
MWE_B	Write Enable	F1	O	GV_{DD}	—
MRAS_B	Row Address Strobe	F3	O	GV_{DD}	—
MCAS_B	Column Address Strobe	E1	O	GV_{DD}	—
MCS0_B	Chip Select	D1	O	GV_{DD}	—
MCS1_B	Chip Select	C1	O	GV_{DD}	—
MCS2_B	Chip Select	M4	O	GV_{DD}	—
MCS3_B	Chip Select	K4	O	GV_{DD}	—
MCKE0	Clock Enable	M3	O	GV_{DD}	—
MCKE1	Clock Enable	M1	O	GV_{DD}	—
MCK	Clock	J1	O	GV_{DD}	—
MCK_B	Clock Complement	J2	O	GV_{DD}	—
MODT0	On Die Termination	E2	O	GV_{DD}	—
MODT1	On Die Termination	D3	O	GV_{DD}	—
MDIC0	Driver Impedance Calibration	C2	I/O	GV_{DD}	—
MDIC1	Driver Impedance Calibration	B1	I/O	GV_{DD}	—
MVREF	DDR Reference Voltage	L5	I	$GV_{DD}/2$	—
SerDes					
SD_TX_3	Tx Data (pos)	AB15	O	XVDD	—
SD_TX_2	Tx Data (pos)	Y14	O	XVDD	—
SD_TX_1	Tx Data (pos)	Y10	O	XVDD	—
SD_TX_0	Tx Data (pos)	AB9	O	XVDD	—
SD_TX_B3	Tx Data (neg)	AC15	O	XVDD	—
SD_TX_B2	Tx Data (neg)	AA14	O	XVDD	—
SD_TX_B1	Tx Data (neg)	AA10	O	XVDD	—
SD_TX_B0	Tx Data (neg)	AC9	O	XVDD	—
SD_RX_3	Rx Data (pos)	Y16	I	XVDD	—
SD_RX_2	Rx Data (pos)	AB13	I	XVDD	—
SD_RX_1	Rx Data (pos)	AB11	I	XVDD	—
SD_RX_0	Rx Data (pos)	Y8	I	XVDD	—
SD_RX_B3	Rx Data (neg)	AA16	I	XVDD	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SD_RX_B2	Rx Data (neg)	AC13	I	XVDD	—
SD_RX_B1	Rx Data (neg)	AC11	I	XVDD	—
SD_RX_B0	Rx Data (neg)	AA8	I	XVDD	—
SD_REF_CLK	PLL Reference Clock	Y12	I	XVDD	—
SD_REF_CLK_B	PLL Reference Clock Complement	AA12	I	XVDD	—
SD_PLL_TPD	PLL Test Point Digital	W11	O	XVDD	—
SD_IMP_CAL_RX	SerDes Rx Impedance Calibration	U10	I	XVDD	—
SD_IMP_CAL_TX	SerDes Tx Impedance Calibration	U13	I	XVDD	—
SD_PLL_TPA	SerDes PLL Test Point Analog	W13	O	XVDD	—
Enhanced Local Bus Controller Interface					
LAD00	Muxed Data/Address	B8	I/O	BV_{DD}	2
LAD01	Muxed Data/Address	C12	I/O	BV_{DD}	2
LAD02	Muxed Data/Address	B9	I/O	BV_{DD}	2
LAD03	Muxed Data/Address	B11	I/O	BV_{DD}	2
LAD04	Muxed Data/Address	A9	I/O	BV_{DD}	2
LAD05	Muxed Data/Address	A8	I/O	BV_{DD}	2
LAD06	Muxed Data/Address	A6	I/O	BV_{DD}	2
LAD07	Muxed Data/Address	A10	I/O	BV_{DD}	2
LAD08	Muxed Data/Address	E14	I/O	BV_{DD}	2
LAD09	Muxed Data/Address	D4	I/O	BV_{DD}	2
LAD10	Muxed Data/Address	A7	I/O	BV_{DD}	2
LAD11	Muxed Data/Address	B5	I/O	BV_{DD}	2
LAD12	Muxed Data/Address	C9	I/O	BV_{DD}	2
LAD13	Muxed Data/Address	A2	I/O	BV_{DD}	2
LAD14	Muxed Data/Address	C7	I/O	BV_{DD}	2
LAD15	Muxed Data/Address	B6	I/O	BV_{DD}	2
LA16	Address	D12	O	BV_{DD}	2
LA17	Address	A13	O	BV_{DD}	5
LA18	Address	B12	O	BV_{DD}	2
LA19	Address	D15	O	BV_{DD}	2
LA20	Address	A4	O	BV_{DD}	2
LA21	Address	A12	O	BV_{DD}	2

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
LA22	Address	B3	O	BV_{DD}	5
LA23	Address	C15	O	BV_{DD}	2
LA24	Address	C14	O	BV_{DD}	2
LA25	Address	D13	O	BV_{DD}	2
LA26	Address	A14	O	BV_{DD}	2
LA27	Address	C13	O	BV_{DD}	2
LA28	Address	B14	O	BV_{DD}	2
LA29	Address	A15	O	BV_{DD}	2
LA30	Address	B15	O	BV_{DD}	2
LA31	Address	A16	O	BV_{DD}	2
LCS0_B	Chip Select	A11	O	BV_{DD}	—
LCS1_B	Chip Select	D7	O	BV_{DD}	—
LWE0_B	Write Enable	C5	O	BV_{DD}	2
LWE1_B	Write Enable	C4	O	BV_{DD}	2
LBCTL	Buffer Control	C10	O	BV_{DD}	2
LALE	Address Latch Enable	C8	O	BV_{DD}	2
LGPL0	UPM General Purpose Line 0	A3	O	BV_{DD}	2
LGPL1	UPM General Purpose Line 1	D6	O	BV_{DD}	5
LGPL2	UPM General Purpose Line 2	C11	O	BV_{DD}	2
LGPL3	UPM General Purpose Line 3	C3	I/O	BV_{DD}	2
LGPL4	UPM General Purpose Line 4	C6	I/O	BV_{DD}	—
LGPL5	UPM General Purpose Line 5	D10	O	BV_{DD}	2
LCLK	Local Bus Clock	A5	O	BV_{DD}	—
Programmable Interrupt Controller					
IRQ00	External Interrupt	E23	I	OV_{DD}	—
IRQ01/SRESET_B	External Interrupt/Soft Reset	H21	I	OV_{DD}	—
IRQ02/CKSTP_IN0_B	External Interrupt/Checkstop In	D23	I	OV_{DD}	—
IRQ03/CKSTP_IN1_B	External Interrupt/Checkstop In	F22	I	OV_{DD}	—
IRQ_OUT_B/CKSTOP_OUT 0_B	Interrupt Output/Checkstop Out	J21	O	OV_{DD}	—
1588					
TSEC_1588_CLK_IN	Clock In	AC20	I	LV_{DD}	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TSEC_1588_TRIG_IN1	Trigger In	AC18	I	LV_{DD}	—
TSEC_1588_TRIG_IN2/DMA2_DREQ_B	Trigger In/DMA2 Request	Y19	I	LV_{DD}	—
TSEC_1588_ALARM_OUT1	Trigger Out	Y18	O	LV_{DD}	2
TSEC_1588_ALARM_OUT2/DMA2_DACK_B	Trigger Out/DMA2 Acknowledge	AC17	O	LV_{DD}	2
TSEC_1588_CLK_OUT/DMA2_DDONE_B	Clock Out/DMA2 Done	AB20	O	LV_{DD}	2
TSEC_1588_PULSE_OUT1	Pulse Out	AA19	O	LV_{DD}	2
TSEC_1588_PULSE_OUT2	Pulse Out	AC19	O	LV_{DD}	2
Ethernet Management Interface					
EC_MDC	Management Data Clock	AA18	O	LV_{DD}	—
EC_MDIO	Management Data In/Out	AB18	I/O	LV_{DD}	—
Gigabit Ethernet Reference Clock					
EC_GTX_CLK125	Reference Clock	Y22	I	LV_{DD}	—
Three Speed Ethernet Controller 1					
TSEC1_TXD03	Tx Data	V22	O	LV_{DD}	2
TSEC1_TXD02	Tx Data	T21	O	LV_{DD}	2
TSEC1_TXD01	Tx Data	U21	O	LV_{DD}	2
TSEC1_TXD00	Tx Data	U22	O	LV_{DD}	2
TSEC1_TX_EN	Tx Enable	W20	O	LV_{DD}	—
TSEC1_TX_CLK/TSEC1_GTX_CLK125	Tx Clock/Reference Clock	AB23	I	LV_{DD}	—
TSEC1_GTX_CLK	Tx Clock Out	V21	O	LV_{DD}	—
TSEC1_RXD03	Rx Data	U23	I	LV_{DD}	—
TSEC1_RXD02	Rx Data	AA22	I	LV_{DD}	—
TSEC1_RXD01	Rx Data	AA20	I	LV_{DD}	—
TSEC1_RXD00	Rx Data	W21	I	LV_{DD}	—
TSEC1_RX_DV	Rx Data Valid	W23	I	LV_{DD}	—
TSEC1_RX_ER	Rx Error	AC23	I	LV_{DD}	—
TSEC1_RX_CLK	Rx Clock	T23	I	LV_{DD}	—
Three Speed Ethernet Controller 2					
TSEC2_TXD03	Tx Data	Y21	O	LV_{DD}	6

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_TXD02	Tx Data	AA23	O	LV_{DD}	2, 6
TSEC2_TXD01	Tx Data	Y23	O	LV_{DD}	2, 6
TSEC2_TXD00	Tx Data	AC21	O	LV_{DD}	2, 6
TSEC2_TX_EN	Tx Enable	T20	O	LV_{DD}	—
TSEC2_GTX_CLK	Tx Clock	T19	O	LV_{DD}	—
TSEC2_RXD03	Rx Data	AA21	I	LV_{DD}	6
TSEC2_RXD02	Rx Data	AB21	I	LV_{DD}	6
TSEC2_RXD01	Rx Data	AC22	I	LV_{DD}	6
TSEC2_RXD00	Rx Data	U19	I	LV_{DD}	6
TSEC2_RX_DV	Rx Data Valid	V23	I	LV_{DD}	6
TSEC2_RX_CLK	Rx Clock	V20	I	LV_{DD}	6
DUART					
UART_SOUT0/MSRCID4/LB_MSRCID4	Tx Data/Memory Debug Source ID	C23	O	OV_{DD}	2
UART_SOUT1/MSRCID3/LB_MSRCID3	Tx Data/Memory Debug Source ID	G21	O	OV_{DD}	2
UART_SIN0/MSRCID2/LB_MSRCID2	Rx Data/Memory Debug Source ID	A23	I/O	OV_{DD}	—
UART_SIN1/MSRCID1/LB_MSRCID1	Rx Data/Memory Debug Source ID	H20	I/O	OV_{DD}	—
UART_CTS1_B/MSRCID0/LB_MSRCID0	Clear To Send/Memory Debug Source ID	B23	I/O	OV_{DD}	—
UART_RTS1_B/MDVAL/LB_MDVAL	Ready to Send/Memory Debug Data Valid	D22	O	OV_{DD}	—
I^2C					
IIC1_SDA	Serial Data	C22	I/O	OV_{DD}	—
IIC1_SCL	Serial Clock	E21	I/O	OV_{DD}	—
IIC2_SDA	Serial Data	H19	I/O	OV_{DD}	—
IIC2_SCL	Serial Clock	F21	I/O	OV_{DD}	—
eSPI					
SPI_MISO	Master Input Slave Output Data	D21	I	OV_{DD}	—
SPI_MOSI	Master Output Slave Input Data	G19	O	OV_{DD}	—
SPI_CS0_B	SPI Slave Select	F20	O	OV_{DD}	5
SPI_CS1_B	SPI Slave Select	A22	O	OV_{DD}	5

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SPI_CLK	Serial clock	E20	O	OV_{DD}	—
USB					
USB_NXT	Next Data Throttle Control	D18	I	OV_{DD}	—
USB_DIR	Databus Direction	C19	I	OV_{DD}	—
USB_STP/MDVAL/LB_MDVAL	Stop/Memory Debug Data Valid	C21	O	OV_{DD}	5
USB_CLK	PHY Clock	D19	I	OV_{DD}	—
USB_D07/MSRCID4/LB_MSRCID4	Bidirectional Databus/Memory Debug Source ID	B21	I/O	OV_{DD}	—
USB_D06/MSRCID3/LB_MSRCID3	Bidirectional Databus/Memory Debug Source ID	A20	I/O	OV_{DD}	—
USB_D05/MSRCID2/LB_MSRCID2	Bidirectional Databus/Memory Debug Source ID	B20	I/O	OV_{DD}	—
USB_D04/MSRCID1/LB_MSRCID1	Bidirectional Databus/Memory Debug Source ID	B18	I/O	OV_{DD}	—
USB_D03/MSRCID0/LB_MSRCID0	Bidirectional Databus/Memory Debug Source ID	A21	I/O	OV_{DD}	—
USB_D02	Bidirectional Databus	A19	I/O	OV_{DD}	—
USB_D01	Bidirectional Databus	C18	I/O	OV_{DD}	—
USB_D00	Bidirectional Databus	C20	I/O	OV_{DD}	—
General-Purpose Input/Output					
GPIO00/IRQ7/ASLEEP	General Purpose Input/Output/External Interrupt/Asleep	H23	I/O	OV_{DD}	—
GPIO01/IRQ8	General Purpose Input/Output/External Interrupt	G22	I/O	OV_{DD}	—
GPIO02/IRQ9/POWER_EN	General Purpose Input/Output/External Interrupt/Power Enable	L21	I/O	OV_{DD}	7
GPIO03/IRQ10/CKSTP_OUT1_B	General Purpose Input/Output/External Interrupt/Checkstop Out	L19	I/O	OV_{DD}	—
GPIO04/UDE1_B	General Purpose Input/Output/Unconditional Debug Event	J22	I/O	OV_{DD}	—
GPIO05/MCP0_B	General Purpose Input/Output/Machine Check Processor	L20	I/O	OV_{DD}	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
GPIO06/MCP1_B	General Purpose Input/Output/Machine Check Processor	G23	I/O	OV_{DD}	—
GPIO07/UDE0_B	General Purpose Input/Output/Unconditional Debug Event	F23	I/O	OV_{DD}	—
GPIO08/DMA1_DDONE_B	General Purpose Input/Output/DMA1 Done	D16	I/O	BV_{DD}	—
GPIO09/DMA1_DACK_B	General Purpose Input/Output/DMA1 Acknowledge	C16	I/O	BV_{DD}	—
GPIO10/USB_PCTL0	General Purpose Input/Output/USB port Control	A17	I/O	BV_{DD}	—
GPIO11/USB_PCTL1	General Purpose Input/Output/USB port Control	B17	I/O	BV_{DD}	—
GPIO12/TSEC1_XTRNL_TX_STMP	General Purpose Input/Output/TSEC1 External Transmit Timestamp	E16	I/O	BV_{DD}	—
GPIO13/TSEC1_XTRNL_RX_STMP	General Purpose Input/Output/TSEC1 External ReceiveTimestamp	C17	I/O	BV_{DD}	—
GPIO14/TSEC2_XTRNL_TX_STMP/DMA1_DREQ_B	General Purpose Input/Output/TSEC2 External Transmit Timestamp/DMA1 Request	E17	I/O	BV_{DD}	—
GPIO15/TSEC2_XTRNL_RX_STMP	General Purpose Input/Output/TSEC2 External Receive Timestamp	A18	I/O	BV_{DD}	—
System Control					
HRESET_B	Hard Reset	R22	I	OV_{DD}	—
HRESET_REQ_B	Hard Reset - Request	M20	O	OV_{DD}	5
Debug					
TRIG_IN	Trigger In	R20	I	OV_{DD}	—
TRIG_OUT	Trigger Out	J23	O	OV_{DD}	5
READY_P1	Ready Proc1	R23	O	OV_{DD}	2
Clocks					
CLK_OUT	Clock Out	N21	O	OV_{DD}	—
RTC	Real Time Clock	J20	I	OV_{DD}	—
DDRCLK	DDR Clock	AB6	I	OV_{DD}	—
SYSCLK	System Clock	P23	I	OV_{DD}	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
DFT					
SCAN_MODE_B	Scan Mode	P19	I	OV_{DD}	—
TEST_SEL_B	Test Select	R21	I	OV_{DD}	4
JTAG					
TCK	Test Clock	N22	I	OV_{DD}	—
TDI	Test Data In	N23	I	OV_{DD}	—
TDO	Test Data Out	M21	O	OV_{DD}	—
TMS	Test Mode Select	P21	I	OV_{DD}	—
TRST_B	Test Reset	P20	I	OV_{DD}	—
Power and Ground Signals					
BVDD_VSEL	BVDD Voltage Selection	K19	—	—	1
AVDD_CORE0	CPU0 PLL supply	E13	—	—	—
AVDD_CORE1	CPU1 PLL supply	E10	—	—	—
AVDD_DDR	DDR PLL supply	AC7	—	—	—
AVDD_PLAT	Platform PLL supply	N19	—	—	—
SVDD	SerDes core logic supply	Y7	—	—	—
SVDD	SerDes core logic supply	AB7	—	—	—
SVDD	SerDes core logic supply	AB10	—	—	—
SVDD	SerDes core logic supply	T11	—	—	—
SVDD	SerDes core logic supply	AA11	—	—	—
SVDD	SerDes core logic supply	AB12	—	—	—
SVDD	SerDes core logic supply	T13	—	—	—
SVDD	SerDes core logic supply	Y13	—	—	—
SVDD	SerDes core logic supply	AB14	—	—	—
SVDD	SerDes core logic supply	AA17	—	—	—
BVDD	Local Bus & GPIO I/O supply	G8	—	—	—
BVDD	Local Bus & GPIO I/O supply	G9	—	—	—
BVDD	Local Bus & GPIO I/O supply	G10	—	—	—
BVDD	Local Bus & GPIO I/O supply	G11	—	—	—
BVDD	Local Bus & GPIO I/O supply	G12	—	—	—
BVDD	Local Bus & GPIO I/O supply	G13	—	—	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
BVDD	Local Bus & GPIO I/O supply	G14	—	—	—
BVDD	Local Bus & GPIO I/O supply	G15	—	—	—
BVDD	Local Bus & GPIO I/O supply	G16	—	—	—
GVDD	DDR I/O supply	G7	—	—	—
GVDD	DDR I/O supply	H7	—	—	—
GVDD	DDR I/O supply	J7	—	—	—
GVDD	DDR I/O supply	K7	—	—	—
GVDD	DDR I/O supply	L7	—	—	—
GVDD	DDR I/O supply	M7	—	—	—
GVDD	DDR I/O supply	N7	—	—	—
GVDD	DDR I/O supply	P7	—	—	—
GVDD	DDR I/O supply	R7	—	—	—
GVDD	DDR I/O supply	T7	—	—	—
GVDD	DDR I/O supply	U7	—	—	—
GVDD	DDR I/O supply	U8	—	—	—
LVDD	TSEC 1&3 I/O supply	U15	—	—	—
LVDD	TSEC 1&3 I/O supply	U16	—	—	—
LVDD	TSEC 1&3 I/O supply	T17	—	—	—
LVDD	TSEC 1&3 I/O supply	U17	—	—	—
OVDD	General I/O supply	G17	—	—	—
OVDD	General I/O supply	H17	—	—	—
OVDD	General I/O supply	J17	—	—	—
OVDD	General I/O supply	K17	—	—	—
OVDD	General I/O supply	L17	—	—	—
OVDD	General I/O supply	M17	—	—	—
OVDD	General I/O supply	N17	—	—	—
OVDD	General I/O supply	P17	—	—	—
OVDD	General I/O supply	R17	—	—	—
VDD	CPU1 Supplies	J8	—	—	—
VDD	CPU1 Supplies	K8	—	—	—
VDD	CPU1 Supplies	H9	—	—	—
VDD	CPU1 Supplies	H10	—	—	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
VDD	CPU1 Supplies	H11	—	—	—
VDDC	Platform and CPU0 Supplies	H8	—	—	—
VDDC	Platform and CPU0 Supplies	L8	—	—	—
VDDC	Platform and CPU0 Supplies	M8	—	—	—
VDDC	Platform and CPU0 Supplies	N8	—	—	—
VDDC	Platform and CPU0 Supplies	R8	—	—	—
VDDC	Platform and CPU0 Supplies	P8	—	—	—
VDDC	Platform and CPU0 Supplies	T8	—	—	—
VDDC	Platform and CPU0 Supplies	T9	—	—	—
VDDC	Platform and CPU0 Supplies	T10	—	—	—
VDDC	Platform and CPU0 Supplies	H12	—	—	—
VDDC	Platform and CPU0 Supplies	H13	—	—	—
VDDC	Platform and CPU0 Supplies	H14	—	—	—
VDDC	Platform and CPU0 Supplies	T14	—	—	—
VDDC	Platform and CPU0 Supplies	H15	—	—	—
VDDC	Platform and CPU0 Supplies	T15	—	—	—
VDDC	Platform and CPU0 Supplies	H16	—	—	—
VDDC	Platform and CPU0 Supplies	J16	—	—	—
VDDC	Platform and CPU0 Supplies	K16	—	—	—
VDDC	Platform and CPU0 Supplies	L16	—	—	—
VDDC	Platform and CPU0 Supplies	M16	—	—	—
VDDC	Platform and CPU0 Supplies	N16	—	—	—
VDDC	Platform and CPU0 Supplies	R16	—	—	—
VDDC	Platform and CPU0 Supplies	P16	—	—	—
VDDC	Platform and CPU0 Supplies	T16	—	—	—
XVDD	SerDes Transceiver supply	AB8	—	—	—
XVDD	SerDes Transceiver supply	Y9	—	—	—
XVDD	SerDes Transceiver supply	T12	—	—	—
XVDD	SerDes Transceiver supply	Y15	—	—	—
XVDD	SerDes Transceiver supply	AB16	—	—	—
SDAVDD	SerDes PLL supply	U11	—	—	—
SDAGND	SerDes PLL GND	U12	—	—	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
SGND	Serdes Transceiver core logic GND	AA7	—	—	—
SGND	Serdes Transceiver core logic GND	W8	—	—	—
SGND	Serdes Transceiver core logic GND	AC10	—	—	—
SGND	Serdes Transceiver core logic GND	Y11	—	—	—
SGND	Serdes Transceiver core logic GND	AC12	—	—	—
SGND	Serdes Transceiver core logic GND	AA13	—	—	—
SGND	Serdes Transceiver core logic GND	AC14	—	—	—
SGND	Serdes Transceiver core logic GND	Y17	—	—	—
SGND	Serdes Transceiver core logic GND	AB17	—	—	—
XGND	Serdes Transceiver pad GND	AC8	—	—	—
XGND	Serdes Transceiver pad GND	AA9	—	—	—
XGND	Serdes Transceiver pad GND	W10	—	—	—
XGND	Serdes Transceiver pad GND	W14	—	—	—
XGND	Serdes Transceiver pad GND	AA15	—	—	—
XGND	Serdes Transceiver pad GND	AC16	—	—	—
GND	GND	A1	—	—	—
GND	GND	D2	—	—	—
GND	GND	G2	—	—	—
GND	GND	K2	—	—	—
GND	GND	N2	—	—	—
GND	GND	T2	—	—	—
GND	GND	W2	—	—	—
GND	GND	AB2	—	—	—
GND	GND	B4	—	—	—
GND	GND	E4	—	—	—
GND	GND	H4	—	—	—
GND	GND	L4	—	—	—
GND	GND	P4	—	—	—
GND	GND	U4	—	—	—
GND	GND	Y4	—	—	—
GND	GND	D5	—	—	—
GND	GND	AB5	—	—	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
GND	GND	Y6	—	—	—
GND	GND	AA6	—	—	—
GND	GND	AC6	—	—	—
GND	GND	B7	—	—	—
GND	GND	D8	—	—	—
GND	GND	J9	—	—	—
GND	GND	K9	—	—	—
GND	GND	L9	—	—	—
GND	GND	M9	—	—	—
GND	GND	N9	—	—	—
GND	GND	P9	—	—	—
GND	GND	R9	—	—	—
GND	GND	B10	—	—	—
GND	GND	J10	—	—	—
GND	GND	K10	—	—	—
GND	GND	L10	—	—	—
GND	GND	M10	—	—	—
GND	GND	N10	—	—	—
GND	GND	P10	—	—	—
GND	GND	R10	—	—	—
GND	GND	D11	—	—	—
GND	GND	J11	—	—	—
GND	GND	K11	—	—	—
GND	GND	L11	—	—	—
GND	GND	M11	—	—	—
GND	GND	N11	—	—	—
GND	GND	P11	—	—	—
GND	GND	R11	—	—	—
GND	GND	J12	—	—	—
GND	GND	K12	—	—	—
GND	GND	L12	—	—	—
GND	GND	M12	—	—	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
GND	GND	N12	—	—	—
GND	GND	R12	—	—	—
GND	GND	P12	—	—	—
GND	GND	B13	—	—	—
GND	GND	J13	—	—	—
GND	GND	K13	—	—	—
GND	GND	L13	—	—	—
GND	GND	M13	—	—	—
GND	GND	N13	—	—	—
GND	GND	P13	—	—	—
GND	GND	R13	—	—	—
GND	GND	D14	—	—	—
GND	GND	J14	—	—	—
GND	GND	K14	—	—	—
GND	GND	L14	—	—	—
GND	GND	M14	—	—	—
GND	GND	N14	—	—	—
GND	GND	P14	—	—	—
GND	GND	R14	—	—	—
GND	GND	J15	—	—	—
GND	GND	K15	—	—	—
GND	GND	L15	—	—	—
GND	GND	M15	—	—	—
GND	GND	N15	—	—	—
GND	GND	P15	—	—	—
GND	GND	R15	—	—	—
GND	GND	B16	—	—	—
GND	GND	D17	—	—	—
GND	GND	B19	—	—	—
GND	GND	AB19	—	—	—
GND	GND	D20	—	—	—
GND	GND	G20	—	—	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
GND	GND	K20	—	—	—
GND	GND	N20	—	—	—
GND	GND	U20	—	—	—
GND	GND	Y20	—	—	—
GND	GND	B22	—	—	—
GND	GND	E22	—	—	—
GND	GND	H22	—	—	—
GND	GND	L22	—	—	—
GND	GND	P22,	—	—	—
GND	GND	T22	—	—	—
GND	GND	W22	—	—	—
GND	GND	AB22	—	—	—
Reserved and No Connects					
RSVD	Reserved	K5	—	—	3
RSVD	Reserved	E7	—	—	3
RSVD	Reserved	E8	—	—	3
RSVD	Reserved	D9	—	—	3
RSVD	Reserved	E11	—	—	3
RSVD	Reserved	B2	—	—	3
RSVD	Reserved	U14	—	—	3
RSVD	Reserved	U9	—	—	3
RSVD	Reserved	W16	—	—	3
RSVD	Reserved	W17	—	—	3
RSVD	Reserved	W7	—	—	3
RSVD	Reserved	K22	—	—	3
RSVD	Reserved	K21	—	—	3
RSVD	Reserved	L23	—	—	3
RSVD	Reserved	K23	—	—	3
RSVD	Reserved	M23	—	—	3

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
RSVD	Reserved	M22	—	—	3

Note:
1. Tie this pin to GND to select 1.8V BVDD; tie this pin to VDD to select 3.3V BVDD.
2. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kO pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
3. This pin should not be connected.
4. This pin should be pulled up.
5. This pin is a reserved reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pin must NOT be pulled down during power-on reset.
6. This pin is reserved by default and must be enabled by pin multiplexing.
7. POWER_EN is the default function for this pin.

3 Electrical Characteristics

This section provides the AC and DC electrical specifications for the chip. The chip is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

3.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

3.1.1 Absolute Maximum Ratings

The following table provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic	Symbol	Max Value	Unit	Note
Core 0 and Platform supply voltage	V_{DDC}	–0.3 to 1.1	V	—
Core 1 supply voltage	V_{DD}	–0.3 to 1.1	V	—
PLL supply voltage	AV_{DD}_CORE0 AV_{DD}_CORE1 AV_{DD}_DDR AV_{DD}_PLAT $SDAV_{DD}$	–0.3 to 1.1	V	8
Core power supply for SerDes transceivers	SV_{DD}	–0.3 to 1.1	V	—
Pad power supply for SerDes transceivers	XV_{DD}	–0.3 to 1.1	V	—
DDR3 DRAM I/O voltage	GV_{DD}	–0.3 to 1.65 DDR3 –0.3 to 1.485 DDR3L	V	—
Three-speed Ethernet I/O, Ethernet management voltage (TSEC)	LV_{DD}	–0.3 to 2.75	V	—

Table 2. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Max Value	Unit	Note
DUART, system control and power management, I^2C, GPIO x8 and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
USB, eSPI		OV_{DD}	–0.3 to 3.63	V	—
Enhanced local bus I/O voltage and GPIOx8 voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 1.98	V	—
Input voltage	DDR3 DRAM signals	MV_{IN}	–0.3 to (GVDD + 0.3)	V	2, 7
	DDR3 DRAM reference	MV_{REF}	–0.3 to (GV_{DD}/2 + 0.3)	V	7
	Three-speed Ethernet signals	LV_{IN}	–0.3 to (LVDD + 0.3)	V	3, 7
	Enhanced local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	—	5, 7
	DUART, DDRCLK, SYSCLK, system control and power management, I^2C, clocking, I/O voltage select, and JTAG I/O voltage	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	4, 7
	USB, eSPI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	4, 7
	SerDes signals	XV_{IN}	–0.3 to (XV_{DD} + 0.3)	V	6, 7
Storage temperature range		T_{STG}	–55 to 150	°C	—

Note:

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution**: MVIN must not exceed GVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution**: LVIN must not exceed LVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution**: OVIN must not exceed OVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. **Caution**: BVIN must not exceed BVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. **Caution**: XVIN must not exceed XVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. (X,B,M,L,O)VIN and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.
8. AV_{DD} is measured at the input to the filter and not at the pin of the device.

3.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this device. Note that the values in the following table are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Note
Core 0 and Platform supply voltage	V_{DDC}	1.0 ± 50 mV	V	1
Core 1 supply voltage	V_{DD}	1.0 ± 50 mV	V	1

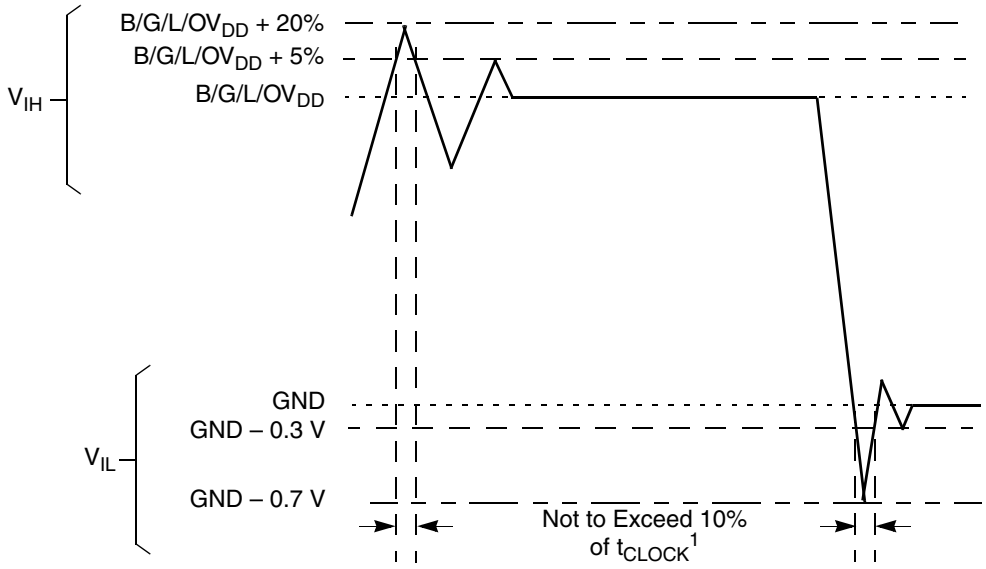
Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Note
PLL supply voltage		AV_{DD}_CORE0 AV_{DD}_CORE1 AV_{DD}_DDR AV_{DD}_PLAT $SDAV_{DD}$	1.0 ± 50 mV	V	—
Core power supply for SerDes transceivers		SV_{DD}	1.0 ± 50 mV	V	—
Pad power supply for SerDes transceivers and PCI Express		XV_{DD}	1.0 ± 50 mV	V	—
DDR3 DRAM I/O voltage		GV_{DD}	1.5 V ± 75 mV DDR3 1.35 V ± 67.5 mV DDR3L	—	—
Three-speed Ethernet I/O voltage (TSEC)		LV_{DD}	2.5 V ± 125 mV	V	—
DUART, system control and power management, I^2C, GPIO x8, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	—
Enhanced local bus I/O and GPIO x8 voltage		BV_{DD}	3.3 V ± 165 mV 1.8 V ± 90 mV	V	—
USB, eSPI		OV_{DD}	3.3 V ± 165 mV	V	—
Input voltage	DDR3 DRAM signals	MV_{IN}	GND to GV_{DD}	V	—
	DDR3 DRAM reference	MV_{REF}	GND to $GV_{DD}/2$	V	—
	Three-speed Ethernet signals	LV_{IN}	GND to LV_{DD}	V	—
	Enhanced local bus signals	BV_{IN}	GND to BV_{DD}	V	—
	DUART, DDRCLK, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	—
	USB, eSPI	OV_{IN}	GND to OV_{DD}	V	—
Operational Temperature range		T_A/T_J	0 to 105 Commercial –40 to 105 Industrial	°C	2

Note:

1. **Caution:** Until V_{DD} reaches its recommended operating voltage, V_{DD} may exceed L/B/G/OV_{DD} by up to 0.7 V. If 0.7 V is exceeded, extra current will be drawn by the device.
2. Minimum temperature is specified with T_A; maximum temperature is specified with T_J.

The following figure shows the undershoot and overshoot voltages at the interfaces of the chip.



Note:
1. t_{CLOCK} refers to the clock period associated with the respective interface:
For I^2C and JTAG, t_{CLOCK} references SYSCLK.
For DDR, t_{CLOCK} references MCLK.
For TSEC, t_{CLOCK} references EC_GTX_CLK125.
For eLBC, t_{CLOCK} references LCLK.

Figure 7. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}$

The core voltage must always be provided at nominal 1.0 V (See Table 3 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The SDRAM interface uses a differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$). The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

3.1.3 Output Driver Characteristics

The following table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage	Note
Enhanced local bus interface, GPIO[0:7]	45	BV_{DD} = 3.3 V BV_{DD} = 1.8 V	—
DDR3 signal (Programmable)	16 32 (half strength mode)	GV_{DD} = 1.5 V DDR3 GV_{DD} = 1.35 V DDR3L	1

Table 4. Output Drive Capability (continued)

Driver Type	Output Impedance (Ω)	Supply Voltage	Note
TSEC signals	45	LV_{DD} = 2.5 V	—
DUART, system control, JTAG	45	OV_{DD} = 3.3 V	—
I^2C	45	OV_{DD} = 3.3 V	—
USB, eSPI	45	OV_{DD} = 3.3 V	—

Notes:
1. The drive strength of the DDR3 interface in half-strength mode is at T_j = 105°C and at GV_{DD} (min).

3.2 Power Sequencing

The chip requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up when POWER_EN is not used to control switchable supplies:

1. VDD, VDDC, AVDD_CORE0, AVDD_CORE1, AVDD_PLAT, AVDD_DDR, BVDD, LVDD, OVDD, SDAVDD, SVDD and XVDD
2. GVDD

The requirements are as follows for power up when POWER_EN is used to control switchable supplies:

1. Always ON supply: VDDC, AVDD_CORE0, AVDD_PLAT, AVDD_DDR, BVDD, LVDD, OVDD, SDAVDD, SVDD and XVDD
– Wait for POWER_EN to assert
2. Switchable supply: VDD, AVDD_CORE1
3. GVDD

The core 1 power supplies (VDD and AVDD_CORE1) can be turned on as the result of POWER_EN assertion.

There is no ordering requirement between steps 2 and 3 as there is no relationship between the core 1 power supplies and the DRAM controller or interface; they may occur in any order or simultaneously.

POWER_EN pin is muxed with GPIO02 pin.

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for GV_{DD} is not required.

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

3.3 Power Characteristics

The following table shows the power dissipations of the VDD, VDDC, and SVDD supply for various operating platform clock frequencies versus the core and DDR clock frequencies.

Table 5. Core Power Dissipation

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	DDR Data Rate (MHz)	V_{DD}, V_{DDC}, S_{VDD} (V)	Junction Temp (°C)	Power (W)			Total Core and Platform Power (W)[1]	Notes
						VDD	VDDC	SVDD		
Typical	2x500	320	640	1.0	65	0.16	1.83	0.2	2.19	2, 3
Thermal					105	0.26	3.00	0.2	3.46	5, 7
Maximum					105	0.28	3.07	0.2	3.55	4, 6, 7

Notes:
1) Combined power of VDDC, VDD and SVDDx with DDR Controller and all Serdes banks active. Does not include I/O power.
2) Typical power assumes Dhrystone running with activity factor of 80% (on all cores) and executing DMA on the platform with 90% activity factor
3) Typical power is based on nominal processed device.
4) Maximum power assumes Multicore Dhrystone activity factor at 100% and executing DMA on the platform at 100% activity factor.
5) Thermal power assumes Multicore Dhrystone activity factor of 80% and executing DMA on the platform with 90% activity factor.
6) Maximum power is provided for power supply design sizing.
7) Thermal and Maximum power are based on worst case processed device.

3.3.1 I/O DC Power Supply Recommendation

The following table provides estimated I/O power numbers for each block: DDR, PCIe, eLBC, TSEC, SGMII, USB, eSPI, DUART, I^2C and GPIO.

Table 6. I/O Power Supply Estimated Values

Interface	Parameter	Symbol	Typical	Maximum	Unit	Note
DDR3	667 MHz data rate	GV_{DD} (1.5V)	0.493	0.517	W	1,2,3
	800 MHz data rate	GV_{DD} (1.5V)	0.509	0.532	W	1,2,3
DDR3L	667 MHz data rate	GV_{DD} (1.35V)	0.399	0.419	W	1,2,3
	800 MHz data rate	GV_{DD} (1.35V)	0.412	0.431	W	1,2,3
PCI Express	x2, 2.5 G-baud	SV_{DD} (1.0V)	0.167	0.18	W	1,2,3
SGMII	x1, 1.25G-baud	SV_{DD} (1.0V)	0.134	0.146	W	1,2,3
eLBC	16-bit, 75 MHz	BV_{DD} (1.8V)	0.008	0.023	W	1,2,3
		BV_{DD} (3.3V)	0.019	0.046	W	1,2,3
TSEC	RMII, RGMII, 1588	LV_{DD} (2.5V)	0.059	0.072	W	1,2,3,4
USB		OV_{DD} (3.3V)	0.125	0.135	W	1,2,3

Table 6. I/O Power Supply Estimated Values (continued)

Interface	Parameter	Symbol	Typical	Maximum	Unit	Note
eSPI		OV_{DD} (3.3V)	0.002	0.005	W	1,2,3
I^2C		OV_{DD} (3.3V)	0.001	0.004	W	1,2,3
DUART		OV_{DD} (3.3V)	0.003	0.006	W	1,2,3
GPIO [0:7]	x8	OV_{DD} (3.3V)	0.002	0.004	W	1,2,3,5
GPIO [8:15]	x8	BV_{DD} (1.8V)	0.001	0.002	W	1,2,3,5
		BV_{DD} (3.3V)	0.002	0.004	W	1,2,3,5
Others	Clocking, Debug, DFT, EPIC, IOVSEL, JTAG, Power Mgt, Sys Control	OV_{DD} (3.3V)	0.014	0.033	W	1,2,3

Notes:
1. The maximum value is dependent on actual use case such as what application, external components used, environmental conditions such as temperature voltage and frequency. This is not intended to be the maximum guaranteed current. Depending on use case different result is expected.
2. The typical value are estimates based on simulations at nominal recommended core voltage (V_{DD}) and assuming 65 C junction temperature.
3. The maximum value are estimates based on simulations at nominal recommended core voltage (V_{DD}) and assuming 105 C junction temperature.
4. The current values are per each TSEC used.
5. GPIO x8 support on OVDD and x8 on BVDD rail supply.

3.4 Input Clocks

3.4.1 System Clock Timing

The following table provides the system clock (SYSCLK) DC specifications for the chip.

Table 7. SYSCLK DC Electrical Characteristics (OV_{DD} = 3.3 V ± 165 mV)

Parameter	Symbol	Min	Typical	Max	Unit	Note
High-level input voltage	V_{IH}	2.0	—	—	V	1
Low-level input voltage	V_{IL}	—	—	0.8	V	2
Input Capacitance	C_{IN}	—	7	15	pf	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DD})	I_{IN}	—	—	±50	μA	2

Note:
1. The max V_{IH}, and min V_{IL} values can be found in Table 3
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced inTable 3

The following table provides the system clock (SYSCLK) AC timing specifications for the chip.

Table 8. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 3) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
SYSCLK frequency	f_{SYSCLK}	64	—	100	MHz	1
SYSCLK cycle time	t_{SYSCLK}	10	—	15.6	ns	—
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	2
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	± 150	ps	—
SYSCLK jitter phase noise at – 56dBc	—	—	—	500	KHz	4
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Notes:
1. **Caution:** The CCB_clk to SYSCLK ratio and e500v2dp core to CCB_clk ratio settings must be chosen such that the resulting SYSCLK frequency, e500v2dp core frequency, and CCB_clk frequency do not exceed their respective maximum or minimum operating frequencies.Refer to the Design Checklist for ratio settings.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate as measured from +/- 0.3 ΔV_{AC} at center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

3.4.2 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 9 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the chip's input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the chip is compatible with spread spectrum sources if the recommendations listed in Table 9 are observed.

Table 9. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 3.

Parameter	Min	Max	Unit	Note
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	1, 2

Note:
1. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 8.
2. Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device

CAUTION

The processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500v2dp core frequency should avoid violating the stated limits by using down-spreading only.

3.4.3 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500v2dp. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

3.4.4 TSEC Gigabit Reference Clock Timing

The following table lists the TSEC gigabit reference clock DC electrical characteristics for the chip.

Table 10. TSEC Gigabit Reference Clock DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
High-level input voltage	V_{IH}	1.7	—	V	1
Low-level input voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = LV_{DD})	I_{IH}	—	25	μA	2
Input current (V_{IN} = GND)	I_{IL}	–15	—	μA	2

Note:
1. The max V_{IH}, and min V_{IL} values can be found in Table 3
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 3

The following table provides the TSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the chip.

Table 11. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK rise and fall time LV_{DD} = 2.5V	t_{G125R}/t_{G125F}	—	—	0.75	ns	1
EC_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	47	—	53	%	2
EC_GTX_CLK125 total jitter	—	—	—	+/– 150	ps	2

Notes:
1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5V and 2.0V for LV_{DD}=2.5V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the TSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the TSEC GTX_CLK. See Section 3.10.1.2.3, “RGMII AC Timing Specifications” for duty cycle for 10Base-T and 100Base-T reference clock.

3.4.5 DDR Clock Timing

The following table provides the system clock (DDRCLK) DC specifications for the chip.

Table 12. DDRCLK DC Electrical Characteristics (OV_{DD} = 3.3 V ± 165 mV)

Parameter	Symbol	Min	Typical	Max	Unit	Note
High-level input voltage	V_{IH}	2.0	—	OV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	—	0.8	V	—
Input Capacitance	C_{IN}	—	7	15	pf	—
Input current (V_{IN} = 0 V or V_{IN} = V_{DD})	I_{IN}	—	—	±50	μA	1

Note:

1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

The following table provides the DDR clock (DDRCLK) AC timing specifications for the chip.

Table 13. DDRCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
DDRCLK frequency	f_{DDRCLK}	64	—	100	MHz	1, 2
DDRCLK cycle time	t_{DDRCLK}	10	—	15.6	ns	1, 2
DDRCLK duty cycle	t_{KHK}/t_{DDRCLK}	40	—	60	%	2
DDRCLK slew rate	—	1	—	4	V/ns	3
DDRCLK peak period jitter	—	—	—	± 150	ps	—
DDRCLK jitter phase noise at – 56dBc	—	—	—	500	KHz	4
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Notes:

1. **Caution:** The DDR complex clock to DDRCLK ratio settings must be chosen such that the resulting DDR complex clock frequency does not exceed the maximum or minimum operating frequencies. Refer to the Design Checklist for ratio settings.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate as measured from +/- 0.3 ΔV_{AC} at center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

3.4.6 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes and TSEC, see the specific section of this document.

3.5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the chip. The following table provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 14. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$	25	—	μs	—
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	μs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1, 2

Notes:
1. SYSCLK is the primary clock input for the chip.
2. $\overline{\text{HRESET}}$ should have a rise time of no more than one sysclk cycle.

The following table provides the PLL lock times.

Table 15. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

3.6 Power-on Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum Power-On Ramp Rate is required to avoid falsely triggering the ESD circuitry. The following table provides the power supply ramp rate specifications.

Table 16. Power Supply Ramp Rate

Parameter	Min	Max	Unit	Note
Required ramp rate for all voltage supplies (including OVDD/XVDD/ GVDD/BVDD/SVDD/LVDD, All VDD supplies, MVREF and all AVDD supplies.)	—	36000	Volts/Sec	1,2

Note:
1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (e.g. exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range Table 3.

3.7 DDR3 and DDR3L SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR3 and DDR3L SDRAM controller interface of the chip. Note that the required GV_{DD}(typ) voltage is 1.5 V or 1.35 V when interfacing to DDR3 or DDR3L SDRAM respectively.

3.7.1 DDR3 and DDR3L SDRAM Interface DC Electrical Characteristics

The following table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 17. DDR3 SDRAM Interface DC Electrical Characteristics

At recommended operating condition with GV_{DD} = 1.5 V[1].

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MV_{REF} + 0.100	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MV_{REF} – 0.100	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed the MV_{REF} DC level by more than ±1% of GV_{DD} (i.e. ±15 mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MV_{REF} with a min value of MV_{REF} – 0.04 and a max value of MV_{REF} + 0.04. V_{TT} should track variations in the DC level of MV_{REF}.
4. The voltage regulator for MVREFn must meet the specifications stated in Table 20.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

The following table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 18. DDR3L SDRAM Interface DC Electrical Characteristics

At recommended operating condition with GV_{DD} = 1.35 V1.

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MVREFn	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MVREFn + 0.090	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MVREFn – 0.090	V	5

Table 18. DDR3L SDRAM Interface DC Electrical Characteristics (continued)

At recommended operating condition with GV_{DD} = 1.35 V1.

Parameter	Symbol	Min	Max	Unit	Note
Output high current (V_{OUT} = 0.963 V)	I_{OH}	—	–12.8	mA	6, 7
Output low current (V_{OUT} = 0.320 V)	I_{OL}	12.8	—	mA	6, 7
I/O leakage current	I_{OZ}	–50	50	μA	8

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed the MV_{REF} DC level by more than ±1% of GV_{DD} (i.e. ±13.5 mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MV_{REF} with a min value of MV_{REF} – 0.04 and a max value of MV_{REF} + 0.04. V_{TT} should track variations in the DC level of MV_{REF}.
4. The voltage regulator for MV_{REF} must meet the specifications stated in Table 20.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. I_{OH} and I_{OL} are measured at GV_{DD} = 1.283 V.
7. Refer to the IBIS model for the complete output IV curve characteristics.
8. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

The following table provides the DDR controller interface capacitance for DDR3 and DDR3L.

Table 19. DDR3 and DDR3L SDRAM Capacitance

At recommended operating conditions with GV_{DD} of 1.5 V ± 5%.for DDR3 or 1.35 V ± 5%.for DDR3L

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	

The following table provides the current draw characteristics for MV_{REF}.

Table 20. Current Draw Characteristics for MV_{REF}

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Current draw for DDR3 SDRAM for MV_{REF}	MV_{REF}	—	1250	μA	—
Current draw for DDR3L SDRAM for MV_{REF}	MV_{REF}	—	1150	μA	—

3.7.2 DDR3 and DDR3L SDRAM Interface AC Timing Specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports both DDR3 and DDR3L memories. Note that the required GV_{DD}(typ) voltage is 1.5 V or 1.35 V when interfacing to DDR3 or DDR3L SDRAM respectively.

3.7.2.1 DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications

The following table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 21. DDR3 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GVDD of 1.5 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{ILAC}	—	MV_{REF} – 0.175	V	—
AC input high voltage	V_{IHAC}	MV_{REF} + 0.175	—	V	—

The following table provides the input AC timing specifications for the DDR controller when interfacing to DDR3L SDRAM.

Table 22. DDR3L SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GVDD of 1.35 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{ILAC}	—	MV_{REF} – 0.135	V	—
AC input high voltage	V_{IHAC}	MV_{REF} + 0.135	—	V	—

The following table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 and DDR3L SDRAM.

Table 23. DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.5 V ± 5%.for DDR3 or 1.35 V ± 5%.for DDR3L.

Parameter	Symbol	Min	Max	Unit	Note
Controller Skew for MDQS 800 MHz data rate 667 MHz data rate	t_{CISKEW}	 –350 –390	 350 390	ps	1
Tolerated Skew for MDQS 800 MHz data rate 667 MHz data rate	t_{DISKEW}	 –275 –360	 275 360	ps	2

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

The following figure shows the DDR3 and DDR3L SDRAM interface input timing diagram.

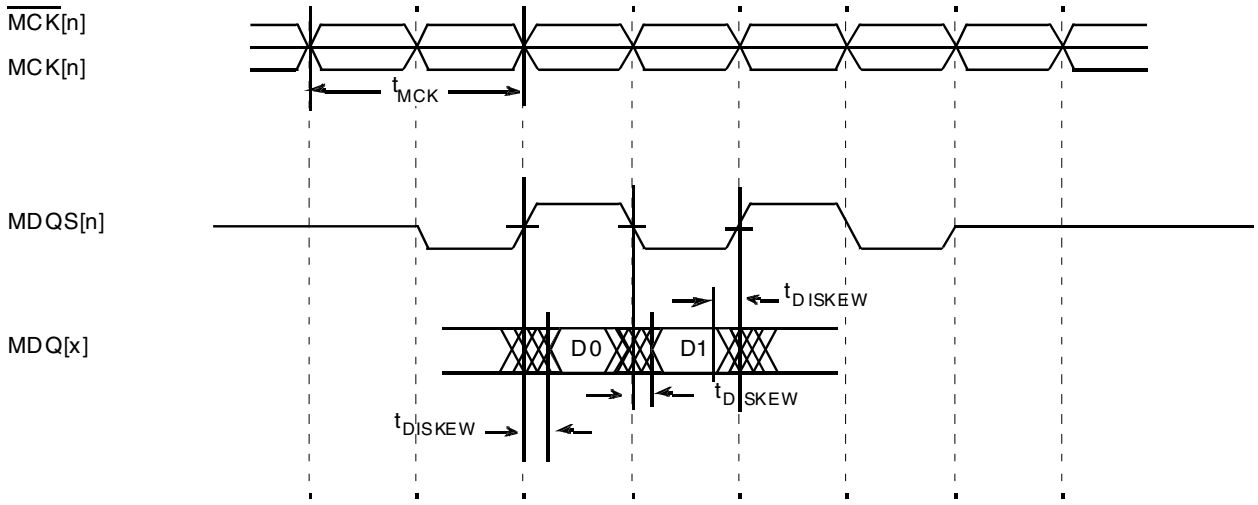


Figure 8. DDR3 and DDR3L SDRAM Interface Input Timing Diagram

3.7.2.2 DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications

The following table contains the output AC timing targets for the DDR3 and DDR3L SDRAM interface.

Table 24. DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.5 V ± 5%.for DDR3 or 1.35 V ± 5%.for DDR3L

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK[n] cycle time	t_{MCK}	2.5	5	ns	2
ADDR/CMD output setup with respect to MCK 800 MHz data rate 667 MHz data rate	t_{DDKHAS}	 0.767 0.950	 — —	ns	3
ADDR/CMD output hold with respect to MCK 800 MHz data rate 667 MHz data rate	t_{DDKHAX}	 0.767 0.950	 — —	ns	3
$\overline{MCS}$[n] output setup with respect to MCK 800 MHz data rate 667 MHz data rate	t_{DDKHCS}	 0.767 0.950	 — —	ns	3
$\overline{MCS}$[n] output hold with respect to MCK 800 MHz data rate 667 MHz data rate	t_{DDKHCX}	 0.767 0.950	 — —	ns	3
MCK to MDQS Skew 800 MHz data rate 667 MHz data rate	t_{DDKHMH}	 –0.525 –0.625	 0.525 0.625	ns	4

Table 24. DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.5 V ± 5%.for DDR3 or 1.35 V ± 5%.for DDR3L

Parameter	Symbol[1]	Min	Max	Unit	Note
MDQ/MDM output setup with respect to MDQS 800 MHz data rate 667 MHz data rate	t_{DDKHDS}, t_{DDKLDS}	 225 300	 — —	ps	5
MDQ/MDM output hold with respect to MDQS 800 MHz data rate 667 MHz data rate	t_{DDKHDX}, t_{DDKLDX}	 225 300	 — —	ps	5
MDQS preamble	t_{DDKHMP}	$0.9 \times t_{MCK}$	—	ns	—
MDQS postamble	t_{DDKHME}	$0.4 \times t_{MCK}$	$0.6 \times t_{MCK}$	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ and MCDQS/$\overline{\text{MCDQS}}$ referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the chip reference manual for a description and explanation of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ) or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.

NOTE

For the ADDR/CMD setup and hold specifications in Table 24, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

The following figure shows the DDR3 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

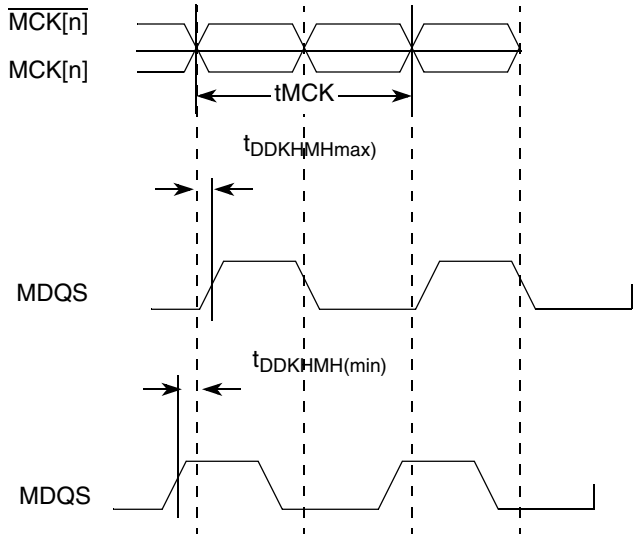


Figure 9. t_{DDKHMH} Timing Diagram

The following figure shows the DDR3 and DDR3L SDRAM output timing diagram.

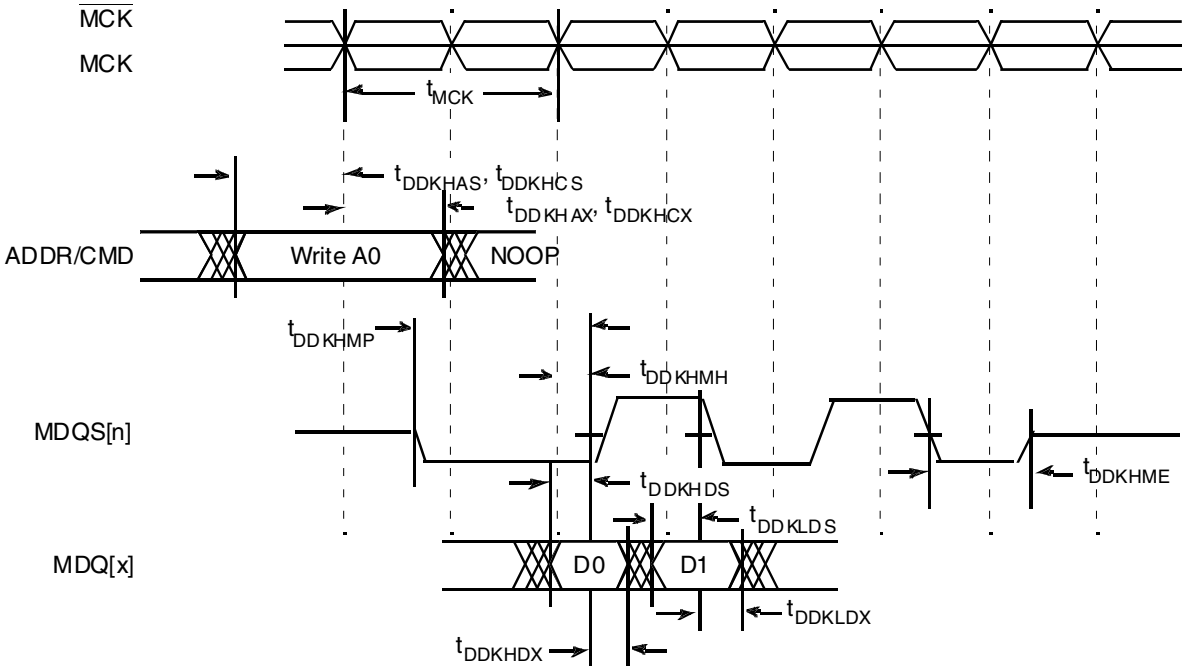


Figure 10. DDR3 and DDR3L Output Timing Diagram

The following figure provides the AC test load for the DDR3 and DDR3L controller bus.

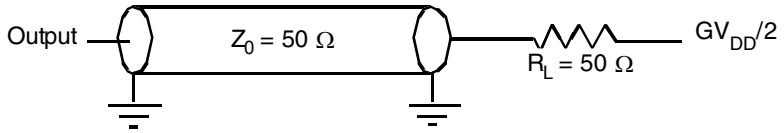


Figure 11. DDR3 and DDR3L Controller Bus AC Test Load

3.7.2.3 DDR3 and DDR3L SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR3 and DDR3L SDRAM controller interface. The following figure shows the differential timing specification.

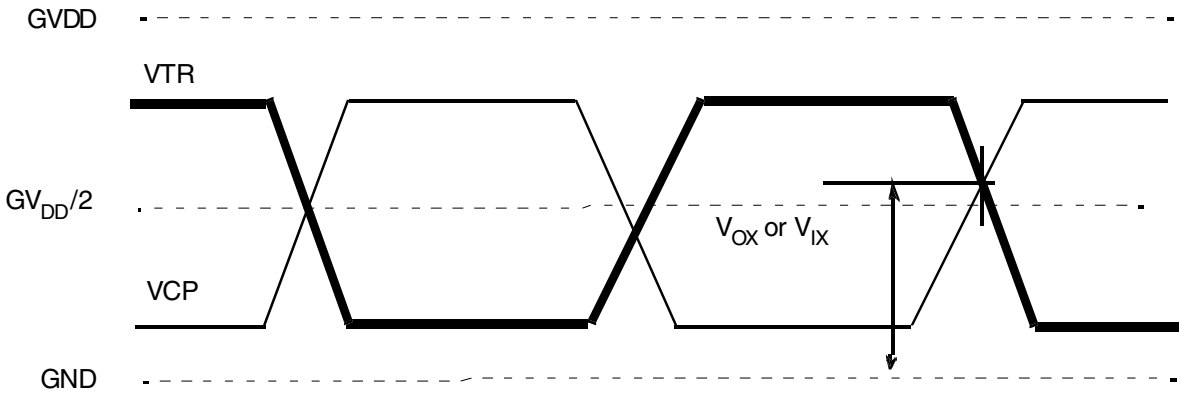


Figure 12. DDR3 and DDR3L SDRAM Differential Timing Specifications

NOTE

VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as $\overline{\text{MCK}}$ or $\overline{\text{MDQS}}$).

The following table provides the DDR3 differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 25. DDR3 SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Input AC Differential Cross-Point Voltage	V_{IXAC}	0.5 × GVDD – 0.150	0.5 × GVDD + 0.150	V	—
Output AC Differential Cross-Point Voltage	V_{OXAC}	0.5 × GVDD – 0.115	0.5 × GVDD + 0.115	V	—

The following table provides the DDR3L differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 26. DDR3L SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Input AC Differential Cross-Point Voltage	V_{IXAC}	0.5 × GVDD – 0.135	0.5 × GVDD + 0.135	V	—
Output AC Differential Cross-Point Voltage	V_{OXAC}	0.5 × GVDD – 0.105	0.5 × GVDD + 0.105	V	—

3.8 eSPI

This section describes the DC and AC electrical specifications for the eSPI of the chip.

3.8.1 eSPI DC Electrical Characteristics

The following table provides the DC electrical characteristics for the device eSPI.

Table 27. eSPI DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current ($0 V \le V_{IN} \le OV_{DD}$)	I_{IN}	—	+40	μA	2
Output high voltage (I_{OH} = –6.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (I_{OL} = 6.0mA)	V_{OL}	—	0.5	V	—
Output low voltage (IOL = 3.2mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Section 3.1.2, “Recommended Operating Conditions”.

3.8.2 eSPI AC Timing Specifications

The following table provides the eSPI input and output AC timing specifications.

Table 28. eSPI AC Timing Specifications[1]

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Min	Max	Unit	Note
SPI outputs—Master data (internal clock) hold time	t_{NIKHOX}	0.5 + (t_{plb_clk} * SPMODE[HO_ADJ])	—	ns	2, 3
SPI outputs—Master data (internal clock) delay	t_{NIKHOV}	—	6.0 + (t_{plb_clk} * SPMODE[HO_ADJ])	ns	2, 3
SPI_CS outputs—Master data (internal clock) hold time	$t_{NIKHOX2}$	0	—	ns	2
SPI_CS outputs—Master data (internal clock) delay	$t_{NIKHOV2}$	—	6.0	ns	2
SPI inputs—Master data (internal clock) input setup time	t_{NIIVKH}	5	—	ns	4
SPI inputs—Master data (internal clock) input hold time	t_{NIIXKH}	0	—	ns	4

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
3. See the chip reference manual for details about SPMODE[HO_ADJ] setting. t_{plb_clk} is the platform (CCB) clock.
4. For Windbond flash dual-output mode both SPI_MOSI and SPI_MISO are inputs.

The following figure provides the AC test load for the eSPI.

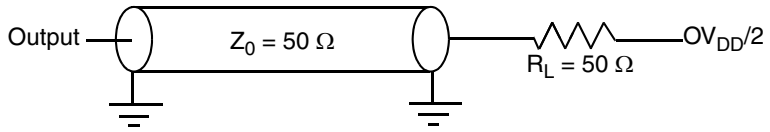


Figure 13. eSPI AC Test Load

The following figure represents the AC timing from Table 28 in master mode (internal clock). (It applies when SPMODEx[CIx]=0, SPMODEx[CPx]=0.) Note that the clock edge is selectable on eSPI.

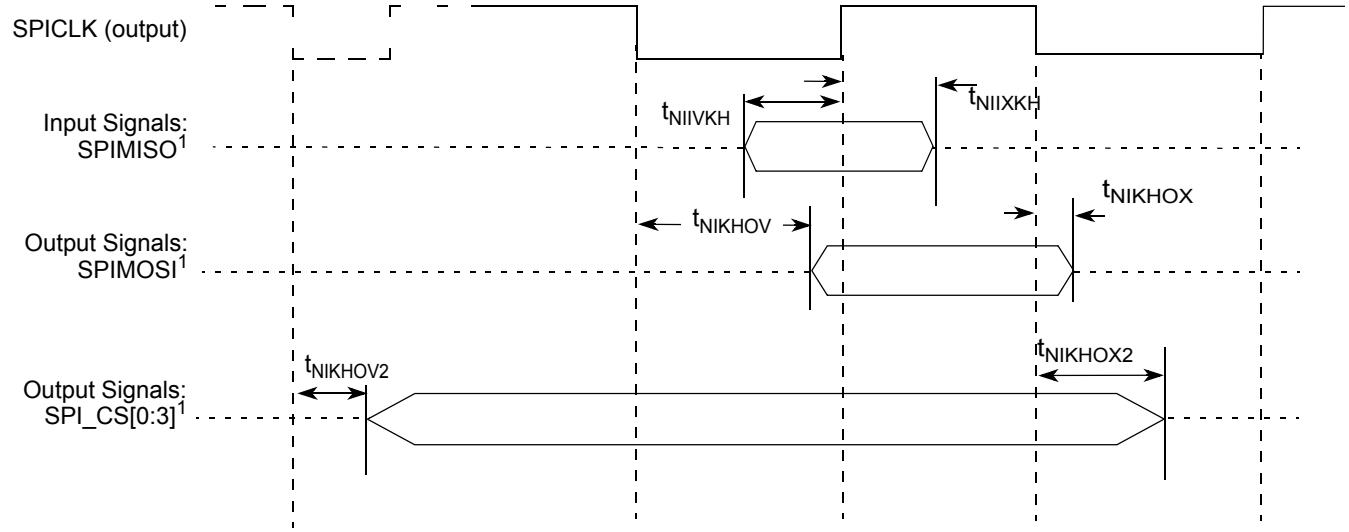


Figure 14. eSPI AC Timing in Master Mode (Internal Clock) Diagram

3.9 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the chip.

3.9.1 DUART DC Electrical Characteristics

The following table provides the DC electrical characteristics for the DUART interface.

Table 29. DUART DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = mn, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—

Table 29. DUART DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Figure 3.
2. Note that the symbol OV_{IN} represents the input voltage of the supply. It is referenced in Figure 3.

3.9.2 DUART AC Electrical Specifications

Table 30 provides the AC timing parameters for the DUART interface.

Table 30. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	CCB clock/1,048,576	baud	1
Maximum baud rate	CCB clock/16	baud	2
Oversample rate	16	—	3

Notes:
1. CCB clock refers to the platform clock.
2. Actual attainable baud rate will be limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

3.10 Ethernet: Three-Speed Ethernet (TSEC)

This section provides the AC and DC electrical characteristics for three-speed Ethernet10/100/1000 controller and Ethernet management interface.

3.10.1 RMII/RGMII Interface Electrical Specifications

This section provides the AC and DC electrical characteristics of RMII/RGMII interface for TSEC.

3.10.1.1 RMII/RGMII DC Electrical Specifications

The following table shows the RMII/RGMII DC electrical characteristics when operating from a 2.5 V supply.

Table 31. RMII/RGMII DC Electrical Characteristics (2.5V)

At recommended operating conditions with LV_{DD} = 2.5 V.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.70	V	—
Input high current (V_{IN} = LV_{DD})	I_{IH}	—	25	μA	—

Table 31. RMII/RGMII DC Electrical Characteristics (2.5V) (continued)

At recommended operating conditions with LV_{DD} = 2.5 V.

Parameter	Symbol	Min	Max	Unit	Note
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	1
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 3.

3.10.1.2 RMII/RGMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications and then the RGMII AC timing specifications.

3.10.1.2.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in Table 32.

Table 32. RMII Transmit AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
TSEC*n*_TX_CLK clock period	t_{RMT}	—	20.0	—	ns
TSEC*n*_TX_CLK duty cycle	t_{RMTH}	35	—	65	%
TSEC*n*_TX_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time TSEC*n*_TX_CLK (20%–80%)	t_{RMTR}	1.0	—	5.0	ns
Fall time TSEC*n*_TX_CLK (80%–20%)	t_{RMTF}	1.0	—	5.0	ns
TSEC*n*_TX_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns

Figure 15 shows the RMII transmit AC timing diagram.

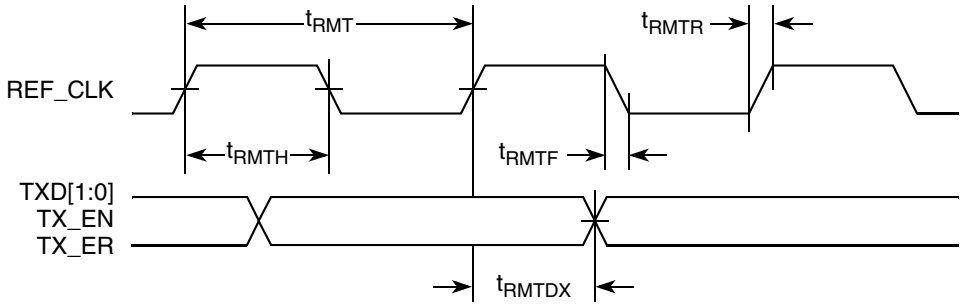


Figure 15. RMII Transmit AC Timing Diagram

3.10.1.2.2 RMII Receive AC Timing Specifications

The following table lists the RMII receive AC timing specifications.

Table 33. RMII Receive AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
TSEC*n*_RX_CLK clock period	t_{RMR}	—	20.0	—	ns
TSEC*n*_RX_CLK duty cycle	t_{RMRH}	35	—	65	%
TSEC*n*_RX_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time TSEC*n*_RX_CLK (20%–80%)	t_{RMRR}	1.0	—	5.0	ns
Fall time TSEC*n*_RX_CLK (80%–20%)	t_{RMRF}	1.0	—	5.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to TSEC*n*_RX_CLK rising edge	t_{RMRDV}	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to TSEC*n*_RX_CLK rising edge	t_{RMRDX}	2.0	—	—	ns

The following figure provides the AC test load for TSEC.

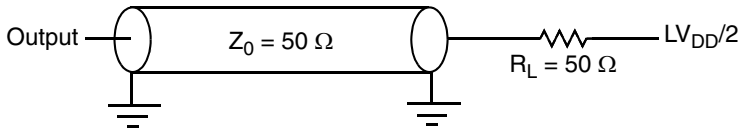


Figure 16. TSEC AC Test Load

The following figure shows the RMII receive AC timing diagram.

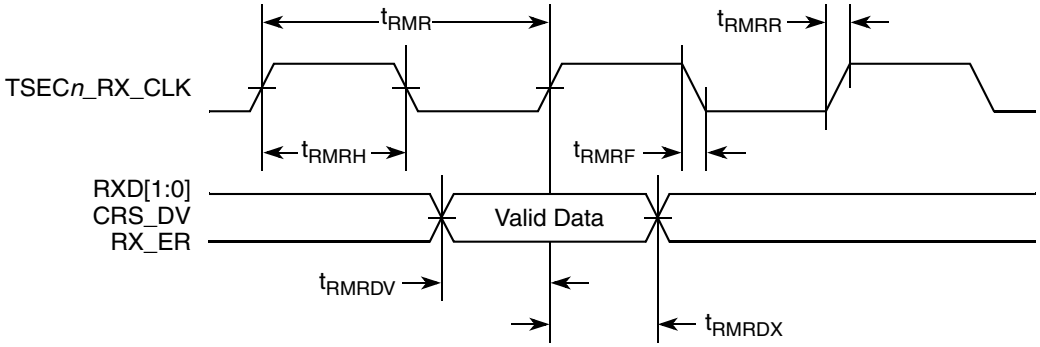


Figure 17. RMII Receive AC Timing Diagram

3.10.1.2.3 RGMII AC Timing Specifications

The following table presents the RGMII AC timing specifications.

Table 34. RGMII AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Typ	Max	Unit	Note
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–500	0	500	ps	—
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	—	2.6	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	—
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns	—
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns	—

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.

The following figure shows the RGMII AC timing and multiplexing diagrams.

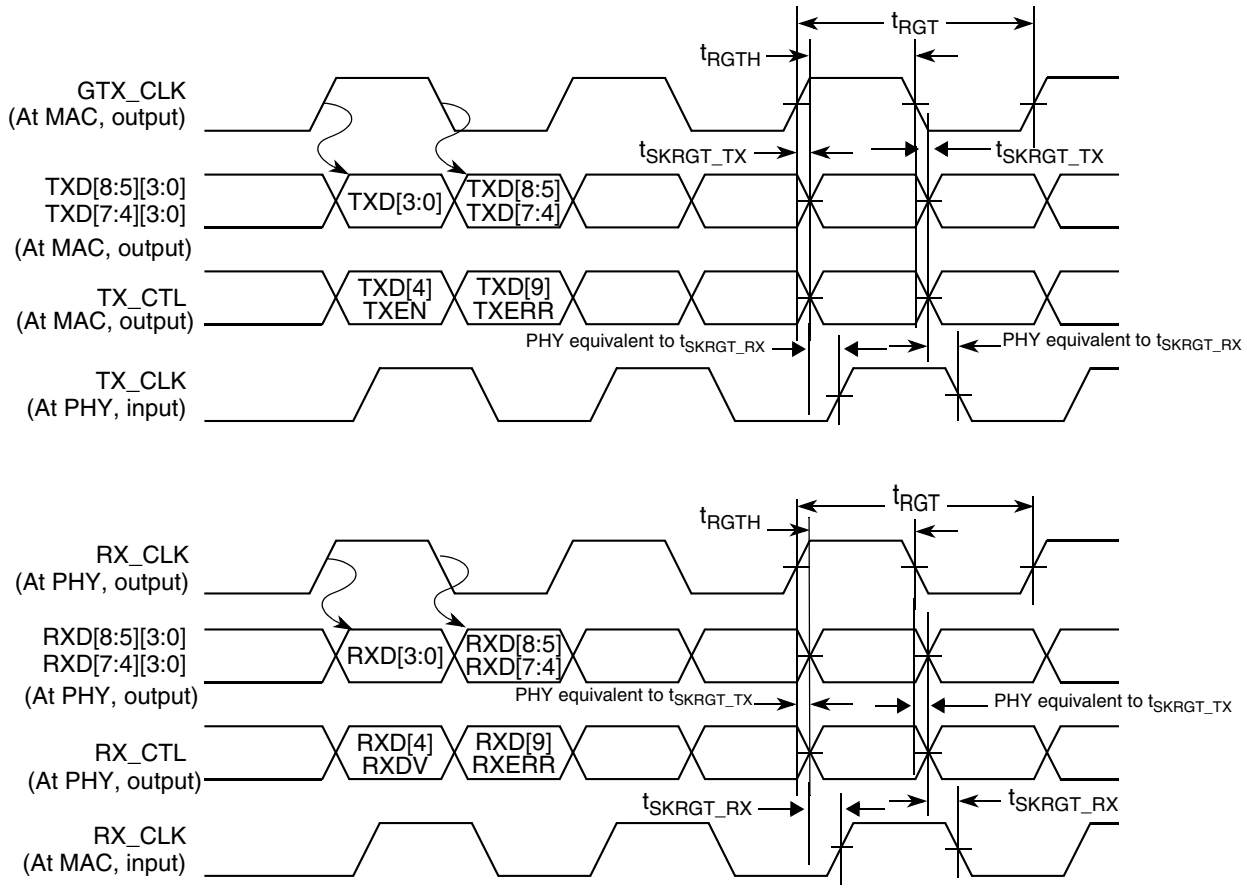


Figure 18. RGMII AC Timing and Multiplexing Diagrams

WARNING

Freescale guarantees timings generated from the MAC. Board designers must ensure delays needed at the PHY or the MAC.

3.10.2 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-Coupled serial link from the dedicated SerDes interface of P1023 as shown in Figure 20, where C_{TX} is the external (on board) AC-Coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to SGND. The reference circuit of the SerDes transmitter and receiver is shown in Figure 43.

3.10.2.1 SGMII DC Electrical Characteristics

This section discusses the electrical characteristics for the SGMII interface.

3.10.2.1.1 DC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 3.17.2.2, "DC Level Requirement for SerDes Reference Clocks."

3.10.2.1.2 SGMII Transmit DC Timing Specifications

The following table describe the SGMII SerDes transmitter AC-Coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TX[n] and $\overline{\text{SD}n\text{\_TX}}$[n]) as shown in Figure 20.

Table 35. SGMII DC Transmitter Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output high voltage	V_{OH}	—	—	$XV_{DD\text{-}Typ}/2 + \lvert V_{OD}\rvert_{\text{-}max}/2$	mV	1
Output low voltage	V_{OL}	$XV_{DD\text{-}Typ}/2 - \lvert V_{OD}\rvert_{\text{-}max}/2$	—	—	mV	1
Output differential voltage[2, 3, 4] ($XV_{DD\text{-}Typ}$ at 1.0V)	$\lvert V_{OD}\rvert$	304	475	689	mV	Equalization setting: 1.0x
		279	436	632		Equalization setting: 1.09x
		254	396	574		Equalization setting: 1.2x
		229	357	518		Equalization setting: 1.33x
		202	316	459		Equalization setting: 1.5x
		178	277	402		Equalization setting: 1.71x
		152	237	344		Equalization setting: 2.0x
Output impedance (single-ended)	R_O	40	50	60	Ω	—

Notes:

1. This will not align to DC-coupled SGMII. $XV_{DD\text{-}Typ}$=1.0V.
2. $\lvert V_{OD}\rvert = \lvert V_{SD2\_TXn} - V_{\overline{SD2\_TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{OD}\rvert$.
3. The $\lvert V_{OD}\rvert$ value shown in the table assumes the following transmit equalization setting in the XMITEQ**AB** (for SerDes lanes A & B) or XMITEQ**EF** (for SerDes lanes E & F) bit field of P1023's SerDes 2 Control Register:
   - The MSbit (bit 0) of the above bit field is set to zero (selecting the full $V_{DD\text{-}DIFF\text{-}p\text{-}p}$ amplitude - power up default);
   - The LSbits (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.
4. The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $XV_{DD\text{-}Typ}$=1.0V, no common mode offset variation (V_{OS} =500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TX[n] and SD_TX[n].

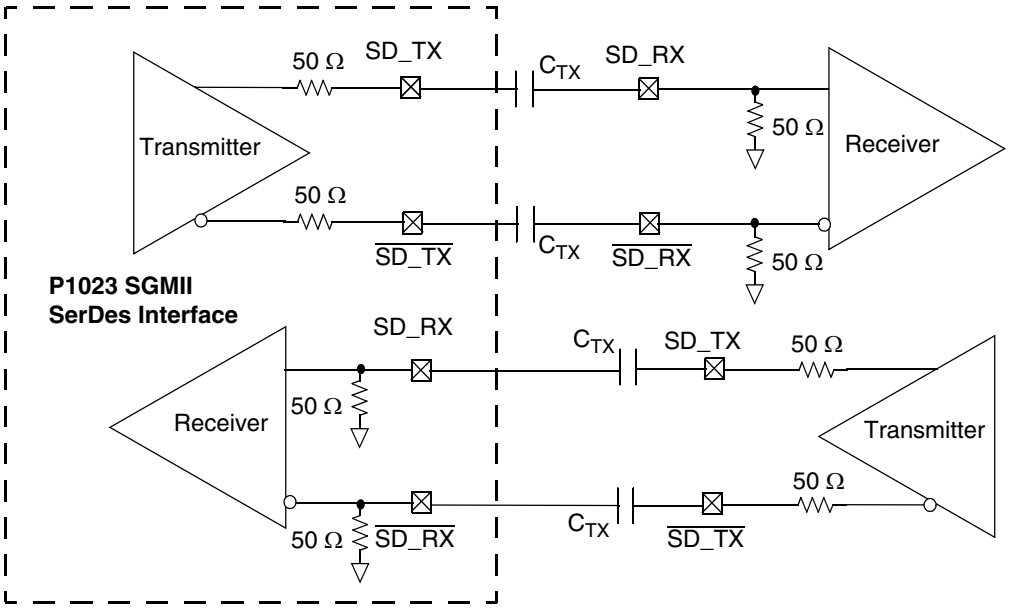


Figure 19. 4-Wire AC-Coupled SGMII Serial Link Connection Example

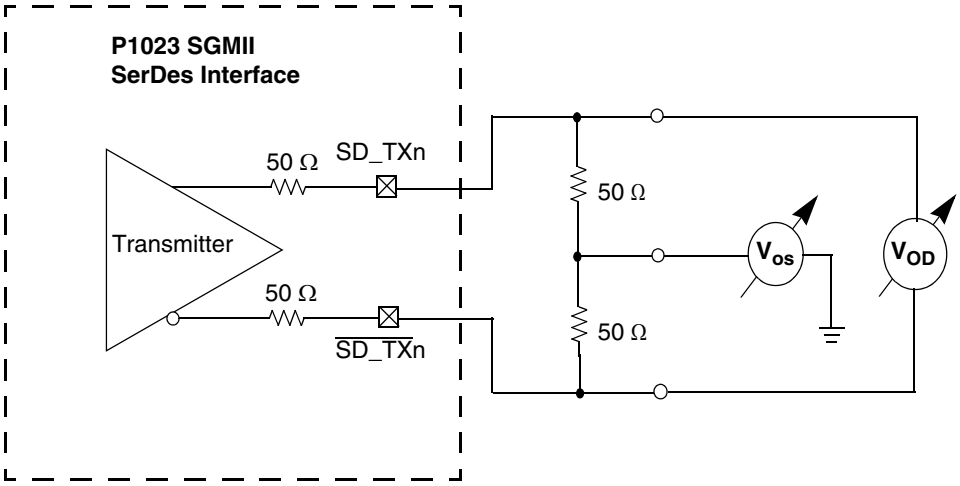


Figure 20. SGMII Transmitter DC Measurement Circuit

3.10.2.1.3 SGMII DC Receiver Timing Specification

The following table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 36. SGMII DC Receiver Electrical Characteristics[5]

For recommended operating conditions, see Table 3

Parameter		Symbol	Min	Typ	Max	Unit	Note
DC Input voltage range		—	N/A			—	1
Input differential voltage	LSTS = 0	$V_{RX\_DIFFp-p}$	100	—	1200	mV	2, 4
	LSTS = 1		175	—			
Loss of signal threshold	LSTS = 0	VLOS	30	—	100	mV	3, 4
	LSTS = 1		65	—	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	—	120	Ω	—

Note:

1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in PCI Express. Refer to PCI Express Differential Receiver (RX) Input Specifications section for further explanation.
4. The LSTS shown in the table refers to the LSTS**AB** or LSTS**EF** bit field of P1023's SerDes Control Register.
5. The supply voltage is 1.0 V.

3.10.2.2 SGMII AC Timing Specifications

This section describes the AC timing specifications for the SGMII interface.

3.10.2.2.1 AC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

Note that the SGMII clock requirements for SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are intended to be used within the clocking guidelines specified by Section 3.17.2.3, "AC Requirements for SerDes Reference Clocks".

3.10.2.2.2 SGMII Transmit AC Timing Specifications

The following table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter

Table 37. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.0V ± 50mV

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic Jitter	JD	—	—	0.17	UI p-p	—
Total Jitter	JT	—	—	0.35	UI p-p	—
Unit Interval	UI	799.92	800	800.08	ps	—

Notes:

1. Each UI is 800 ps ± 100 ppm.
2. See Figure 22 for single frequency sinusoidal jitter limits

3.10.2.2.3 SGMII AC Measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX[n] and $\overline{\text{SD\_TX}}$[n]) or at the receiver inputs (SD_RX[n] and $\overline{\text{SD\_RX}}$[n]) as depicted in the following figure, respectively.

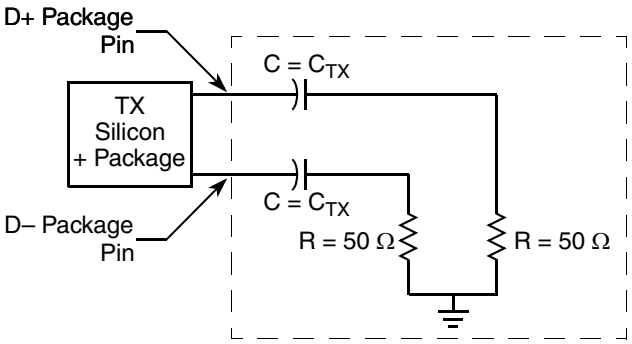


Figure 21. SGMII AC Test/Measurement Load

3.10.2.2.4 SGMII Receiver AC Timing Specifications

The following table provides the SGMII receive AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 38. SGMII Receive AC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.0V ± 50mV

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1, 2
Bit Error Ratio	BER	—	—	10^{-12}		—
Unit Interval	UI	799.92	800	800.08	ps	3

Notes:
1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. Refer to RapidIO™ 1x/4x LP Serial Physical Layer Specification for interpretation of jitter specifications.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 22.

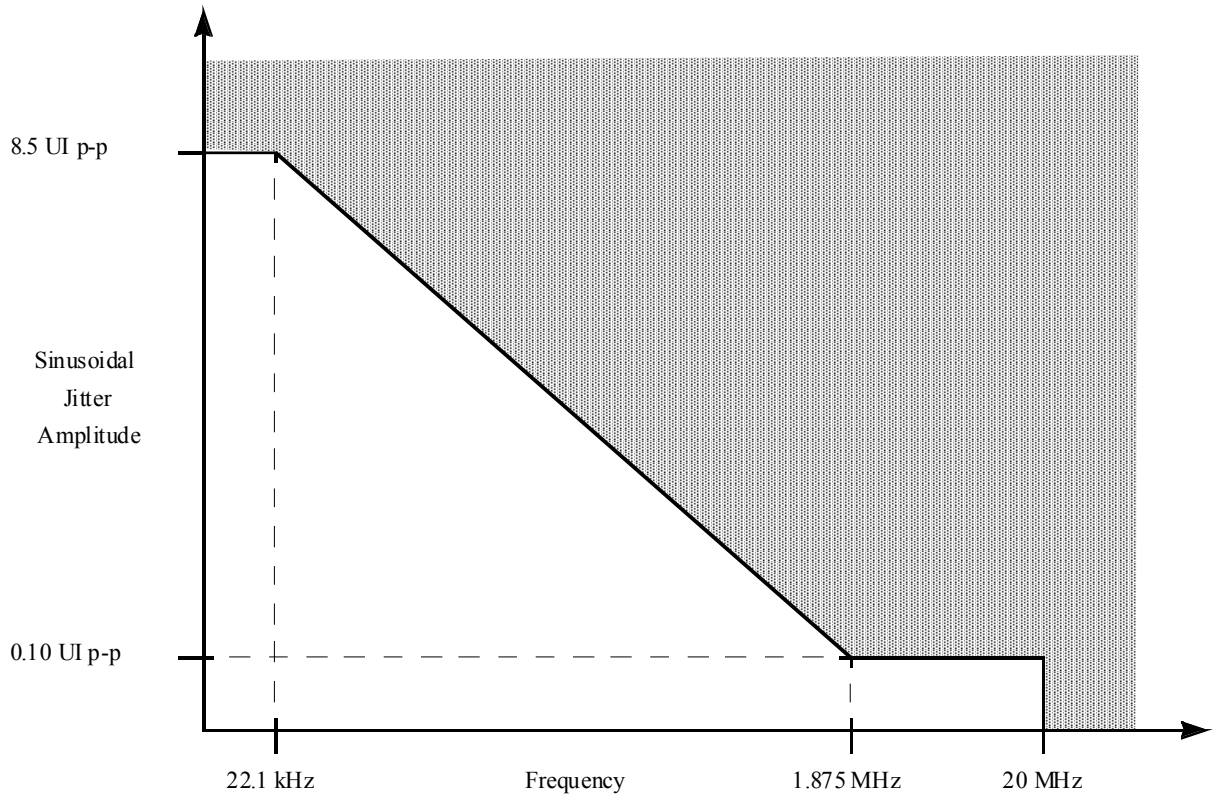


Figure 22. Single Frequency Sinusoidal Jitter Limits

3.10.3 Ethernet Management

3.10.3.1 Ethernet Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 2.5 V. The DC electrical characteristics for MDIO and MDC are provided in Table 39.

Table 39. Ethernet Management DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 2.5 V.

Parameter	Symbol	Min	Max	Unit	Note
Output high voltage (LV_{DD} = Min, IOH = –1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—
Input high voltage	V_{IH}	1.70	LV_{DD} + 0.3	V	—

Table 39. Ethernet Management DC Electrical Characteristics (continued)

At recommended operating conditions with LV_{DD} = 2.5 V.

Parameter	Symbol	Min	Max	Unit	Note
Input low voltage	V_{IL}	–0.3	0.70	V	—
Input high current (V_{IN} = LV_{DD},)	I_{IH}	—	25	μA	1, 2
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	—

Notes:
1. EC1_MDC and EC1_MDIO operate on LV_{DD}.
2. Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 3.

3.10.3.1.1 Ethernet Management AC Electrical Specifications

The following table provides the Ethernet management AC timing specifications.

Table 40. Ethernet Management AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(16 \times t_{plb\_clk}) - 3$	—	$(16 \times t_{plb\_clk}) + 3$	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns.
4. t_{plb_clk} is the platform (CCB) clock.

The following figure shows the Ethernet management interface timing diagram.

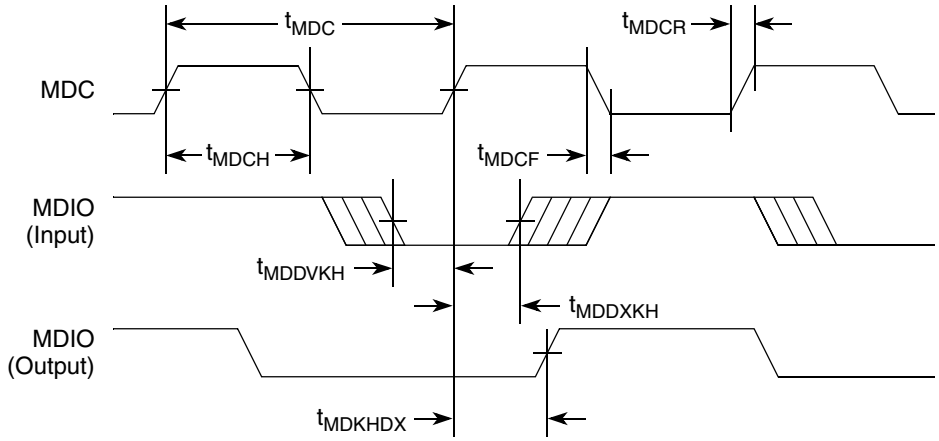


Figure 23. Ethernet Management Interface Timing Diagram

3.10.4 TSEC IEEE 1588 AC Specifications

The following table provides the IEEE 1588 AC timing specifications.

Table 41. TSEC IEEE 1588 AC Timing Specifications

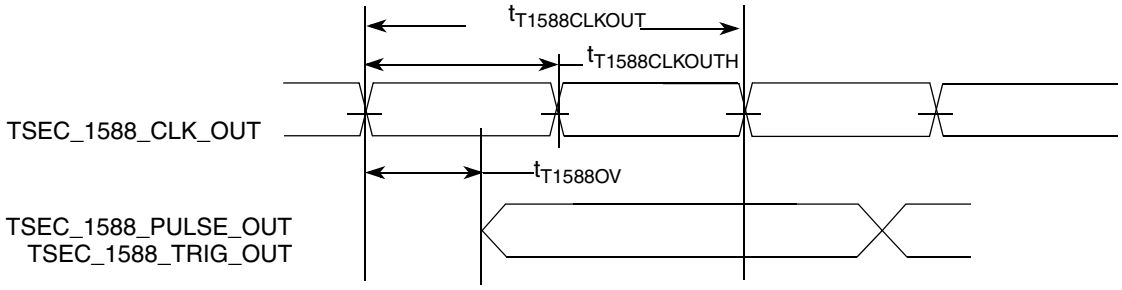
For recommended operating conditions, see Table 3.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	5.0	—	$T_{RX\_CLK} \times 7$	ns	1, 3
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}/t_{T1588CLK}$	40	50	60	%	2
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time TSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time TSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	$2 \times t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}/t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	$2 \times t_{T1588CLK\_MAX}$	—	—	ns	3

Note:

1. T_{RX_CLK} is the max clock period of TSEC receiving clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.
2. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ will be 2800, 280, and 56 ns respectively.

The following figure shows the data and command output AC timing diagram.



NOTE

TSEC IEEE 1588 Output AC timing: The output delay is counted starting at the rising edge if tT1588CLKOUT is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 24. TSEC IEEE 1588 Output AC Timing

The following figure shows the data and command input AC timing diagram.

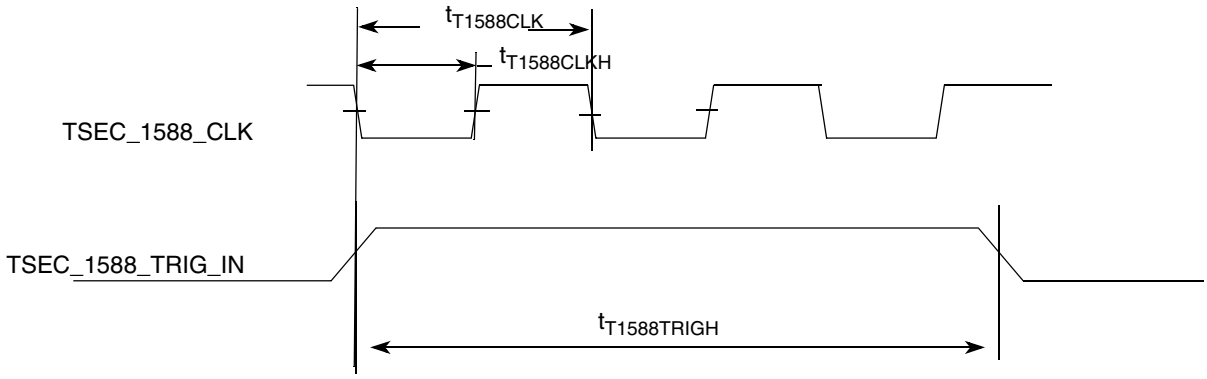


Figure 25. TSEC IEEE 1588 Input AC Timing

3.11 USB

This section provides the AC and DC electrical specifications for the USB interface of the chip.

3.11.1 USB DC Electrical Characteristics

The following table provides the DC electrical characteristics for the USB interface.

Table 42. USB DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output High voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.8	—	V	—
Output Low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.3	V	—

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Note that the symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

3.11.2 USB AC Electrical Specifications

The following table describes the general timing parameters of the USB interface of the chip.

Table 43. USB General Timing Parameters

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
USB clock cycle time	t_{USCK}	15	—	ns	2, 3, 4, 5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2, 3, 4, 5
input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	2, 3, 4, 5
USB clock to output valid— all outputs	t_{USKHOV}	—	7	ns	2, 3, 4, 5
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	2, 3, 4, 5

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H) with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to 0.4 × OV_{DD} of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

The following two figures provide the AC test load and signals for the USB, respectively.

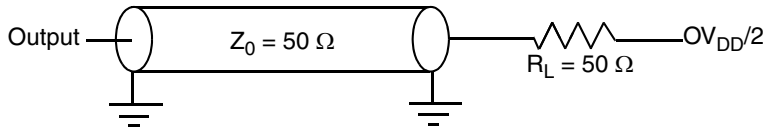


Figure 26. USB AC Test Load

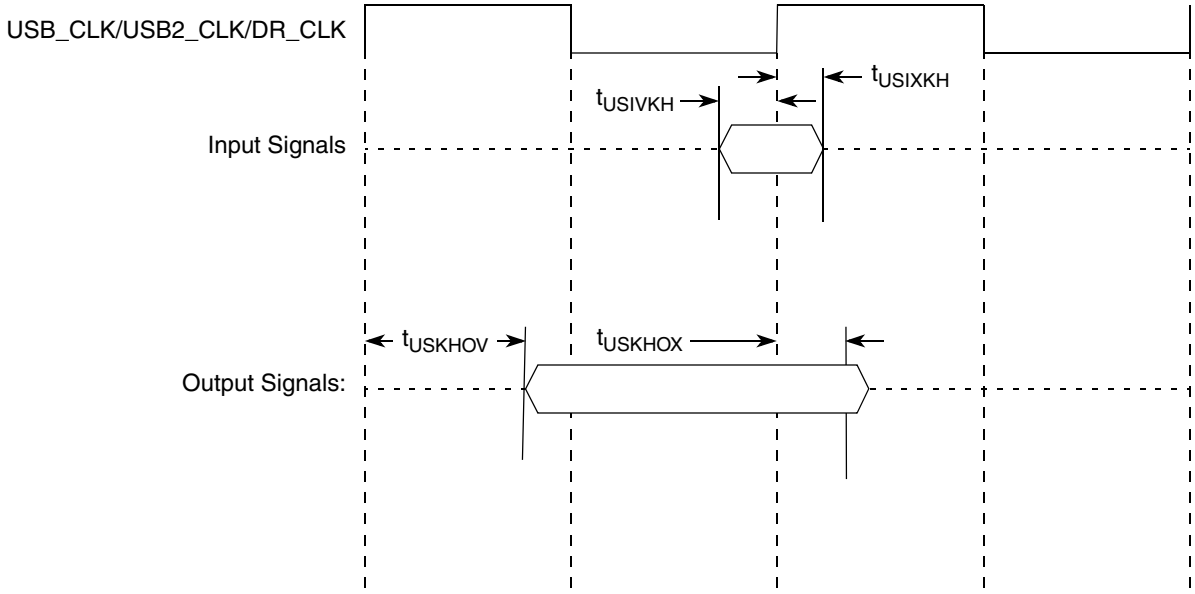


Figure 27. USB Signals

The following table provides the USB clock input (USB_CLK_IN) AC timing specifications.

Table 44. USB_CLK_IN AC Timing Specifications

Parameter/Condition	Conditions	Symbol	Min	Typ	Max	Unit
Frequency range	—	$f_{USB\_CLK\_IN}$	54	60	66	MHz
Clock frequency tolerance	—	t_{CLK_TOL}	–0.05	0	0.05	%
Reference clock duty cycle	Measured at 1.6 V	t_{CLK_DUTY}	40	50	60	%
Total input jitter/time interval error	Peak-to-peak value measured with a second order high-pass filter of 500 kHz bandwidth	t_{CLK_PJ}	—	—	200	ps

3.12 Enhanced Local Bus

This section describes the DC and AC electrical specifications for the enhanced local bus interface.

3.12.1 Enhanced Local Bus DC Electrical Specifications

The following table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 3.3 V DC.

Table 45. Enhanced Local Bus DC Electrical Characteristics (3.3 V DC)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	2	—	V
Input low voltage	V_{IL}	—	0.8	V
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Output low voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 3.1.2, "Recommended Operating Conditions."

The following table provides the DC electrical characteristics for the enhanced local bus interface when operating at BV_{DD} = 1.8 V DC.

Table 46. Enhanced Local Bus DC Electrical Characteristics (1.8 V DC)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	1.25	—	V
Input low voltage	V_{IL}	—	0.6	V
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA
Output high voltage (BVDD = min, IOH = –0.5 mA)	V_{OH}	1.35	—	V
Output low voltage (BVDD = min, IOL = 0.5 mA)	V_{OL}	—	0.4	V

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol VIN, in this case, represents the BVIN symbol referenced in Section 3.1.2, "Recommended Operating Conditions".

3.12.2 Enhanced Local Bus AC Electrical Specifications

3.12.2.1 Test Condition

The following figure provides the AC test load for the enhanced local bus.

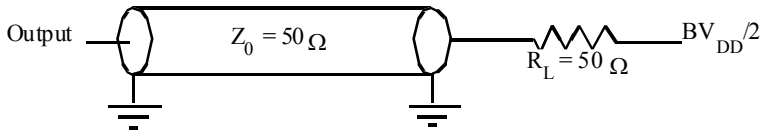


Figure 28. Enhanced Local Bus AC Test Load

3.12.2.2 Local Bus AC Timing Specifications for PLL Bypass Mode

All output signal timings are relative to the falling edge of any LCLKs for PLL bypass mode. The external circuit must use the rising edge of the LCLKs to latch the data.

All input timings except LGTA/LUPWAIT/LFRB are relative to the rising edge of LCLKs. LGTA/LUPWAIT/LFRB are relative to the falling edge of LCLKs.

The following table describes the timing specifications of the local bus interface for PLL bypass mode.

Table 47. Enhanced Local Bus Timing Specifications (BV_{DD} = 3.3 V and 1.8 V)—PLL Bypass Mode

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	12	—	ns	—
Local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	—
Input setup (except LGTA/LUPWAIT/LFRB)	t_{LBIVKH}	6	—	ns	—
Input hold (except LGTA/LUPWAIT/LFRB)	t_{LBIXKH}	1	—	ns	—
Input setup (for LGTA/LUPWAIT/LFRB)	t_{LBIVKL}	6	—	ns	—
Input hold (for LGTA/LUPWAIT/LFRB)	t_{LBIXKL}	1	—	ns	—
Output delay (Except LALE)	t_{LBKLOV}	—	1.5	ns	—
Output hold (Except LALE)	t_{LBKLOX}	-3.5	—	ns	4
Local bus clock to output high impedance for LAD/LDP	t_{LBKLOZ}	—	2	ns	2
LALE output negation to LAD/LDP output transition (LATCH hold time)	t_{LBONOT}	1/2	1	eLBC controller clock cycle	3

Note:

1. All signals are measured from $BV_{DD}/2$ of rising/falling edge of LCLK to $BV_{DD}/2$ of the signal in question.
2. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
3. t_{LBONOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBONOT} is determined by LBCR[AHD]. The unit is the eLBC controller clock cycle, which is the internal clock that runs the local bus controller, not the external LCLK. LCLK cycle = eLBC controller clock cycle × LCRR[CLKDIV]. After power on reset, LBCR[AHD] defaults to 0 and eLBC runs at maximum hold time.
4. Output hold is negative. This means that output transition happens earlier than the falling edge of LCLK.

The following figure shows the AC timing diagram for PLL bypass mode.

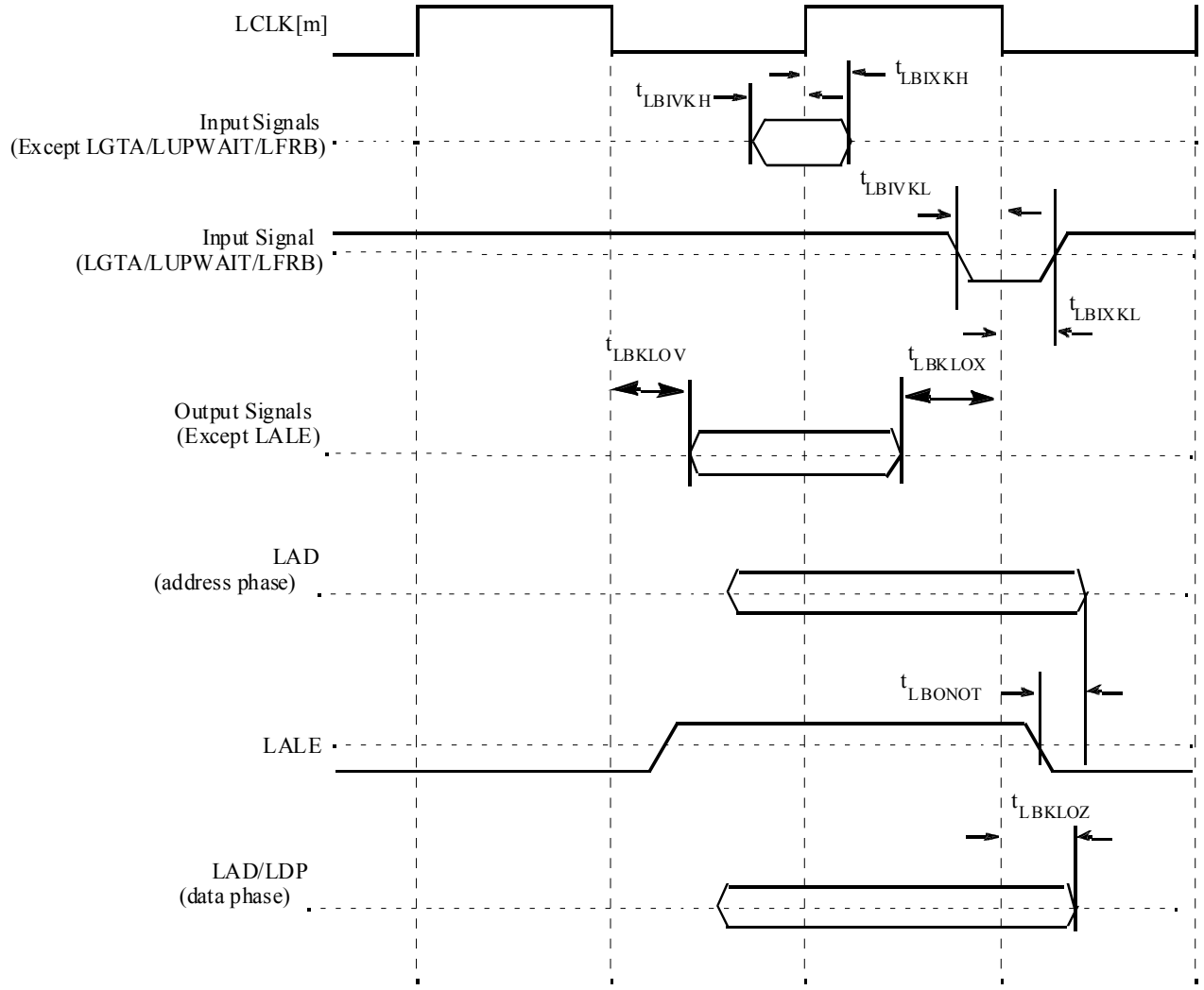


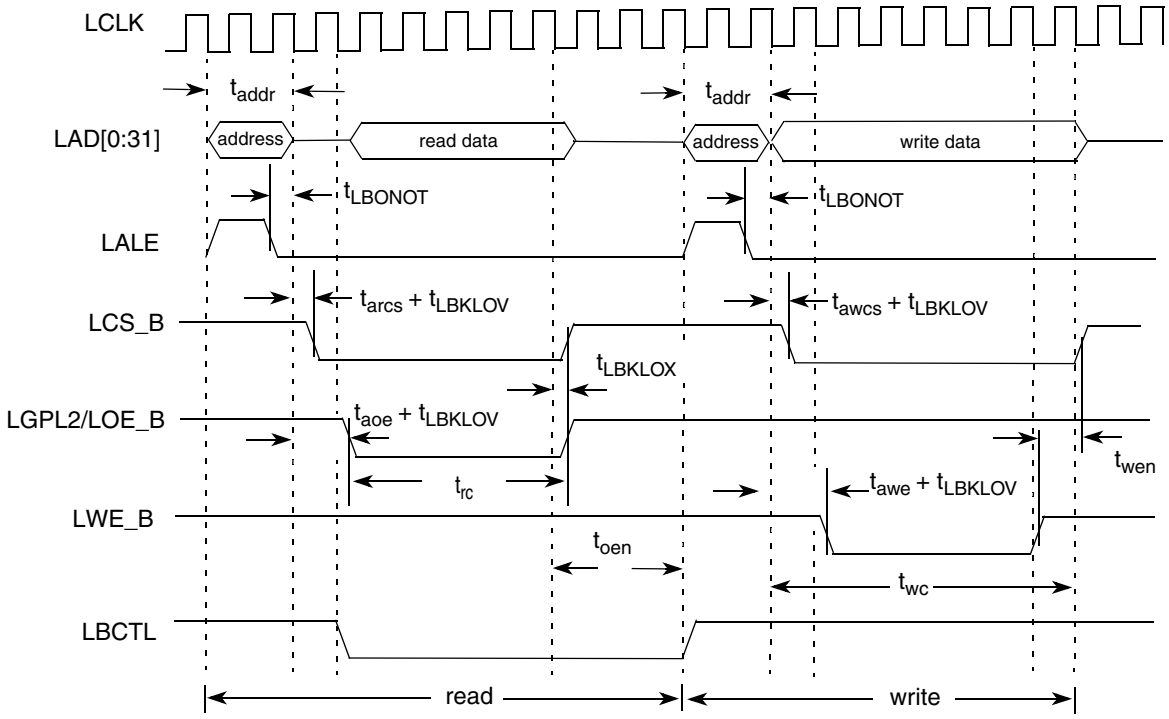
Figure 29. Enhanced Local Bus Signals (PLL Bypass Mode)

Figure 29 applies to all three controllers that eLBC supports: GPCM, UPM, and FCM.

For input signals, the AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKHOV}$.

The following figure shows how the AC timing diagram applies to GPCM in PLL bypass mode. The same principle applies to UPM and FCM



1 t_{addr} is programmable and determined by LCRR[EADC] and ORx[EAD].

2 t_{arcs}, t_{awcs}, t_{aoe}, t_{rc}, t_{oen}, t_{awe}, t_{wc}, t_{wen} are determined by ORx. See the chip reference manual.

Figure 30. GPCM Output Timing Diagram (PLL Bypass Mode)

3.13 Programmable Interrupt Controller (PIC)

This section describes the DC and AC electrical specifications for PIC on the chip.

3.13.1 PIC DC Electrical Characteristics

The following table provides the DC electrical characteristics for the PIC interface.

Table 48. PIC DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—

Table 48. PIC DC Electrical Characteristics (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Note that the symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

3.13.2 PIC AC Timing Specifications

The following table provides the PIC input and output AC timing specifications.

Table 49. PIC Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
PIC inputs—minimum pulse width	t_{PIWID}	3	—	SYSCLK	1

Note:
1. PIC inputs and outputs are asynchronous to any visible clock. PIC outputs should be synchronized before use by any external synchronous logic. PIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge-triggered mode.

3.14 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the chip.

3.14.1 JTAG DC Electrical Characteristics

The following table provides the JTAG DC electrical characteristics.

Table 50. JTAG DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3
2. Note that the symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

3.14.2 JTAG AC Timing Specifications

The following table provides the JTAG AC timing specifications as defined in Figure 31 through Figure 34.

Table 51. JTAG AC Timing Specifications

For recommended operating conditions see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times	t_{JTDVKH}	4	—	ns	—
Input hold times	t_{JTDXKH}	10	—	ns	—
Output valid times	t_{JTKLDV}	0	10	ns	3
Output hold times	t_{JTKLDX}	0	—	ns	3
JTAG external clock to output high impedance	t_{JTKLDZ}	4	10	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

The following figure provides the AC test load for TDO and the boundary-scan outputs.

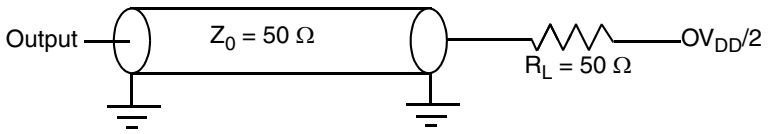


Figure 31. AC Test Load for the JTAG Interface

The following figure provides the JTAG clock input timing diagram.

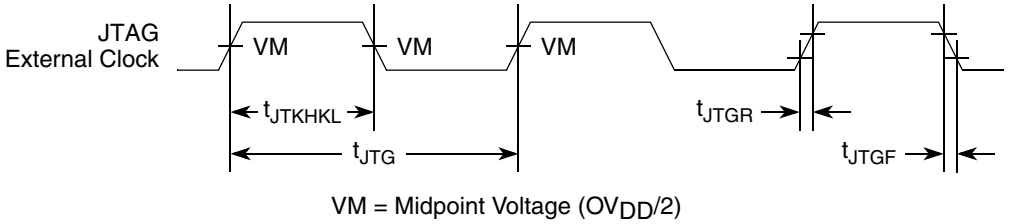


Figure 32. JTAG Clock Input Timing Diagram

The following figure provides the $\overline{\text{TRST}}$ timing diagram.

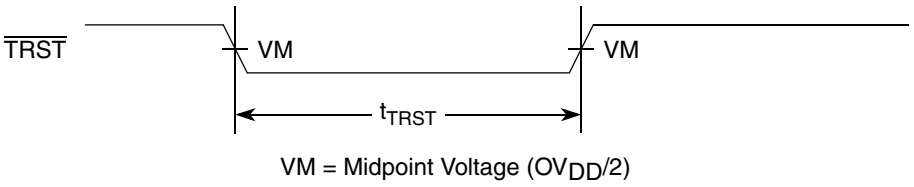


Figure 33. $\overline{\text{TRST}}$ Timing Diagram

The following figure provides the boundary-scan timing diagram.

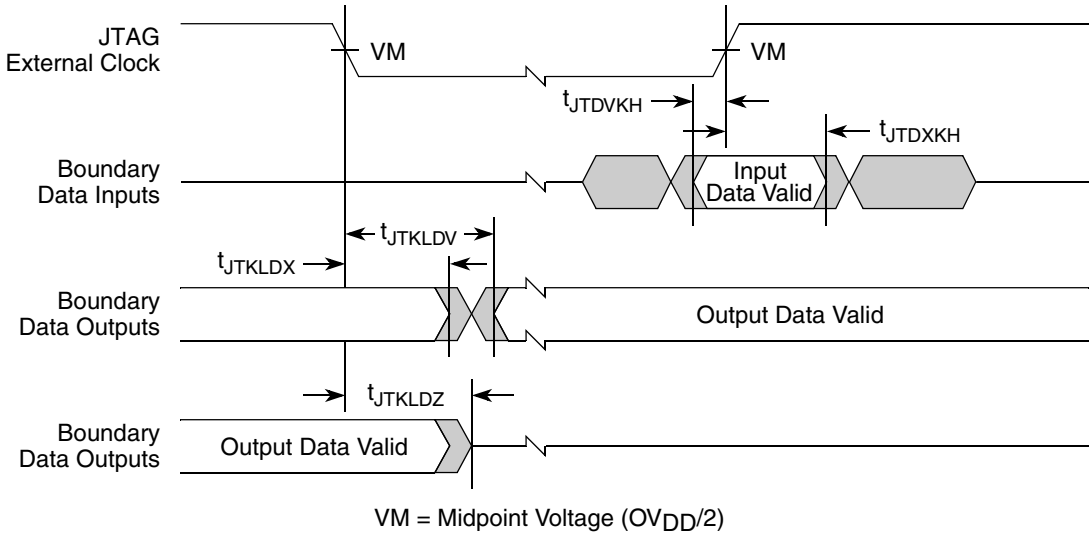


Figure 34. Boundary-Scan Timing Diagram

3.15 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the chip.

3.15.1 I²C DC Electrical Characteristics

The following table provides the DC electrical characteristics for the I²C interfaces.

Table 52. I²C DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Output low voltage	V_{OL}	0	0.4	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 × OV_{DD} and 0.9 × OV_{DD}(max)	I_I	–10	35	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:
1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3
2. Output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the chip reference manual for information on the digital filter used.
4. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

3.15.2 I²C AC Electrical Specifications

The following table provides the AC timing parameters for the I²C interfaces.

Table 53. I²C AC Electrical Specifications

For recommended operation conditions see Table 3. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 52)

Parameter	Symbol	Min	Max	Unit	Note
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0	 — —	μs	3
Data output delay time	t_{I2OVKL}	—	0.9	μs	4
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	μs	—

Table 53. I^2C AC Electrical Specifications (continued)

For recommended operation conditions see Table 3. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 52)

Parameter	Symbol	Min	Max	Unit	Note
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V	—
Capacitive load for each bus line	Cb	—	400	pF	—

Note:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I^2C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I^2C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I^2C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I^2C frequency calculation must be followed. Refer to Freescale application note AN2919, "Determining the I2C Frequency Divider Ratio for SCL."
3. As a transmitter, the chip provides a delay time of at least 300 ns for the SDA signal (referred to as the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the chip acts as the I^2C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If under some rare condition, the 300 ns SDA output delay time is required for the chip as transmitter, application note AN2919 referred to in note 4 below is recommended.
4. The maximum t_{I2OVKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

The following figure provides the AC test load for the I^2C.

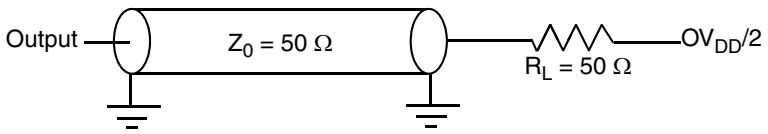


Figure 35. I^2C AC Test Load

The following figure shows the AC timing diagram for the I^2C bus.

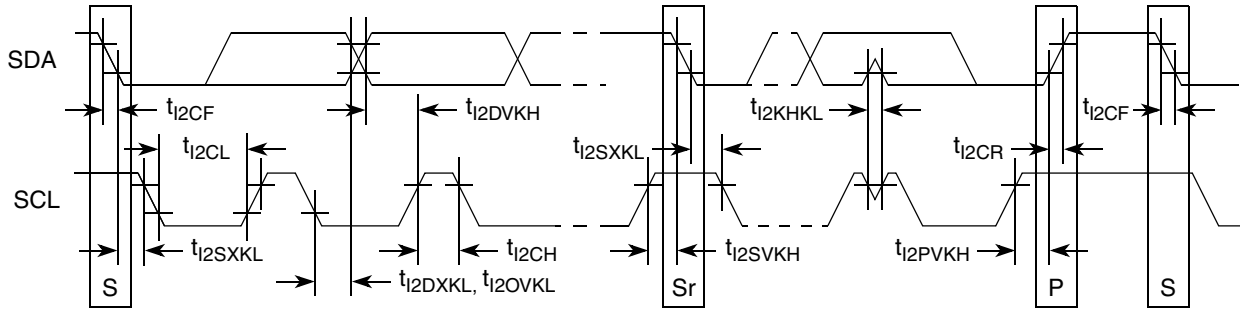


Figure 36. I^2C Bus AC Timing Diagram

3.16 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the chip.

3.16.1 GPIO DC Electrical Characteristics

The following table provides the DC electrical characteristics for the GPIO interface powered by OV_{DD}.

Table 54. GPIO[0:7] DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 3
2. Note that the symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3

The following table provides the DC electrical characteristics for the GPIO interface powered by BV_{DD} when operating from 3.3 V supply.

Table 55. GPIO[8:15] DC Electrical Characteristics (3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the min and max BV_{IN} respective values found in Table 3
2. Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3

The following table provides the DC electrical characteristics for the GPIO interface powered by BV_{DD} when operating from 1.8 V supply.

Table 56. GPIO[8:15] DC Electrical Characteristics (1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.2	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Note:
1. Note that the min $V_{IL}$and max V_{IH} values are based on the min and max BV_{IN} respective values found in Table 3
2. Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3

3.16.2 GPIO AC Timing Specifications

The following table provides the GPIO input and output AC timing specifications.

Table 57. GPIO Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Unit	Note
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Notes:
1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

The following figure provides the AC test load for the GPIO.

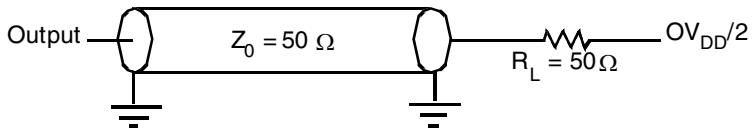


Figure 37. GPIO AC Test Load

3.17 High-Speed Serial Interfaces (HSSI)

The chip features one Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

3.17.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 38 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A volts and B volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

   The transmitter output signals and the receiver input signals SD*n*_TX, $\overline{\text{SD}n\text{\_TX}}$, SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's Single-Ended Swing.

2. **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**):

   The Differential Output Voltage (or Swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SDn\_TX} - V_{\overline{SDn\_TX}}$. The V_{OD} value can be either positive or negative.

3. **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**):

   The Differential Input Voltage (or Swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SDn\_RX} - V_{\overline{SDn\_RX}}$. The V_{ID} value can be either positive or negative.

4. **Differential Peak Voltage**, V_{DIFFp}

   The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. **Differential Peak-to-Peak**, $V_{DIFFp-p}$

   Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

6. **Differential Waveform**

   The differential waveform is constructed by subtracting the inverting signal (SDn_TX, for example) from the non-inverting signal (SDn_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 38 as an example for differential waveform.

7. **Common Mode Voltage, V_{cm}**

   The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (VSDn\_TX + VSDn\_TX)/2 = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may even be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset occasionally.

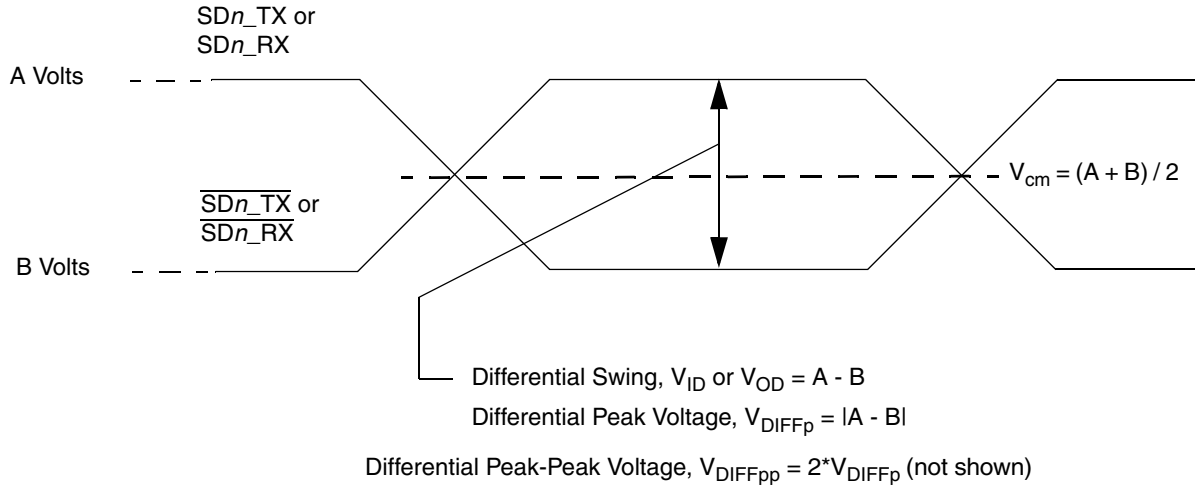


Figure 38. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

3.17.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clock inputs are SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ for PCI Express interface.

The following sections describe the SerDes reference clock requirements and some application information.

3.17.2.1 SerDes Reference Clock Receiver Characteristics

The following figure shows a receiver reference diagram of the SerDes reference clocks.

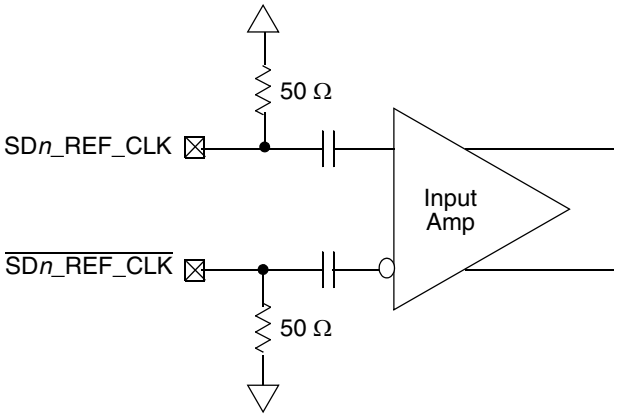


Figure 39. Receiver of SerDes Reference Clocks

The characteristics of the clock signals are as follows:

- The supply voltage requirements for XVDD are specified in Table 2 and Table 3.
- SerDes reference clock receiver reference circuit structure
  - The SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 39. Each differential clock input (SD_REF_CLK or $\overline{\text{SD\_REF\_CLK}}$) has a 50-Ω termination to SGND followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4V (0.4V/50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0mA to 16mA (0-0.8 V), such that each phase of the differential input has a single-ended swing from 0V to 800mV with the common mode voltage at 400 mV.
  - If the device driving the SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ inputs cannot drive 50 Ω to SGND DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

3.17.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the chip's SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For **external DC-coupled** connection, as described in Section 3.17.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 40 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
  - For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND). Figure 41 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

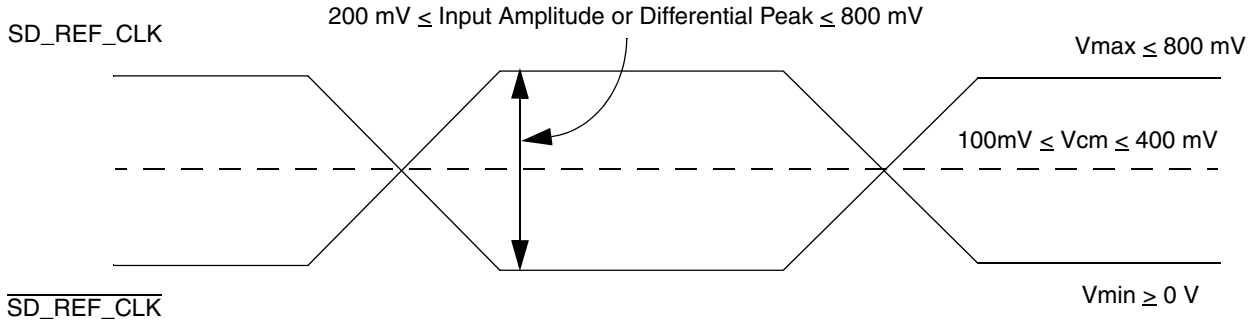


Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

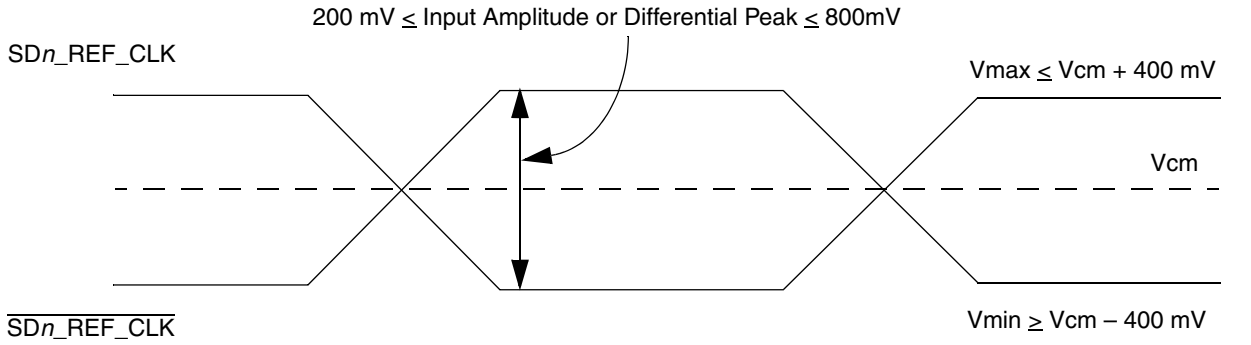


Figure 41. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- **Single-ended Mode**
  - The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.
  - The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

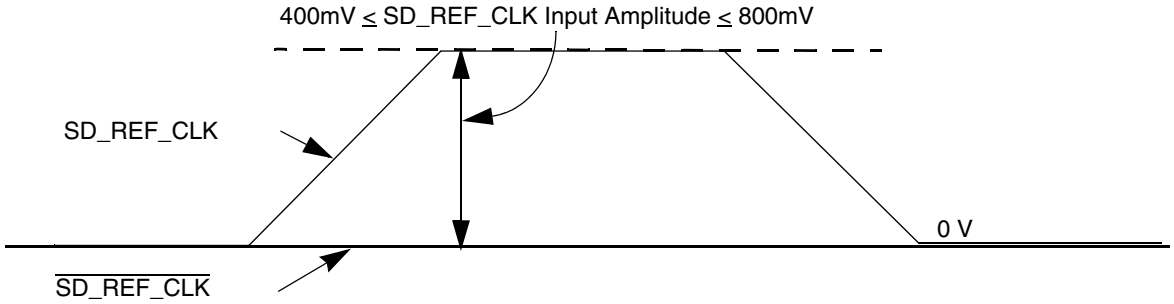


Figure 42. Single-Ended Reference Clock Input DC Requirements

3.17.2.3 AC Requirements for SerDes Reference Clocks

The following table lists AC requirements for the PCI Express and SerDes reference clocks to be guaranteed by the customer's application design.

Table 58. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ Input Clock Requirements

Parameter	Symbol	Min	Typical	Max	Unit	Notes
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	-350	—	+350	ppm	—
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle (Measured at 1.6 V)	t_{CLK_DUTY}	40	50	60	%	—
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ max deterministic peak-peak Jitter @ 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter @ 10^{-6} BER (Peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	2
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3

Note:

1. Only 100/125 have been tested, other in between values will not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 2.0
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SDn_REF_CLK minus SD*n*_REF_CLK).The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing.

3.17.2.4 SerDes Transmitter and Receiver Reference Circuits

The following figure shows the reference circuits for SerDes data lane's transmitter and receiver.

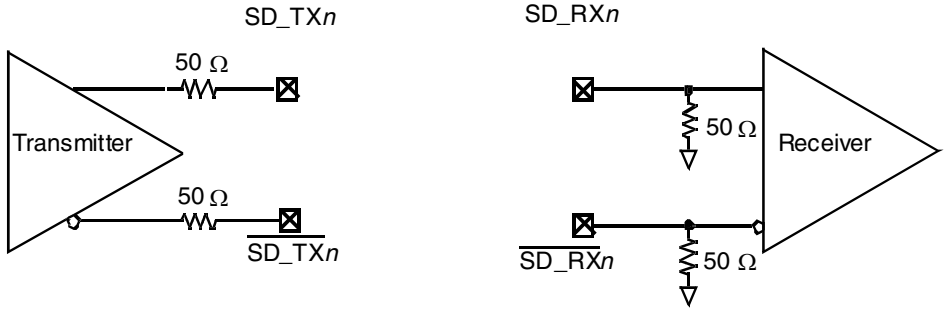


Figure 43. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes is defined in the PCI Express interface protocol section below based on the application usage. Note that external AC Coupling capacitor is required for the above three serial transmission protocols per the protocol's standard requirements.

3.18 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the chip.

3.18.1 PCI Express DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK

For more information, see Section 3.17.2.2, "DC Level Requirement for SerDes Reference Clocks."

3.18.2 PCI Express DC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

3.18.2.1 PCI Express DC Physical Layer Transmitter Specifications

This section discusses PCI Express DC physical layer transmitter specifications for 2.5 Gb/s. Table 59 defines the PCI Express (2.5 Gb/s) DC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 59. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output DC Specifications

Symbol	Parameter	Min	Typical	Max	Units	Comments
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Peak-to-Peak Output Voltage	800	1000	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{TX\text{-}D+} - V_{TX\text{-}D-}\rvert$ See Note 1.
$V_{TX\text{-}DE\text{-}RATIO}$	De- Emphasized Differential Output Voltage (Ratio)	3.0	3.5	4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. See Note 1.
$Z_{TX\text{-}DIFF\text{-}DC}$	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance
$Z_{TX\text{-}DC}$	Transmitter DC Impedance	40	50	60	Ω	Required TX D+ as well as D- DC Impedance during all states

Note:

1. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 44 and measured over any 250 consecutive TX UIs.

3.18.2.2 PCI Express DC Physical Layer Receiver Specifications

This section discusses PCI Express DC physical layer receiver specifications for 2.5 Gb/s. Table 59 defines the PCI Express (2.5 Gb/s) DC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 60. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input DC Specifications

Symbol	Parameter	Min	Typical	Max	Units	Comments
$V_{RX\text{-}DIFFp\text{-}p}$	Differential Input Peak-to-Peak Voltage	175	—	1200	mV	$V_{RX\text{-}DIFFp\text{-}p} = 2*\lvert V_{RX\text{-}D+} - V_{RX\text{-}D-}\rvert$. See Note 1.
$Z_{RX\text{-}DIFF\text{-}DC}$	DC Differential Input Impedance	80	100	120	Ω	RX DC Differential mode impedance. See Note 2.

Table 60. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input DC Specifications (continued)

Symbol	Parameter	Min	Typical	Max	Units	Comments
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω	Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	50 k	—	—	Ω	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power. See Note 3.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	—	235	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$. Measured at the package pins of the Receiver

Note:

1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 44 should be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
2. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
3. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.

3.18.3 PCI Express AC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

3.18.3.1 PCI Express AC Physical Layer Transmitter Specifications

This section discusses the PCI Express AC physical layer transmitter specifications for 2.5Gb/s.

The following table defines the PCI Express (2.5Gb/s) AC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 61. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output AC Specifications

Symbol	Parameter	Min	Typical	Max	Units	Comments
UI	Unit Interval	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
T_{TX-EYE}	Minimum TX Eye Width	0.70	—	—	UI	The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.

Table 61. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output AC Specifications (continued)

Symbol	Parameter	Min	Typical	Max	Units	Comments
C_{TX}	AC Coupling Capacitor	75	—	200	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 4.

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 44 and measured over any 250 consecutive TX UIs.
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The chip's SerDes transmitter does not have CTX built-in. An external AC Coupling capacitor is required.

3.18.3.2 PCI Express AC Physical Layer Receiver Specifications

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 Gb/s.

Table 62 defines the AC specifications for the PCI Express (2.5 Gb/s) differential input at all receivers (RXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 62. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input AC Specifications

Symbol	Parameter	Min	Typical	Max	Units	Comments
UI	Unit Interval	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 - T_{RX-EYE}= 0.6 UI. See Notes 2 and 3.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 4.

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 44 should be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

3.18.3.3 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 44.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

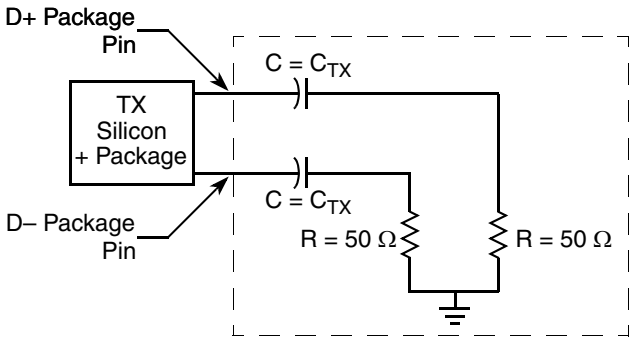


Figure 44. Compliance Test/Measurement Load

4 Thermal

This section describes the thermal specifications of the chip.

4.1 Thermal Characteristics

The following table provides the package thermal characteristics.

Table 63. Package Thermal Characteristics

Characteristic	JEDEC Board	Symbol	Value	Unit	Note
Junction-to-ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	35	°C/W	1, 2
Junction-to-ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	22	°C/W	1, 2, 3
Junction-to-ambient (at 200 ft/min)	Single layer board (1s)	$R_{\theta JA}$	28	°C/W	1, 3
Junction-to-ambient (at 200 ft/min)	Four layer board (2s2p)	$R_{\theta JA}$	19	°C/W	1, 3
Junction-to-board	—	$R_{\theta JB}$	12	°C/W	4
Junction-to-case	—	$R_{\theta JC}$	6	°C/W	5
Junction-to-Package Top Natural Convection	—	Ψ_{JT}	3	°C/W	6

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

5 Package Information

5.1 Package Parameters for the WB-TePBGA

The package parameters are provided in the following list. The package type is 19 mm × 19 mm, 457 plastic ball grid array (WB-TePBGA I).

Package outline	19 mm × 19 mm
Interconnects	457
Pitch	0.8 mm
Module height (typical)	1.4 mm
Solder Balls	Sn3.5%Ag
Ball diameter (typical)	0.40 mm

5.2 Mechanical Dimensions of the WB-TePBGA

Figure 45 shows mechanical dimensions and bottom surface nomenclature of the WB-TePBGA.

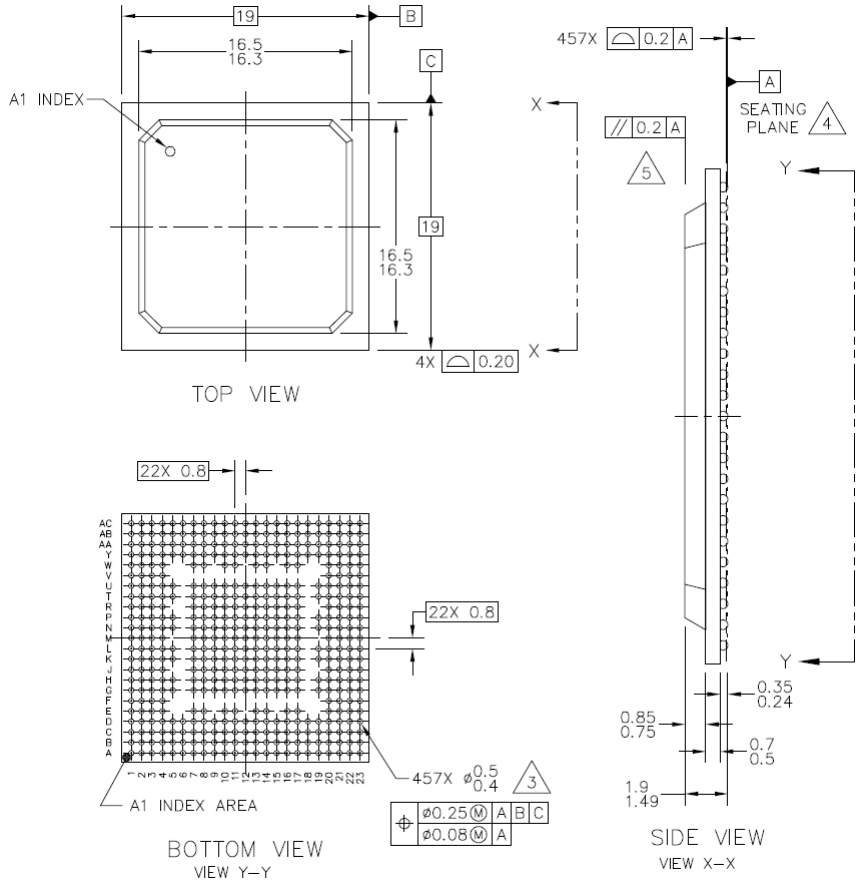


Figure 45. Mechanical Dimensions of the WB-TePBGA package

NOTES:

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14. 5M-1994

3. Maximum solder ball diameter measured parallel to Datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

5.3 Ordering Information

Table 64 provides the Freescale part numbering nomenclature for the P1023. Each part number also contains a revision code which refers to the die mask revision number.

5.3.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the P1023. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

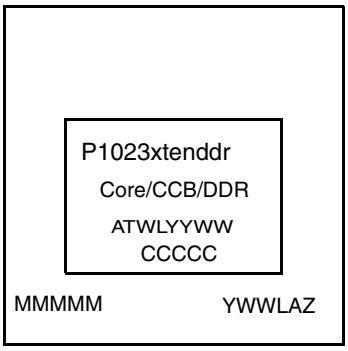
Table 64. Part Numbering Nomenclature

Generation	Platform	Number of cores	Derivative	Qual status	Temperature	Encryption	Package type	CPU/CCB/DDR frequency	Rev
P= 45nm	1	02 = 2 cores	3	S = Special	X = Ext Temp –40 to 105 C	E = SEC Present	5 = TEFPBGA-I Pb Free	CF = 500/320/667	B = Rev 1.1

Notes:

1. See Section 5, “Package Information,” for more information on available package types.

Parts are marked as the example shown in this figure.



TEFPBGA-I

Notes:

P1023xtenddr is the orderable part number.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.
CCCCC is the country code.
ATWLYYWW is the standard assembly, test, year and work week codes.

Figure 46. Part marking for PBGA chips

6 Revision History

The following table provides a revision history for this document.

Table 65. Document Revision History

Rev. Number	Date	Substantive Change(s)
1	05/2013	• Modified the Part Numbering Nomenclature table
0	12/2012	• Initial release

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