MC33272A
MC33274A

Single Supply, High Slew Rate Low Input Offset Voltage, Bipolar Operational Amplifiers

HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

The MC33272/74 series of monolithic operational amplifiers are quality fabricated with innovative Bipolar design concepts. This dual and quad operational amplifier series incorporates Bipolar inputs along with a patented Zip–R–Trim element for input offset voltage reduction. The MC33272/74 series of operational amplifiers exhibits low input offset voltage and high gain bandwidth product. Dual–doublet frequency compensation is used to increase the slew rate while maintaining low input noise characteristics. Its all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, and an excellent phase and gain margin. It also provides a low open loop high frequency output impedance with symmetrical source and sink AC frequency performance.

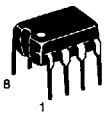
The MC33272/74 series is specified over –40° to +85°C and are available in plastic DIP and SOIC surface mount packages.

- Input Offset Voltage Trimmed to 100 μV (Typ)
- Low Input Bias Current: 300 nA
- Low Input Offset Current: 3.0 nA
- High Input Resistance: 16 MΩ
- Low Noise: 18 nV/$\sqrt{\text{Hz}}$ @ 1.0 kHz
- High Gain Bandwidth Product: 24 MHz @ 100 kHz
- High Slew Rate: 10 V/μs
- Power Bandwidth: 160 kHz
- Excellent Frequency Stability
- Unity Gain Stable: w/Capacitance Loads to 500 pF
- Large Output Voltage Swing: +14.1 V/ –14.6 V
- Low Total Harmonic Distortion: 0.003%
- Power Supply Drain Current: 2.15 mA per Amplifier
- Single or Split Supply Operation: +3.0 V to +36 V or ±1.5 V to ±18 V
- ESD Diodes Provide Added Protection to the Inputs

ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Dual	MC33272AD	T_A = –40° to +85°C	SO–8
	MC33272AP		Plastic DIP
Quad	MC33274AD		SO–14
	MC33274AP		Plastic DIP

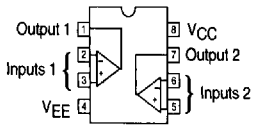
DUAL



P SUFFIX
PLASTIC PACKAGE
CASE 626

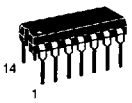
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS

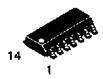


(Top View)

QUAD

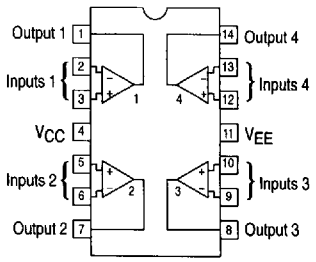


P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} to V_{EE}	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	–60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 2).

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V)	3	$\lvert V_{IO}\rvert$				mV
(V_{CC} = +15 V, V_{EE} = –15 V)						
T_A = +25°C			—	0.1	1.0	
T_A = –40° to +85°C			—	—	1.8	
(V_{CC} = 5.0 V, V_{EE} = 0)						
T_A = +25°C			—	—	2.0	
Average Temperature Coefficient of Input Offset Voltage	3	$\Delta V_{IO}/\Delta T$				μV/°C
R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = –40° to +85°C			—	2.0	—	
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	4, 5	I_{IB}				nA
T_A = +25°C			—	300	650	
T_A = –40° to +85°C			—	—	800	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)		$\lvert I_{IO}\rvert$				nA
T_A = +25°C			—	3.0	65	
T_A = –40° to +85°C			—	—	80	
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V)	6	V_{ICR}				V
T_A = +25°C			V_{EE} to (V_{CC} –1.8)			
Large Signal Voltage Gain (V_O = 0 V to 10 V, R_L = 2.0 kΩ)	7	A_{VOL}				dB
T_A = +25°C			90	100	—	
T_A = –40° to +85°C			86	—	—	
Output Voltage Swing (V_{ID} = ±1.0 V)	8, 9, 12					V
(V_{CC} = +15 V, V_{EE} = –15 V)						
R_L = 2.0 kΩ		V_{O+}	13.4	13.9	—	
R_L = 2.0 kΩ		V_{O-}	—	–13.9	–13.5	
R_L = 10 kΩ		V_{O+}	13.4	14	—	
R_L = 10 kΩ		V_{O-}	—	–14.7	–14.1	
(V_{CC} = 5.0 V, V_{EE} = 0 V)	10, 11					
R_L = 2.0 kΩ		V_{OL}	—	—	0.2	
R_L = 2.0 kΩ		V_{OH}	3.7	—	5.0	
Common Mode Rejection (V_{in} = +13.2 V to –15 V)	13	CMR	80	100	—	dB
Power Supply Rejection	14, 15	PSR				dB
V_{CC}/V_{EE} = +15 V/ –15 V, +5.0 V/ –15 V, +15 V/ –5.0 V			80	105	—	
Output Short Circuit Current (V_{ID} = 1.0 V, Output to Ground)	16	I_{SC}				mA
Source			+25	+37	—	
Sink			–25	–37	—	
Power Supply Current Per Amplifier (V_O = 0 V)	17	I_{CC}				mA
(V_{CC} = +15 V, V_{EE} = –15 V)						
T_A = +25°C			—	2.15	2.75	
T_A = –40° to +85°C			—	—	3.0	
(V_{CC} = 5.0 V, V_{EE} = 0 V)						
T_A = +25°C			—	—	2.75	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0 V)	18, 33	SR	8.0	10	—	V/μs
Gain Bandwidth Product (f = 100 kHz)	19	GBW	17	24	—	MHz
AC Voltage Gain (R_L = 2.0 kΩ, V_O = 0 V, f = 20 kHz)	20, 21, 22	A_{VO}	—	65	—	dB
Unity Gain Frequency (Open Loop)		f_U	—	5.5	—	MHz
Gain Margin (R_L = 2.0 kΩ, C_L = 0 pF)	23, 24, 26	A_m	—	12	—	dB
Phase Margin (R_L = 2.0 kΩ, C_L = 0 pF)	23, 25, 26	ϕ_m	—	55	—	Degrees
Channel Separation (f = 20 Hz to 20 kHz)	27	CS	—	−120	—	dB
Power Bandwidth (V_O = 20 V_{pp}, R_L = 2.0 kΩ, THD ≤ 1.0%)		BW_P	—	160	—	kHz
Total Harmonic Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)	28	THD	—	0.003	—	%
Open Loop Output Impedance (V_O = 0 V, f = 6.0 MHz)	29	$\|Z_O\|$	—	35	—	Ω
Differential Input Resistance (V_{CM} = 0 V)		R_{IN}	—	16	—	MΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{IN}	—	3.0	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)	30	e_n	—	18	—	nV/√Hz
Equivalent Input Noise Current (f = 1.0 kHz)	31	i_n	—	0.5	—	pA/√Hz

Figure 1. Equivalent Circuit Schematic (Each Amplifier)

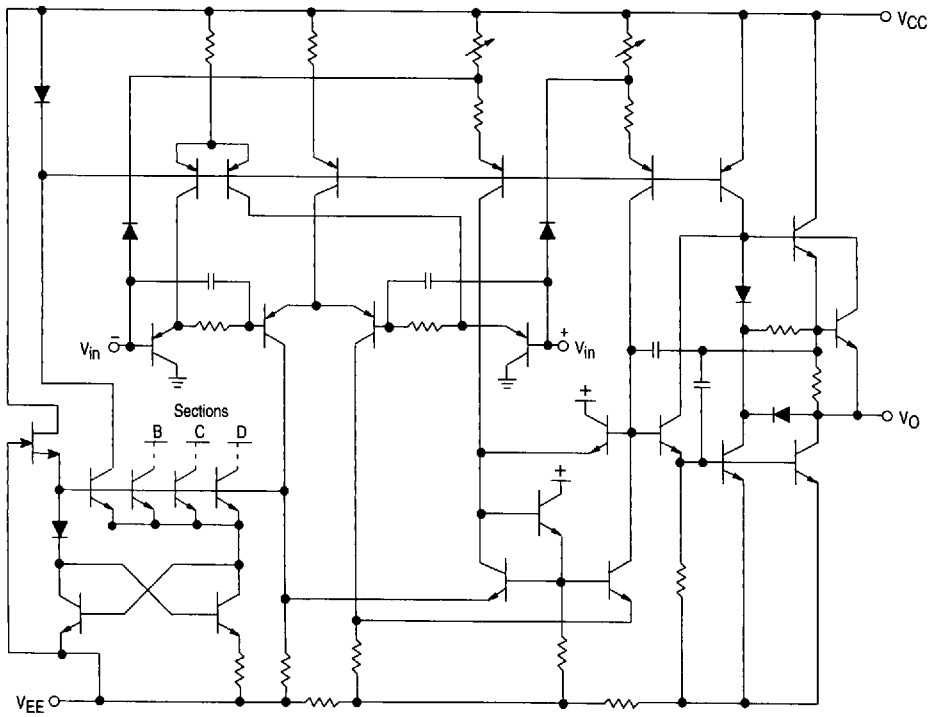

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Figure 2. Maximum Power Dissipation versus Temperature

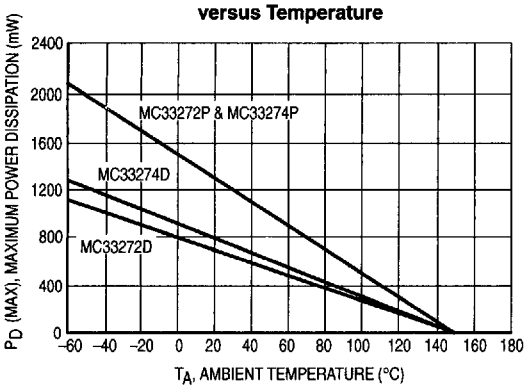

Figure 3. Input Offset Voltage versus Temperature for Typical Units

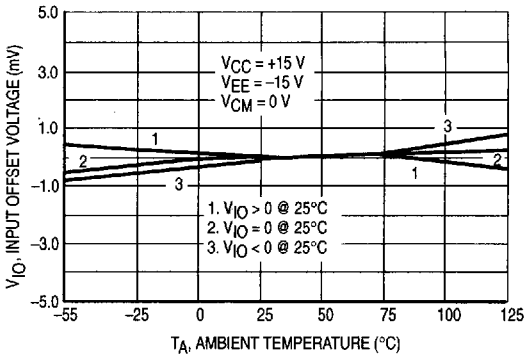

Figure 4. Input Bias Current versus Common Mode Voltage

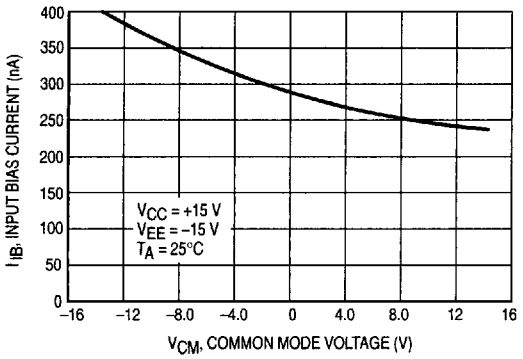

Figure 5. Input Bias Current versus Temperature

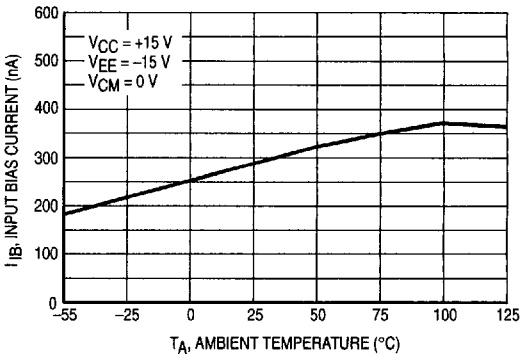

Figure 6. Input Common Mode Voltage Range versus Temperature

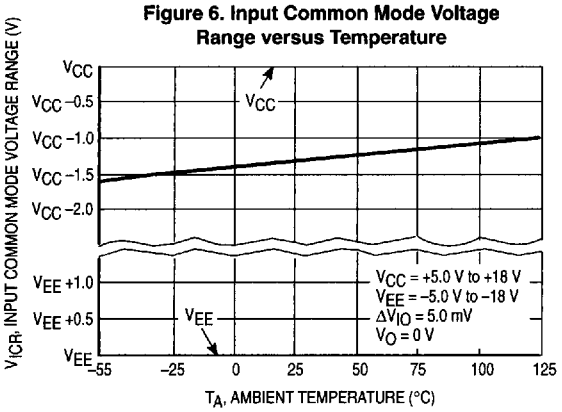

Figure 7. Open Loop Voltage Gain versus Temperature

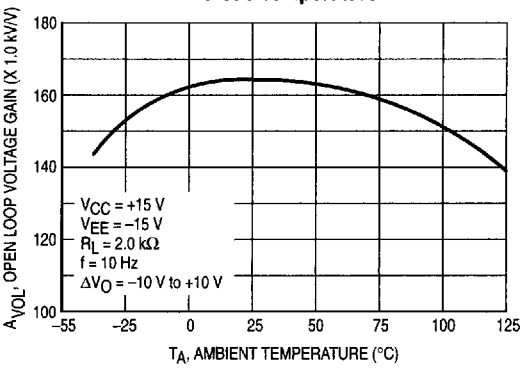

Figure 8. Split Supply Output Voltage Swing versus Supply Voltage

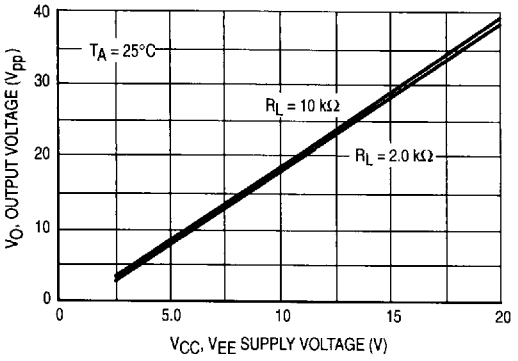

Figure 9. Split Supply Output Saturation Voltage versus Load Current

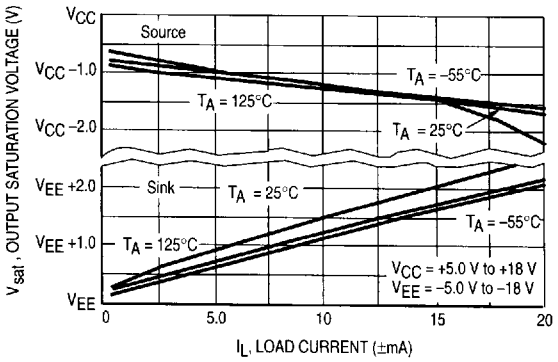

Figure 10. Single Supply Output Saturation Voltage versus Load Resistance to Ground

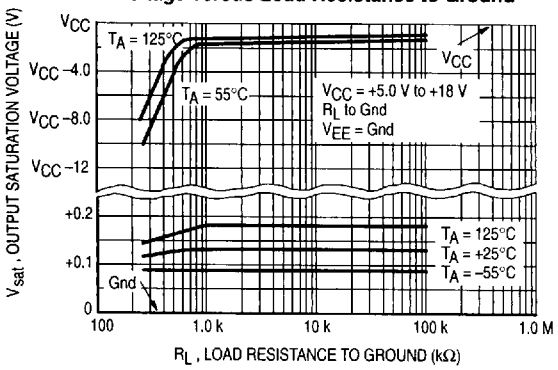

Figure 11. Single Supply Output Saturation Voltage versus Load Resistance to V_{CC}

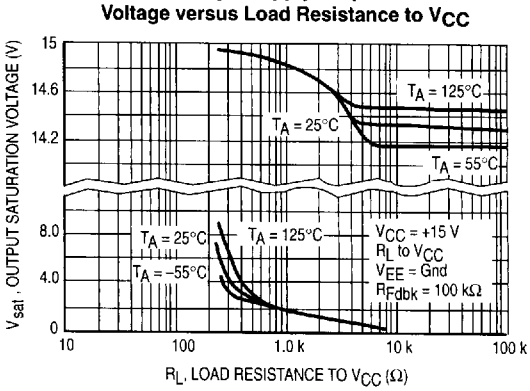

Figure 12. Output Voltage versus Frequency

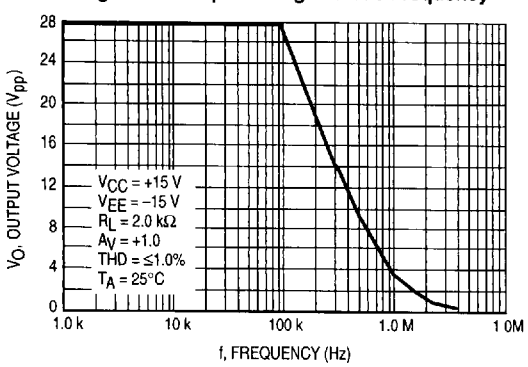

Figure 13. Common Mode Rejection versus Frequency

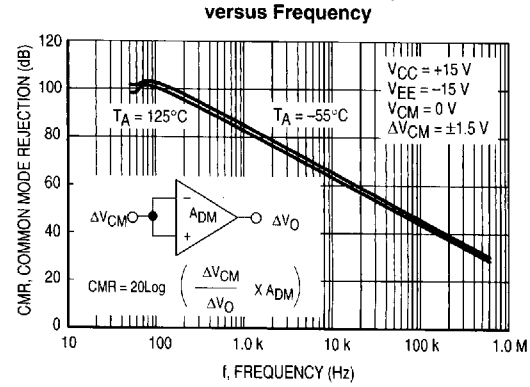

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Figure 14. Positive Power Supply Rejection versus Frequency

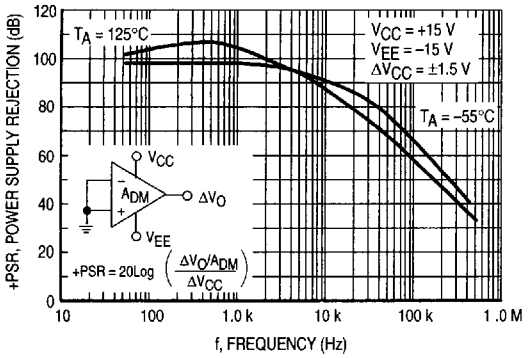

Figure 15. Negative Power Supply Rejection versus Frequency

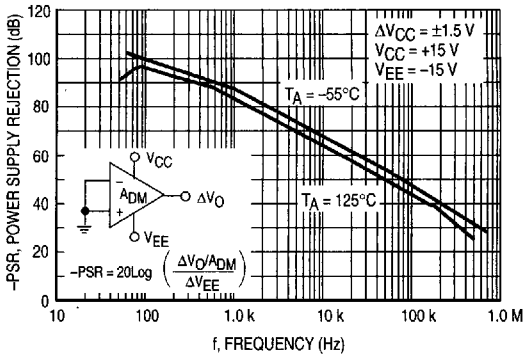

Figure 16. Output Short Circuit Current versus Temperature

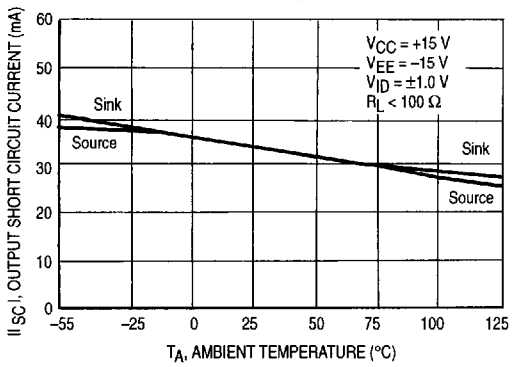

Figure 17. Supply Current versus Supply Voltage

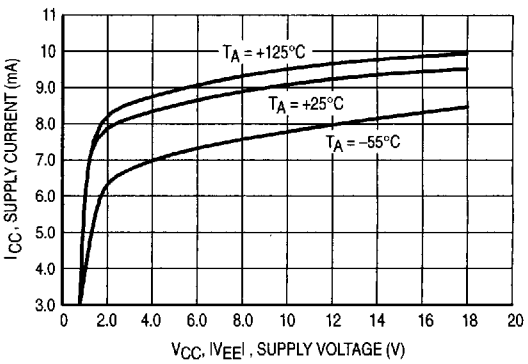

Figure 18. Normalized Slew Rate versus Temperature

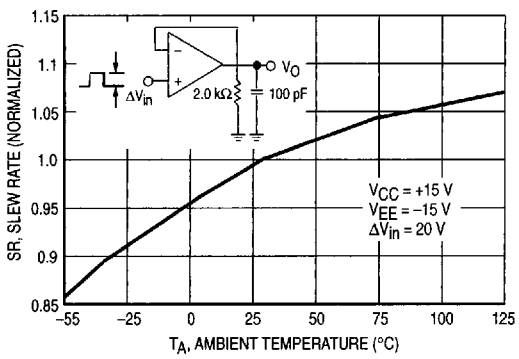

Figure 19. Gain Bandwidth Product versus Temperature

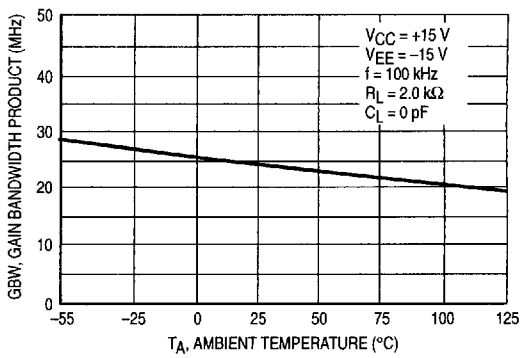

Figure 20. Voltage Gain and Phase versus Frequency

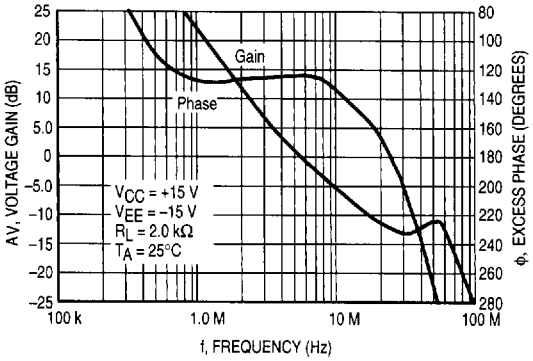

Figure 21. Gain and Phase versus Frequency

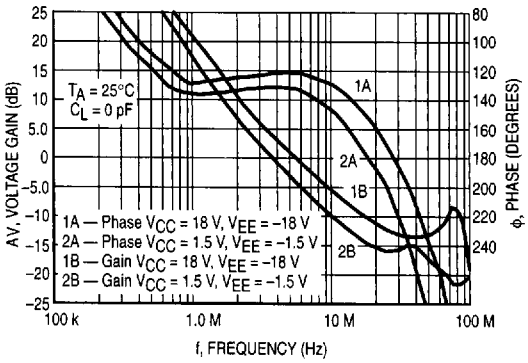

Figure 22. Open Loop Voltage Gain and Phase versus Frequency

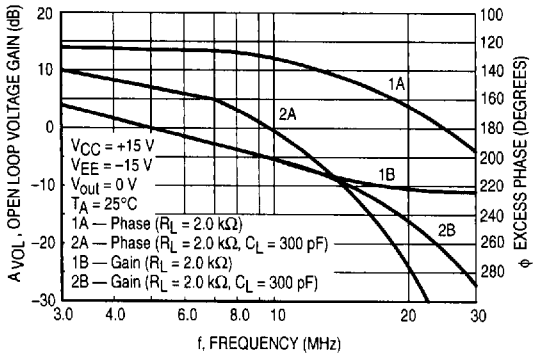

Figure 23. Open Loop Gain Margin and Phase Margin versus Output Load Capacitance

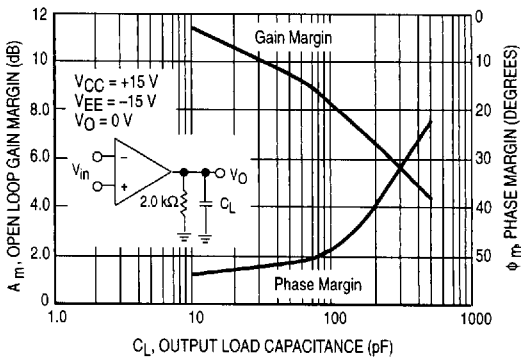

Figure 24. Open Loop Gain Margin versus Temperature

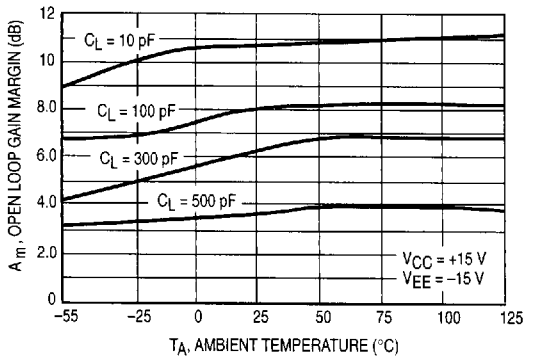

Figure 25. Phase Margin versus Temperature

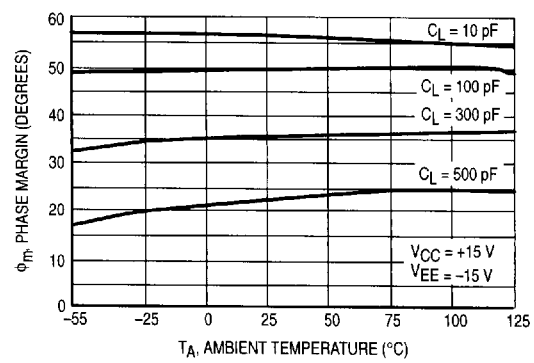

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Figure 26. Phase Margin and Gain Margin versus Differential Source Resistance

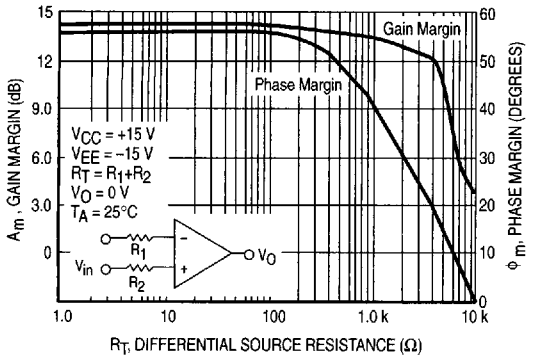

Figure 27. Channel Separation versus Frequency

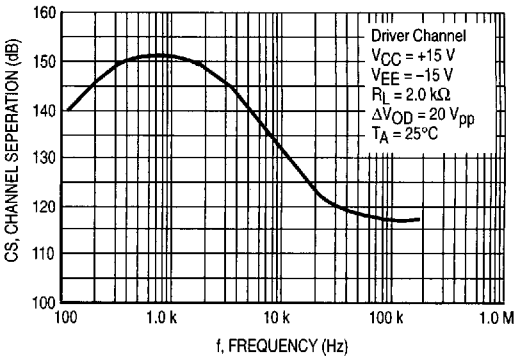

Figure 28. Total Harmonic Distortion versus Frequency

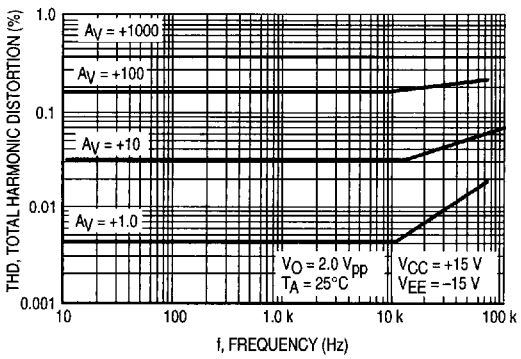

Figure 29. Output Impedance versus Frequency

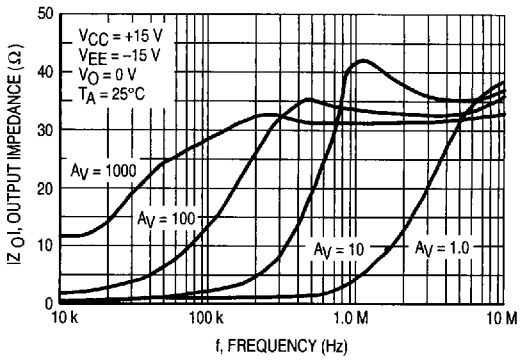

Figure 30. Input Referred Noise Voltage versus Frequency

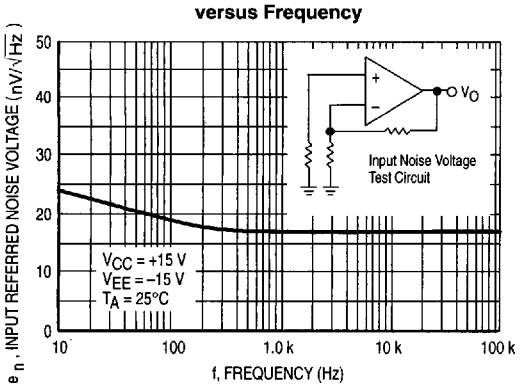

Figure 31. Input Referred Noise Current versus Frequency

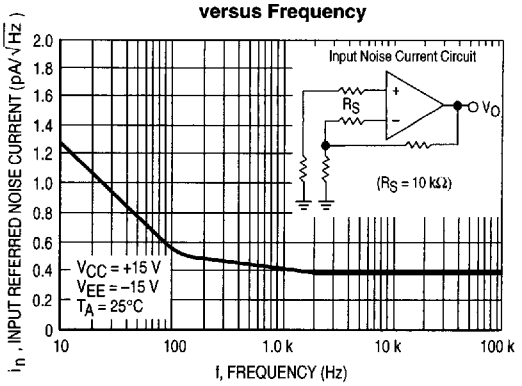

Figure 32. Percent Overshoot versus Load Capacitance

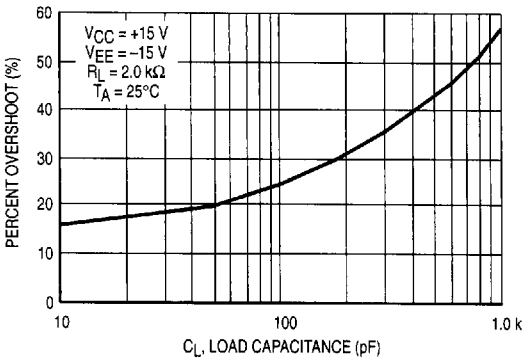

Figure 33. Noninverting Amplifier Slew Rate for the MC33274

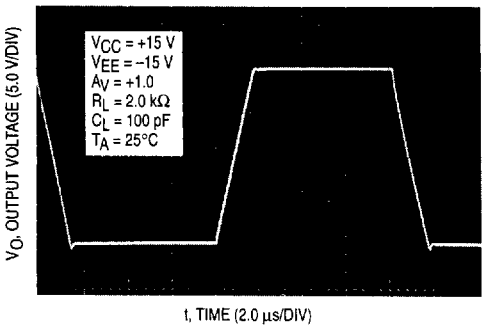

Figure 34. Noninverting Amplifier Overshoot for the MC33274

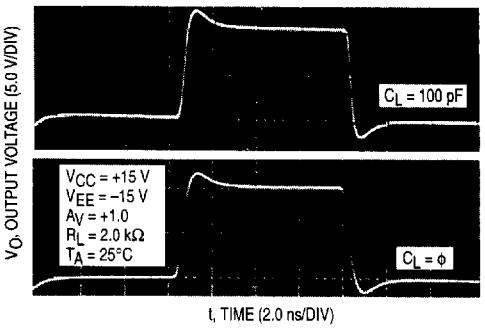

Figure 35. Small Signal Transient Response for MC33274

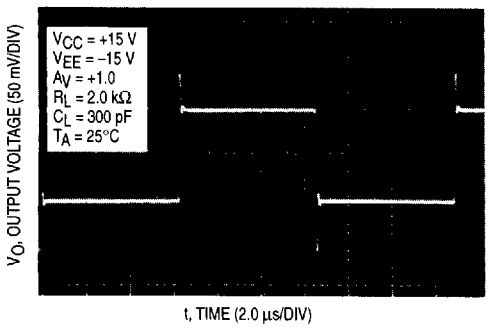

Figure 36. Large Signal Transient Response for MC33274