3257

64 × 5 × 7 CHARACTER GENERATOR

GENERAL DESCRIPTION – The 3257 is a Character Generator designed to display 64 characters in a 5 x 7 font. An on chip column select counter sequences through the five columns of each character. The seven output buffers will each drive one TTL/DTL load directly at a 1 MHz input address rate making the 3257 an ideal device for vertical scan displays. The chip enable allows wired-OR capability if more than 64 characters are required.

- **PROGRAMMABLE WITH A CUSTOM CHARACTER FONT**
- **STANDARD PRODUCT ASCII ENCODED**
- **DIRECT INTERFACING WITH TTL/DTL**
- **WIRED - OR CAPABILITY**

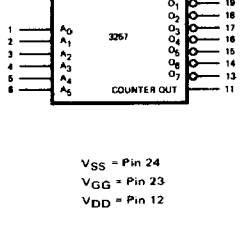
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Voltage on any Pin Relative to V_{SS}	−20 V to +0.3 V

APPLICATIONS:

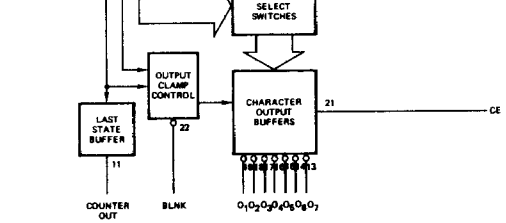
CRT Displays
Billboard Displays
LED Matrix Displays

LOGIC SYMBOL

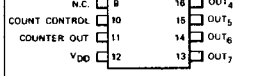


V_{SS} = Pin 24
V_{GG} = Pin 23
V_{DD} = Pin 12

BLOCK DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NC = No Connection
A_n = Address Inputs

FUNCTIONAL DESCRIPTION – A Reset pulse (~GND) is required to set the counter to the first state. A 6-bit binary word presented to the character address inputs is decoded to select 1 of 64 characters in the memory. Information, representing the four columns of the character is available the next clock time after Reset returns HIGH (~V_{SS}). The remaining four columns are sequential, selected by the next four states of the counter. The last state of the counter clamps the outputs HIGH (~V_{SS}) to provide 1 or 2 space blanks between characters. Count Control ~V_{SS} ⇒ MOD 7, Count Control ~ GND ⇒ MOD 6). When the last state (6th or 7th) of the counter is reached, the Counter Output goes HIGH (~V_{SS}). When Chip Enable goes HIGH (~V_{SS}), the chip is activated while a LOW (~ GND) at this terminal, the outputs to allow common out-put bussing. A LOW (~ GND) on the Blanking input pulls the outputs HIGH (~V_{SS}), providing blanking independent of the counter state or the character address.

DC CHARACTERISTICS: V_{SS} = +5 V ±5%, V_{GG} = −12 V ±5%, V_{DD} = 0 V, T_A = 0 C to +70 C

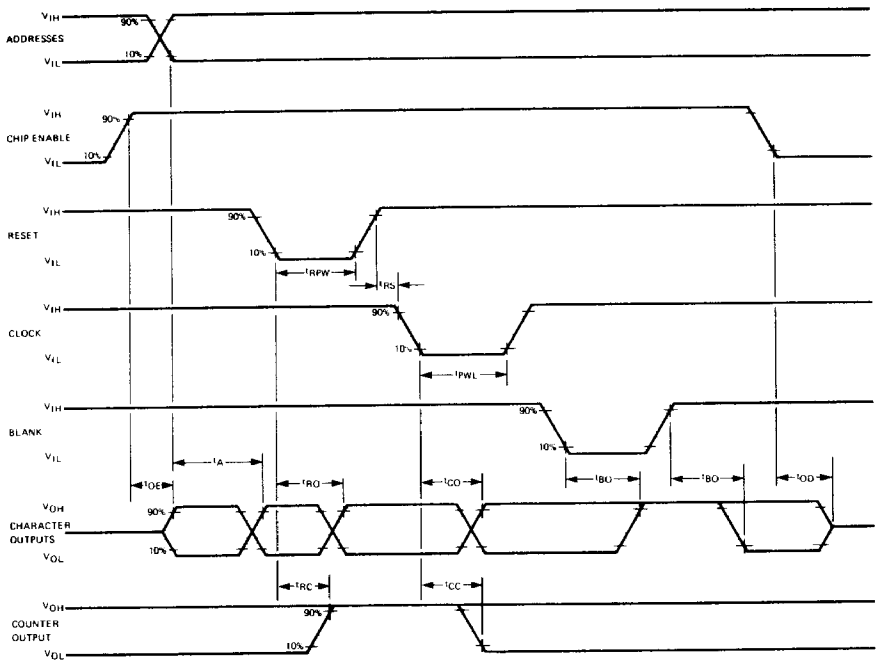
SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	V_{SS} −1	V_{SS}	V	Note 1
V_{IL}	Input LOW Voltage	V_{GG}	0.8	V	Note 1
V_{OH}	Output HIGH Voltage	V_{SS} −0.5	V_{SS}	V	I_{OH} 10 µA
		2.4	V_{SS}	V	I_{OH} 0.5 mA
V_{OL}	Output LOW Voltage	0	0.4	V	I_{DL} 1.6 mA
I_{IN}	Input Leakage Current		−1.0	µA	V_{SS} 0 V, V_{IN} 18 V, Note 1
I_{OUT}	Output Leakage Current		1.0	µA	V_{SS} 0 V, V_{OUT} 6 V, Note 2
I_{SS}	V_{SS} Current		40	mA	V_{SS} 5.25 V, V_{GG} −12.6 V Outputs Open
P_D	Power Dissipation		715	mW	

AC CHARACTERISTICS: V_{SS} = +5 V ±0.25 V, V_{GG} = −12 V ±0.6 V, V_{DD} = 0 V, C_L = 10 pF, T_A = 0 C to +70 C

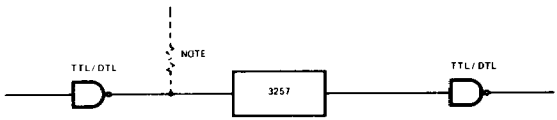
SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
f	Clock Frequency	DC	1.0	MHz	
t_{PWL}	Clock Pulse Width LOW	500		ns	
t_r, t_f	Clock Rise & Fall Time (10%-90%)		2.0	µs	
t_{RPW}	Reset Pulse Width	500		ns	
t_{RS}	Reset to Clock Set Up Time	100		ns	
t_A	Character Address to Output Access Time		1000	ns	Notes 4 & 5
t_{CO}	Clock to Output Access Time		1000	ns	Notes 4 & 5
t_{RO}	Reset to Output Time Delay		600	ns	Notes 4 & 5
t_{BO}	Blanking to Output Time Delay		1000	ns	Notes 4 & 5
t_{CC}	Clock to Counter Output Time Delay		500	ns	Notes 4 & 5
t_{RC}	Reset to Counter Output Time Delay		500	ns	Notes 4 & 5
t_{OE}	Output Enable Delay Time		600	ns	Notes 4 & 5
t_{OD}	Output Disable Delay Time		600	ns	Notes 4 & 5
C_{IN}	Input Capacitance		1.0	pF	f = 1.0 MHz, 0 V Bias Note 1

NOTES:
1. Inputs include Addresses, Count Control, Clock and Reset.
2. Chip Enable = LOW.
3. I_{SS} = −I_{GG} (V_{GG} Supply Current).
4. AC Output LOW level is defined as 0.4 V @ 1.6 mA, current sinking (i.e., 1 TTL load).
5. AC Output HIGH level is defined as 2.4 V @ −40 µA, current sourcing (i.e., 1 TTL load).

TIMING DIAGRAM

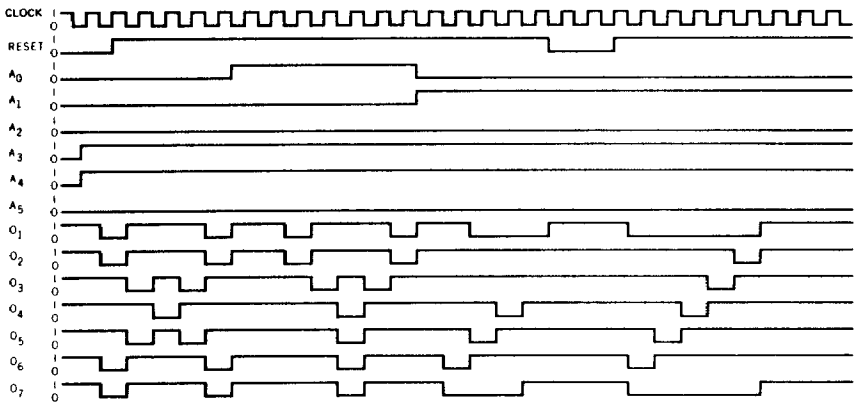


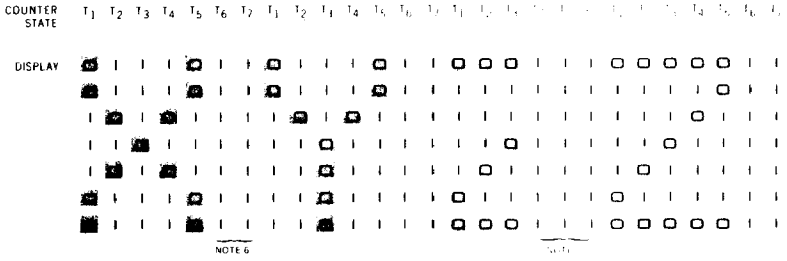
INTERFACING



Note: Directly compatible at outputs with TTL/DTL. Inputs directly compatible with DTL. When being driven by TTL, no pullup resistor needed if TTL output swings to (V_{SS} 1) volts.

TYPICAL FUNCTIONAL TIMING DIAGRAM

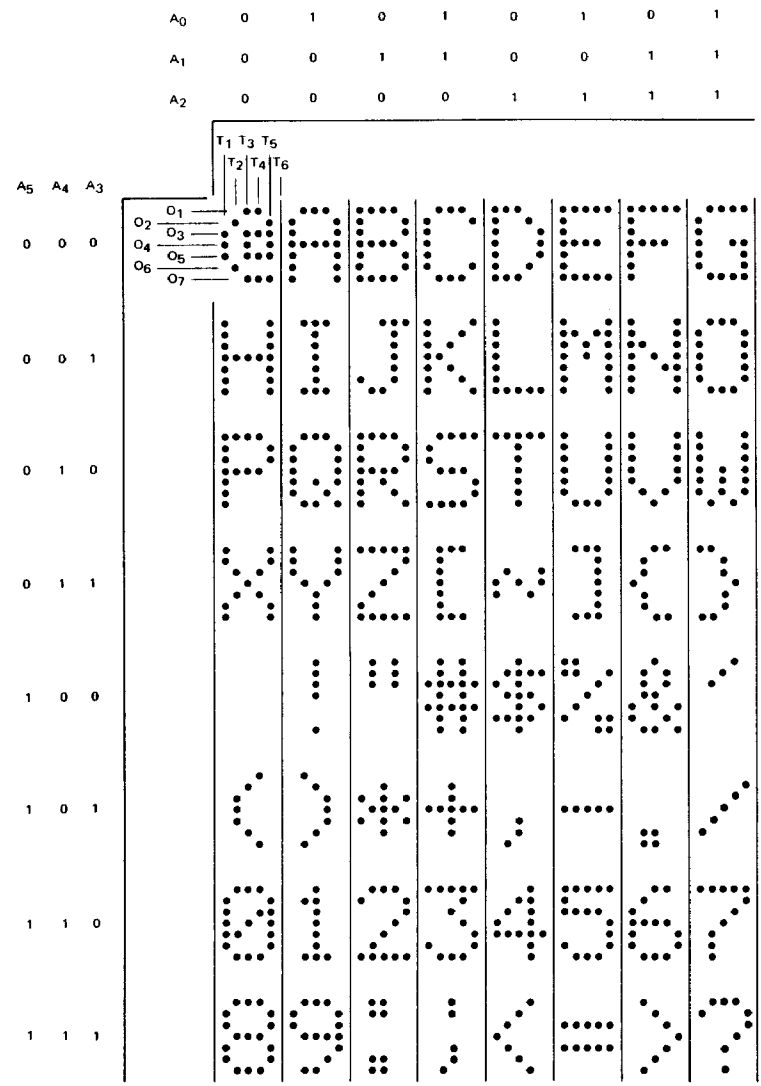




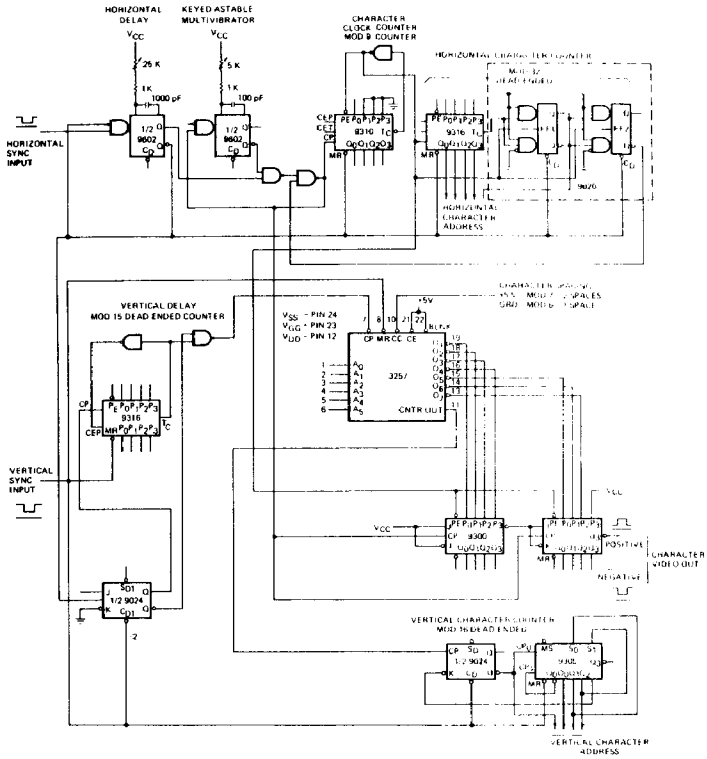
NOTES:
6. Last two counter states (count mode control = HIGH ⇒ MOD 7) provide blanking.
7. Counter is Reset to the last state.

3257A – STANDARD ASCII CHARACTER FONT

COUNT MODE CONTROL = GND ⇒ MOD 6



TYPICAL VERTICAL RASTER SCAN APPLICATION



NOTE:
Horizontal and vertical are referred to as in a standard TV type raster
16 characters per line, 32 character lines in system.
Each character 10 raster lines wide.

CUSTOM FONT ORDERING INFORMATION

Additional patterns may be made available upon request. The 3257 is programmed on IBM cards or IBM forms in the coding format shown below:

A logic "1" = A more positive voltage nominally +5 V
A logic "0" = A more negative voltage nominally 0 V
The character "dots" are defined as logic "0"

6, 7, 8, 9, 10, 11	Character address input code. The most significant bit (A5) is in column 11.
22, 23, 24, 25, 26, 27, 28	The first column of the character addressed. The most significant bit (07) is in Column 28.
30, 31, 32, 33, 34, 35, 36	The next column of the character addressed. The most significant bit (07) is in Column 36.
38, 39, 40, 41, 42, 43, 44	The next column of the character addressed. The most significant bit (07) is in Column 44.
46, 47, 48, 49, 50, 51, 52	The next column of the character addressed. The most significant bit (07) is in Column 52.
54, 55, 56, 57, 58, 59, 60	The last column of the character addressed. The most significant bit (07) is in Column 60.
73, 74, 75, 76, 77, 78, 79, 80	Coding these columns is not essential and may be used for card identification purpose.