February 1996

N

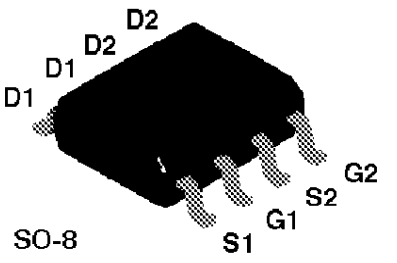
NDS9942
Dual N & P-Channel Enhancement Mode Field Effect Transistor

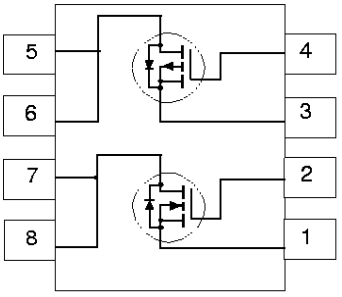
General Description

These dual N- and P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- N-Channel 3.0A, 20V, $R_{DS(ON)}$=0.125Ω @ V_{GS}=10V
  P-Channel -2.5A, -20V, $R_{DS(ON)}$=0.2Ω @ V_{GS}=-10V.
- High density cell design or extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual (N & P-Channel) MOSFET in surface mount package.





Absolute Maximum Ratings T_A= 25°C unless otherwise noted

Symbol	Parameter		N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage		20	-20	V
V_{GSS}	Gate-Source Voltage		± 20	± 20	V
I_D	Drain Current - Continuous T_A = 25°C	(Note 1a)	± 3.0	± 2.5	A
	- Continuous T_A = 70°C	(Note 1a)	± 2.5	± 2.0	
	- Pulsed T_A = 25°C		± 10	± 10	
P_D	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation	(Note 1a)	1.6		
		(Note 1b)	1		
		(Note 1c)	0.9		
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150		°C
THERMAL CHARACTERISTICS					
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40		°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	20			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V	N-Ch			2	µA
		T_J = 55°C				25	µA
		V_{DS} = -16 V, V_{GS} = 0 V	P-Ch			-2	µA
		T_J = 55°C				-25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1	1.5	3	V
		T_J = 125°C		0.7	1.1	2.2	
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-1	-2	-3	
		T_J = 125°C		-0.85	-1.7	-2.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 1.0 A	N-Ch		0.062	0.125	Ω
		T_J = 125°C			0.085	0.175	
		V_{GS} = 4.5 V, I_D = 0.5 A			0.08	0.25	
		T_J = 125°C			0.11	0.35	
		V_{GS} = -10 V, I_D = -1.0 A	P-Ch		0.18	0.2	
		T_J = 125°C			0.24	0.35	
		V_{GS} = -4.5 V, I_D = -0.5 A			0.26	0.4	
		T_J = 125°C			0.35	0.56	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	N-Ch	10			A
		V_{GS} = 4.5 V, V_{DS} = 5 V		2			
		V_{GS} = -10 V, V_{DS} = -5 V	P-Ch	-10			
		V_{GS} = -4.5 V, V_{DS} = 5 V		-2			
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 3 A	N-Ch		7		S
		V_{DS} = -15 V, I_D = -3 A	P-Ch		4		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		525		pF
			P-Ch		525		
C_{oss}	Output Capacitance		N-Ch		315		pF
		P-Channel V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz	P-Ch		300		
C_{rss}	Reverse Transfer Capacitance		N-Ch		185		pF
			P-Ch		130		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	N-Channel V_{DD} = 10 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω	N-Ch		6	15	ns
			P-Ch		8	40	
t_r	Turn - On Rise Time	P-Channel V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω	N-Ch		12	20	ns
			P-Ch		15	40	
$t_{D(off)}$	Turn - Off Delay Time		N-Ch		22	50	ns
			P-Ch		25	90	
t_f	Turn - Off Fall Time		N-Ch		8	50	ns
			P-Ch		8	50	
Q_g	Total Gate Charge	N-Channel V_{DS} = 10 V, I_D = 2.3 A, V_{GS} = 10 V	N-Ch		17	27	nC
			P-Ch		15	25	
Q_{gs}	Gate-Source Charge	P-Channel V_{DS} = -10 V, I_D = -2.3 A, V_{GS} = -10 V	N-Ch		1.2		nC
			P-Ch		1.2		
Q_{gd}	Gate-Drain Charge		N-Ch		5		nC
			P-Ch		4.8		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			1.6	A
			P-Ch			-1.6	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.25 A (Note 2)	N-Ch		0.78	1.2	V
		V_{GS} = 0 V, I_S = -1.25 A (Note 2)	P-Ch		-0.94	-1.6	
t_{rr}	Reverse Recovery Time	N-Channel V_{GS} = 0 V, I_F = 1.25 A, dI_F/dt = 100 A/µs	N-Ch		28	100	ns
			P-Ch		29	100	
I_{rr}	Reverse Recovery Current	P-Channel V_{GS} = 0 V, I_F = -1.25 A, dI_F/dt = 100 A/µs	N-Ch		2.1		A
			P-Ch		1.9		

Notes

1 $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

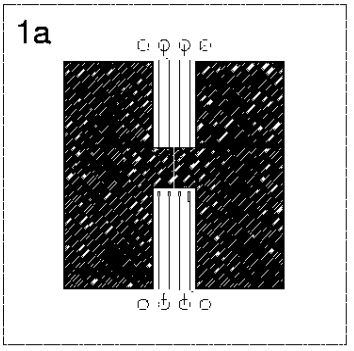
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

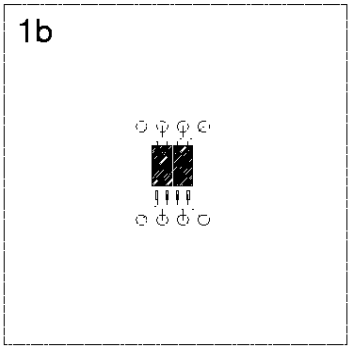
Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

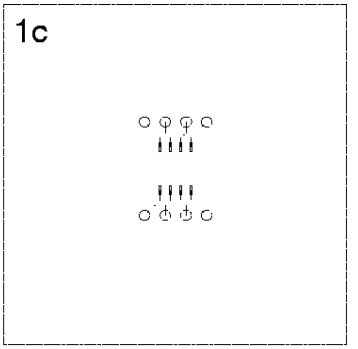
a 78°C/W when mounted on a 0.5 in^2 pad of 2oz copper

b 125°C/W when mounted on a 0.02 in^2 pad of 2oz copper

c 135°C/W when mounted on a 0.003 in^2 pad of 2oz copper







Scale 1 : 1 on letter size paper

2 Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%

Typical Electrical Characteristics: N-Channel

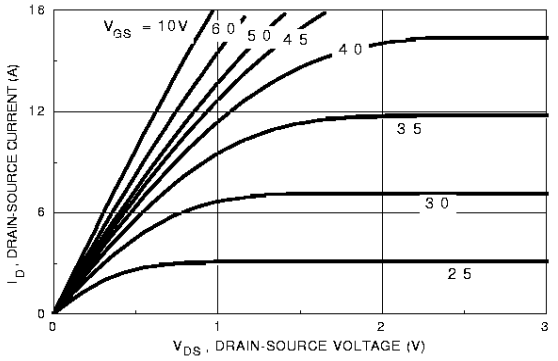


Figure 1. N-Channel On-Region Characteristic.

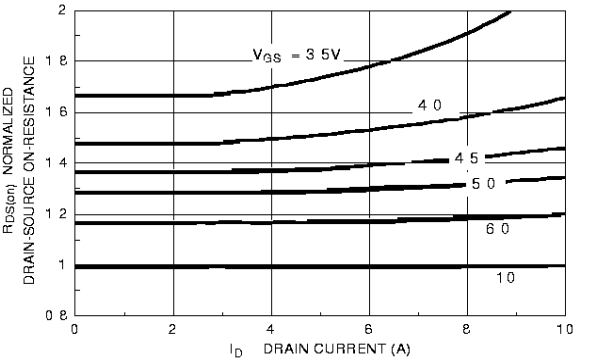


Figure 2. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

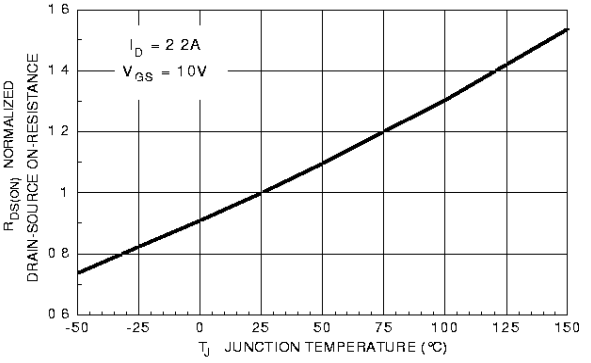


Figure 3. N-Channel On-Resistance Variation with Temperature.

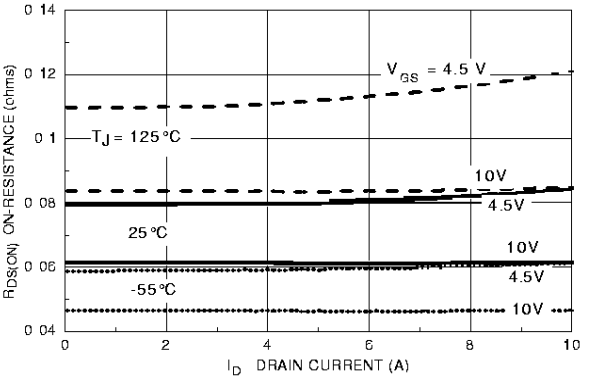


Figure 4. N-Channel On-Resistance Variation with Drain Current and Temperature.

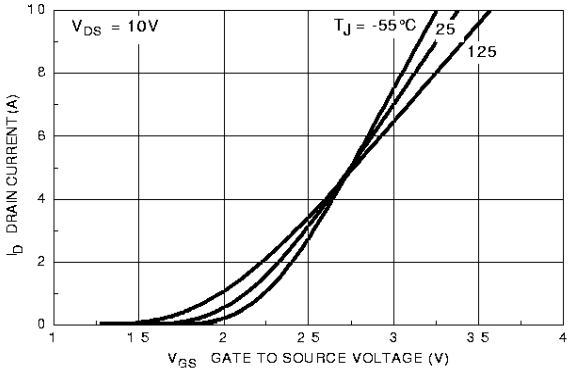


Figure 5. N-Channel Transfer Characteristic.

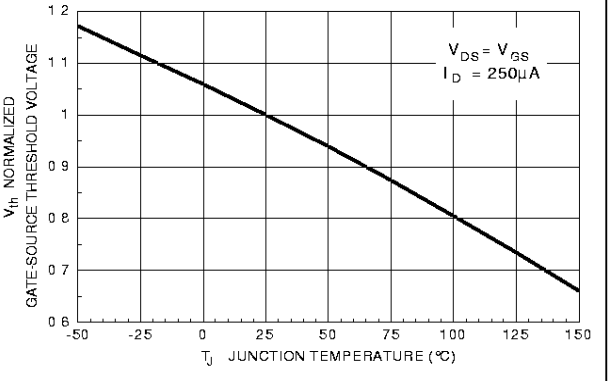


Figure 6. N-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: N-Channel (continued)

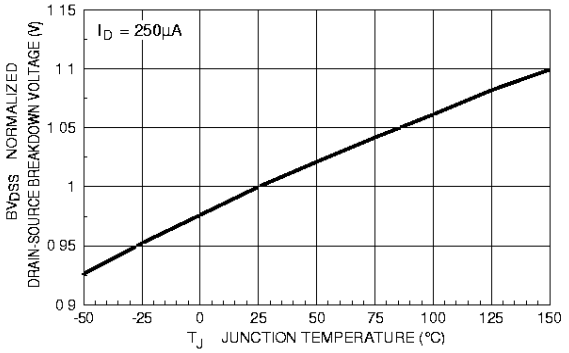


Figure 7. N-Channel Breakdown Voltage Variation with Temperature.

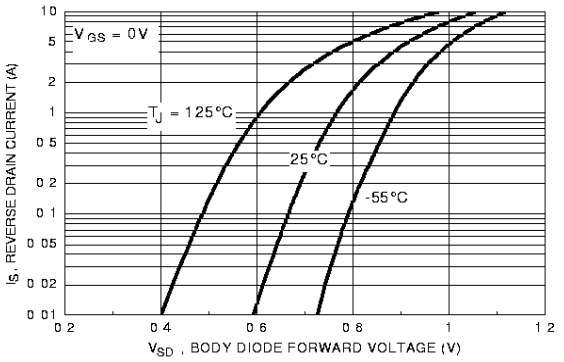


Figure 8. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.

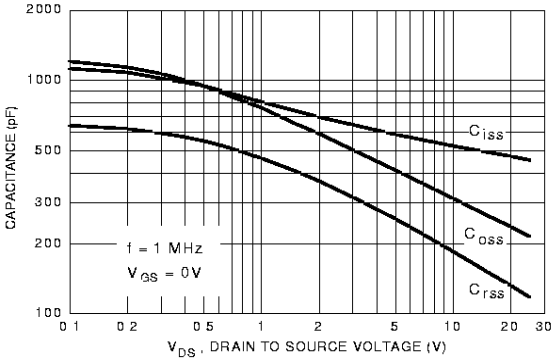


Figure 9. N-Channel Capacitance Characteristics.

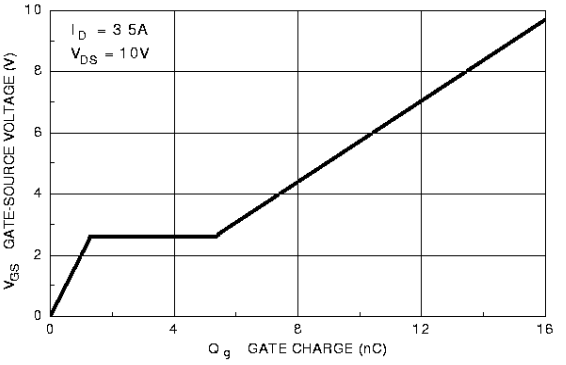


Figure 10. N-Channel Gate Charge Characteristic.

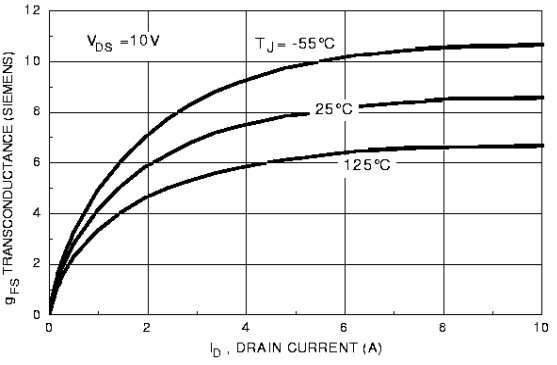


Figure 11. N-Channel Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristics: P-Channel (continued)

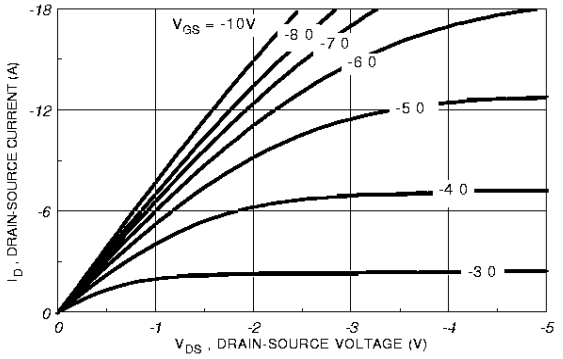


Figure 12. P-Channel On-Region Characteristics.

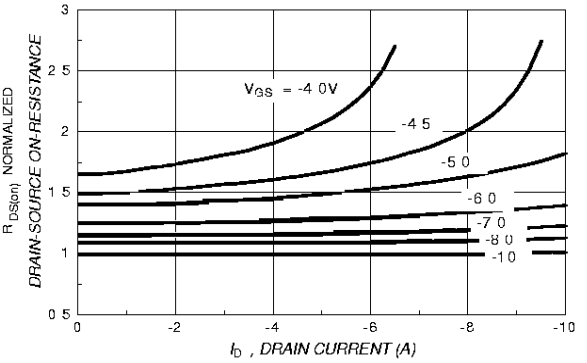


Figure 13. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

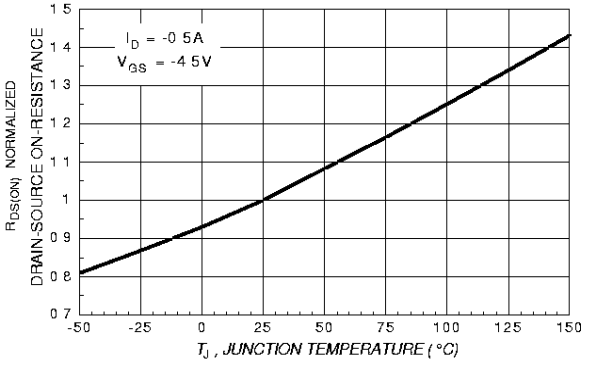


Figure 14. P-Channel On-Resistance Variation with Temperature.

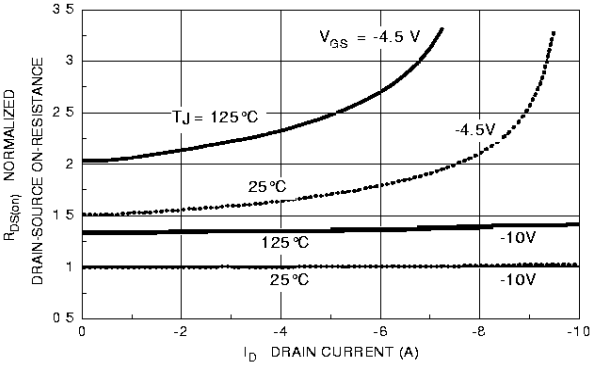


Figure 15. P-Channel On-Resistance Variation with Drain Current and Temperature.

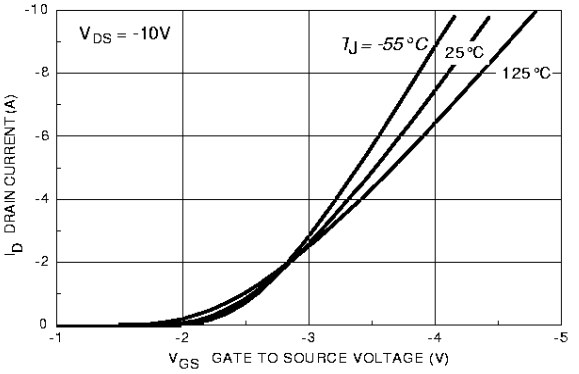


Figure 16. P-Channel Transfer Characteristics.

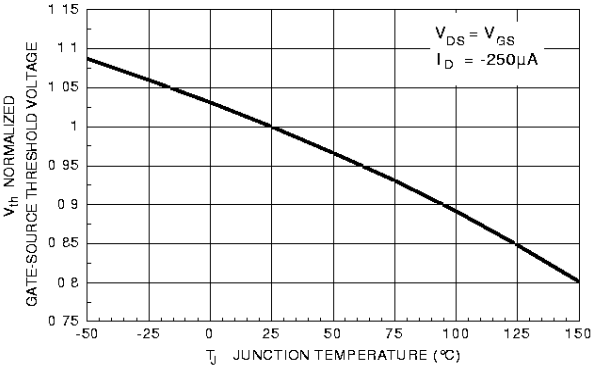


Figure 17. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: P-Channel (continued)

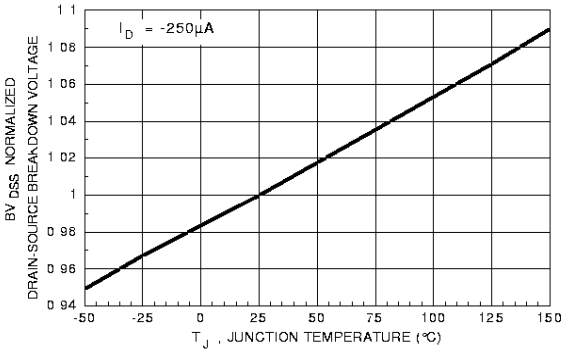


Figure 18. P-Channel Breakdown Voltage Variation with Temperature.

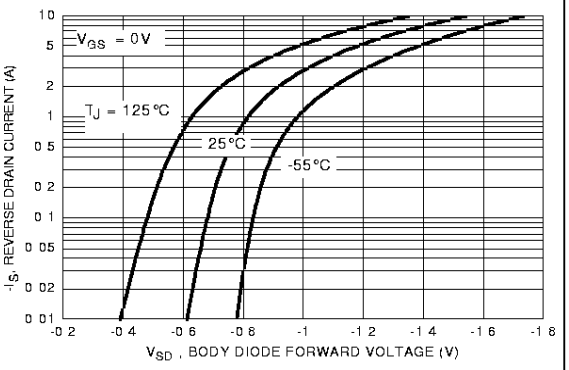


Figure 19. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

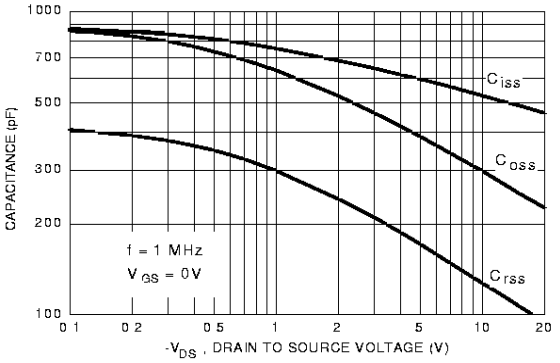


Figure 20. P-Channel Capacitance Characteristics.

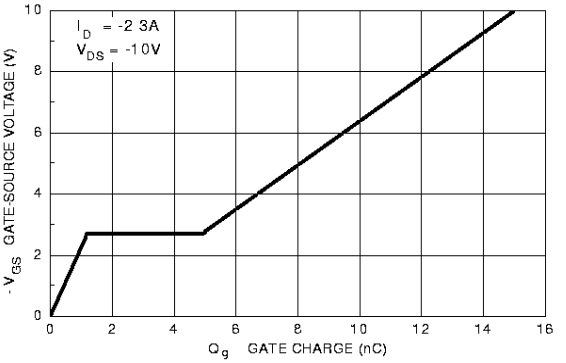


Figure 21. P-Channel Gate Charge Characteristic.

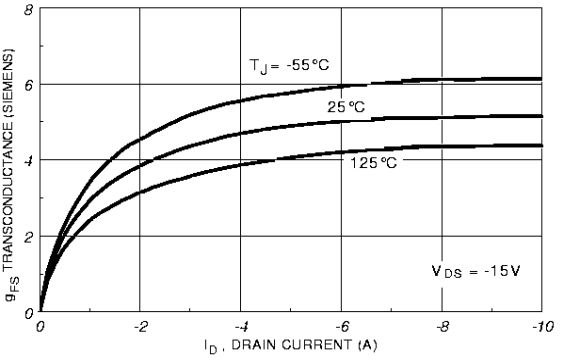


Figure 22. P-Channel Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristic: N & P-Channel (continued)

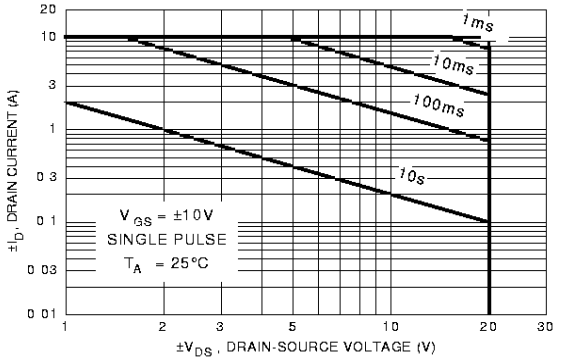


Figure 23. Maximum Safe Operating Area for both N & P-Channel.

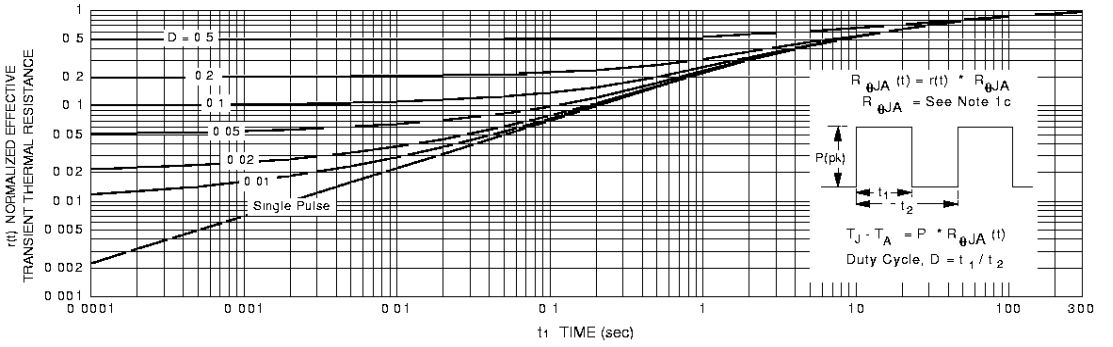


Figure 24. Transient Thermal Response Curve.

Note Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design

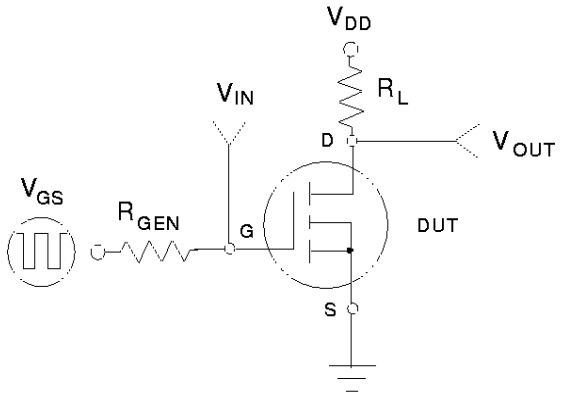


Figure 25. N or P-Channel Switching Test Circuit.

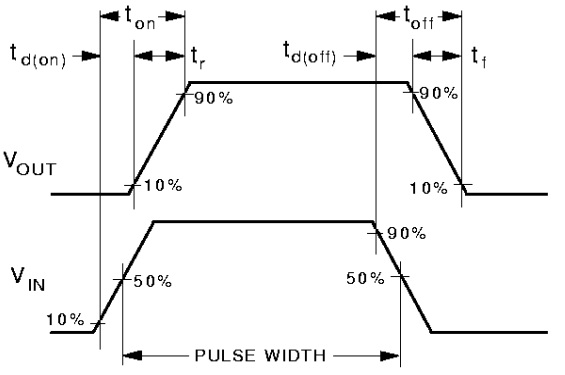


Figure 26. N or P-Channel Switching Waveforms.