8T13

DUAL SINGLE-ENDED LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 8T13 Dual Line Driver is designed for driving 50Ω to 500Ω coaxial cable, strip line, or twisted pair transmission lines. All inputs are TTL or DTL compatible and the emitter-follower outputs enable two or more drivers to operate on the same line in party line applications.

For a dual line driver to meet the IBM System/360 I/O Interface Specification, see 8T23 data sheet.

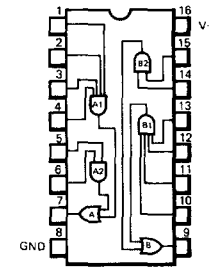
- **HIGH OUTPUT DRIVE CAPABILITY**
- **HIGH SPEED**
- **INPUT CLAMP DIODES**
- **SINGLE 5 V SUPPLY OPERATION**
- **SHORT CIRCUIT PROTECTED**

ABSOLUTE MAXIMUM RATINGS

Input Voltage (Note 1)	+5.5 V
Output Voltage (Note 1)	+7.0 V
Supply Voltage (Note 1)	+7.0 V
Storage Temperature Range	
Hermetic DIP (S8T13E, N8T13E)	−65°C to +150°C
Molded DIP (N8T13B)	−55°C to +125°C
Operating Temperature Range	
Military (S8T13)	−55°C to +125°C
Commercial (N8T13)	0°C to +75°C
Lead Temperatures	
Hermetic DIP (Soldering, 60 seconds)	300°C
Molded DIP (Soldering, 10 seconds)	260°C
Internal Power Dissipation (Note 2)	*730 mW*

NOTES:
1. Voltages are with respect to the ground pin (pin 8).
2. Rating applies to ambient temperatures up to 75°C. Above 75°C derate linearly at 8.3 mW/° C.

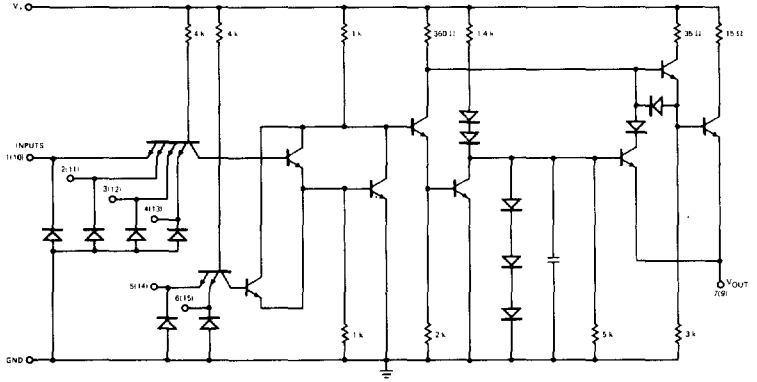
CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6B, 9B



ORDER INFORMATION

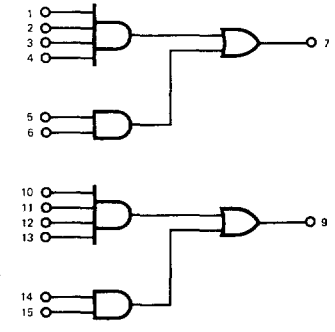
TYPE	PART NO.
S8T13	S8T13E
N8T13	N8T13E
N8T13	N8T13B

EQUIVALENT CIRCUIT *(FOR EACH DRIVER)*



NOTE: Numbers refer to package pins (side A); numbers in parentheses are pinouts (side B).

LOGIC DIAGRAM



V_+ = PIN 16
GND = PIN 8

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ELECTRICAL CHARACTERISTICS FOR S8T13 (V_+ = 5.0 V ±5%, T_A = -55°C to +125°C (Note 3))

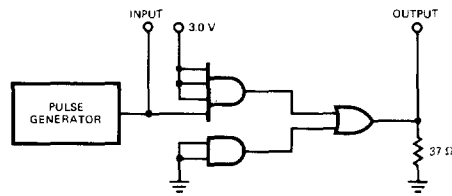
PARAMETER	TEST CONDITIONS				NOTES	LIMITS			UNITS
	AND GATE NO. 1		INPUTS OF NO. 2 AND GATE	OUTPUTS		MIN.	TYP.	MAX.	
	INPUT UNDER TEST	OTHER INPUTS							
Output HIGH Voltage	2.0 V	2.0 V	0.8 V	−75 mA	9	2.4			V
Output HIGH Leakage Current	0 V	0 V	0 V	3.0 V	10			500	μA
Output LOW Leakage Current	0.8 V	4.5 V	0 V	0.4 V				−800	μA
Input LOW Current	0.4 V	4.5 V				−0.1		−1.6	mA
Input HIGH Current	4.5 V	0 V						40	μA

ELECTRICAL CHARACTERISTICS FOR S8T13 AND N8T13 (V_+ = 5.0 V, T_A = 25°C.)

PARAMETER	TEST CONDITIONS				NOTES	LIMITS			UNITS
	AND GATE NO. 1		INPUTS OF NO. 2 AND GATE	OUTPUTS		MIN.	TYP.	MAX.	
	INPUT UNDER TEST	OTHER INPUTS							
Turn On Delay, t_{PHH}					11, 15			20	ns
					12, 15		32		ns
Turn Off Delay, t_{PLL}					11, 15			20	ns
					12, 15		22		ns
Power/Current Consumption:									
Output LOW	0.8 V	0.8 V	0.8 V		14, 17			315/60	mW/mA
Output HIGH	2.0 V	2.0 V	2.0 V		14, 17			150/28	mW/mA
Input Latch Voltage	10 mA	0 V	0 V		13	5.5			V
Output HIGH Current	4.5 V	4.5 V	0 V	2.0 V	16	−100		−250	mA
Output Short Circuit	4.5 V	4.5 V	0 V	0 V	16			−30	mA
Input Clamp Diode Voltage	−12 mA							−1.5	V

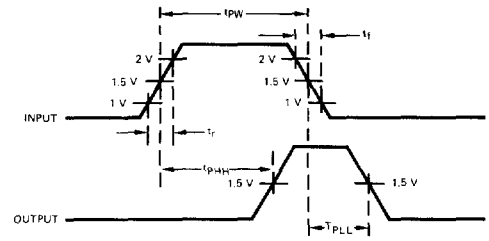
NOTES:
3. Specifications apply V_+ = 5.0 V ±5% and 0°C to 75°C for N8T13.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
5. All measurements are taken with ground pin tied to zero volts.
6. Positive current is defined as into the terminal referenced.
7. Positive logic definition: "UP" Level = HIGH, "DOWN" Level = LOW.
8. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
9. Output source current is supplied through a resistor to ground.
10. With forced output voltage of 3 V no more than 500 μA will enter the driver when output is in LOW state. V_+ = 0 V.
11. R_L = 37Ω to ground.
12. Load is 37 Ω in parallel with 1000 pF.
13. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
14. I_{CC} is dependent upon loading. I_{CC} limit specified is for no-load test condition.
15. Reference ac Test Figure and Pulse Requirements.
16. Reference "Typical Output Current as a function of Output Voltage Curve."
17. V_+ = 5.25 V. Power Consumption specified for both drivers in package.

AC TEST CIRCUIT



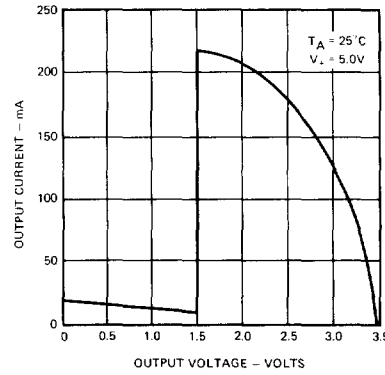
INPUT PULSE:
Amplitude = 3.0 V
t_{PW} = 40 ns (50% Duty Cycle)
$t_r = t_f \leq 5$ ns (10% and 90% measurement points)

VOLTAGE WAVEFORMS



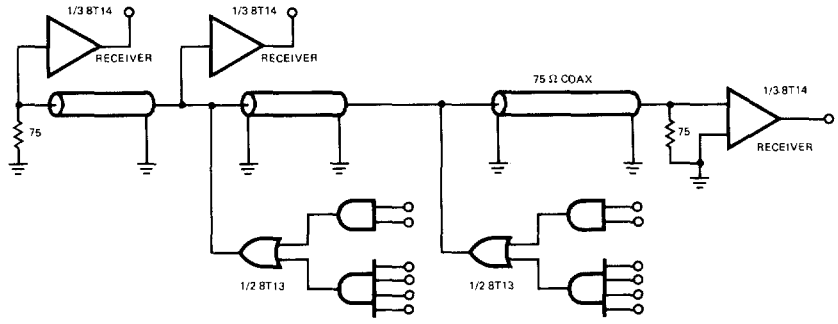
TYPICAL PERFORMANCE CURVE FOR S8T13 AND N8T13

OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



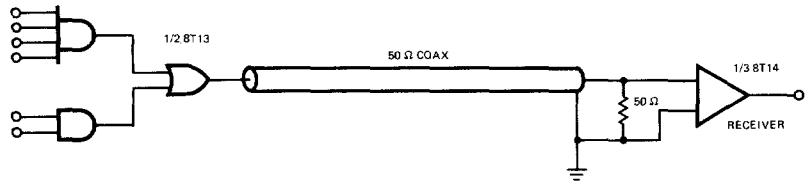
TYPICAL APPLICATIONS

75 Ω PARTY LINE (2 DRIVERS, 3 RECEIVERS)



Note: For party line operation, termination of each physical end of the line is recommended.

SIMPLEX OPERATION (1 DRIVER)



Note: For simplex operation, the line should be terminated only at the distant receiver site.

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