FAIRCHILD™

April 2016

FDD8445_F085

## N-Channel PowerTrench® MOSFET
40V, 50A, 8.7mΩ

Features

- Typ $R_{DS(on)}$ = 6.7mΩ at V_{GS} = 10V, I_D = 50A
- Typ $Q_{g(10)}$ = 45nC at V_{GS} = 10V, I_D = 50A
- Low Miller Charge
- Low Qrr Body Diode
- UIS Capability (Single Pulse/ Repetitive Pulse)
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electronic Transmission
- Distributed Power Architecture and VRMs
- Primary Switch for 12V Systems

D-PAK (TO-252)
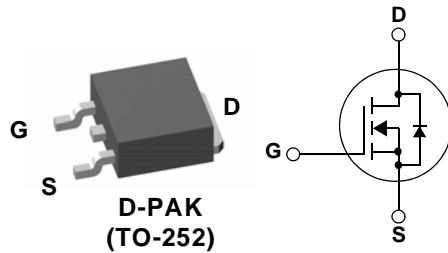
For current package drawing, please refer to the Fairchild website at http://www.fairchildsemi.com/package-drawings/TO/TO252A03.pdf.

MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain to Source Voltage		40	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current Continuous (V_{GS} = 10V)		50	A
	Pulsed		Figure 4	
E_{AS}	Single Pulse Avalanche Energy	(Note 1)	144	mJ
P_D	Power Dissipation		79	W
	Derate above 25°C		0.53	W/°C
T_J, T_{STG}	Operating and Storage Temperature		-55 to +175	°C
$R_{\theta JC}$	Thermal Resistance Junction to Case		1.9	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, 1in^2 copper pad area		52	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8445	FDD8445_F085	TO-252AA	13"	12mm	2500 units

Notes:
1: Starting T_J = 25°C, L = 0.18mH, I_{AS} = 40A
2: A suffix as "…F085P" has been temporarily introduced in order to manage a double source strategy as Fairchild has officially announced in Aug 2014.

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V		40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32V, V_{GS} = 0V		-	-	1	μA
			T_A = 150°C	-	-	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V		-	-	±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	2	2.8	4	V
$r_{DS(on)}$	Drain to Source On Resistance	I_D = 50A, V_{GS}= 10V	-	6.7	8.7	mΩ
		I_D = 50A, V_{GS}= 10V T_J = 175°C	-	12.5	16.3	

Dynamic Characteristics

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	3040	4050	pF
C_{oss}	Output Capacitance			-	295	390	pF
C_{rss}	Reverse Transfer Capacitance			-	178	270	pF
R_G	Gate Resistance	f = 1MHz		-	1.7	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0 to 10V		-	45	59	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0 to 2V	V_{DD} = 20V I_D = 50A		5.8	7.6	nC
Q_{gs}	Gate to Source Gate Charge			-	12.5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	10.5	-	nC

Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{on}	Turn-On Time	V_{DD} = 20V, I_D = 50A V_{GS} = 10V, R_{GS} = 2Ω	-	-	138	ns
$t_{d(on)}$	Turn-On Delay Time		-	10	-	ns
t_r	Rise Time		-	82	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	26	-	ns
t_f	Fall Time		-	9.6	-	ns
t_{off}	Turn-Off Time		-	-	53	ns

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 50A	-	-	1.25	V
		I_{SD} = 25A	-	-	1.0	
t_{rr}	Reverse Recovery Time	I_{SD} = 50A, dI_{SD}/dt = 100A/μs	-	-	39	ns
Q_{rr}	Reverse Recovery Charge		-	-	38	nC

Typical Characteristics
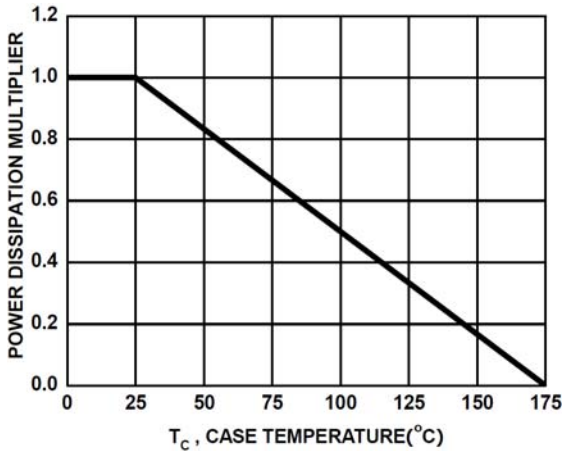

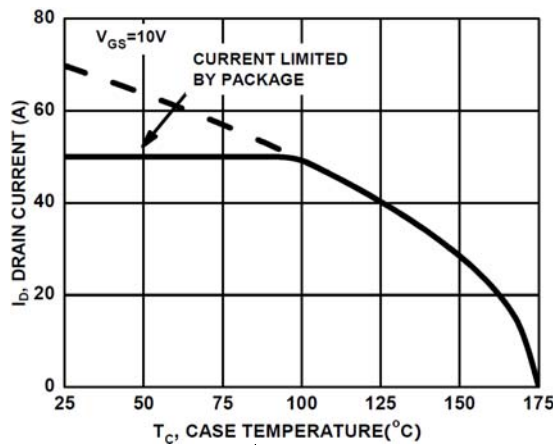Figure 1. Normalized Power Dissipation vs Case Temperature

Figure 2. Maximum Continuous Drain Current vs Case Temperature
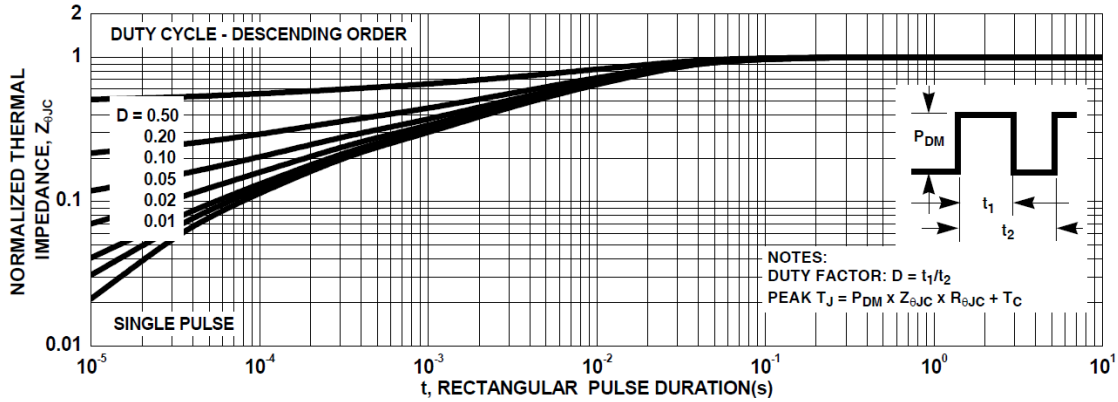

NOTES:
DUTY FACTOR: D = t_1/t_2
PEAK T_J = P_{DM} x $Z_{\theta JC}$ x $R_{\theta JC}$ + T_C

Figure 3. Normalized Maximum Transient Thermal Impedance

$$I = I_{25} \left[\sqrt{\frac{175 - T_C}{150}} \right]$$
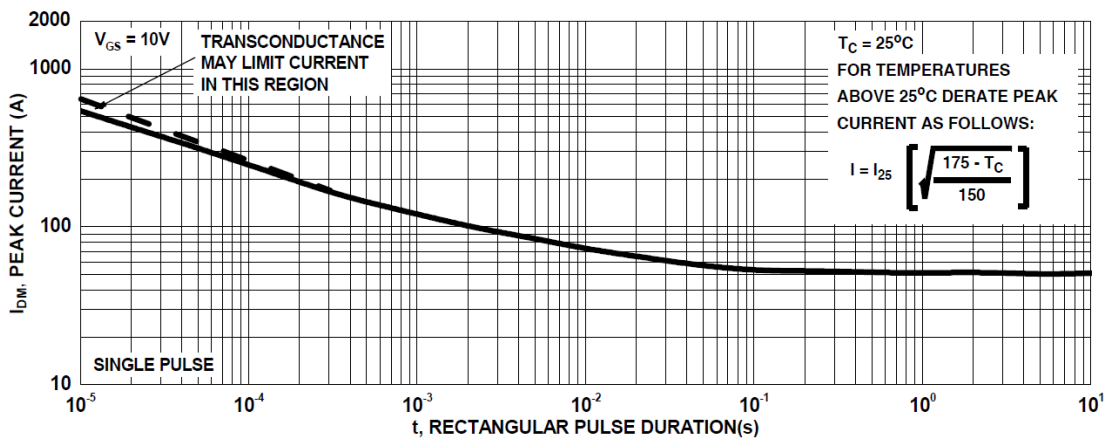
Figure 4. Peak Current Capability

FDD8445_F085 N-Channel PowerTrench® MOSFET

Typical Characteristics
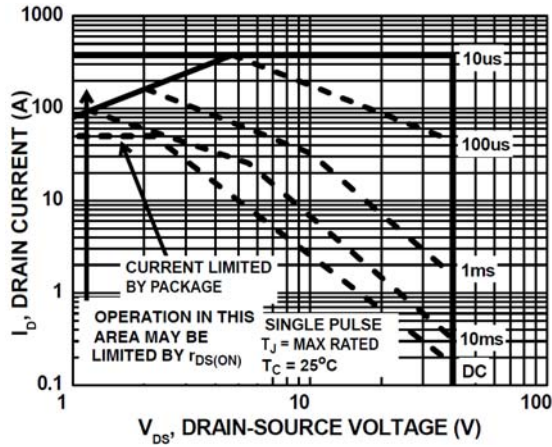
Figure 5. Forward Bias Safe Operating Area
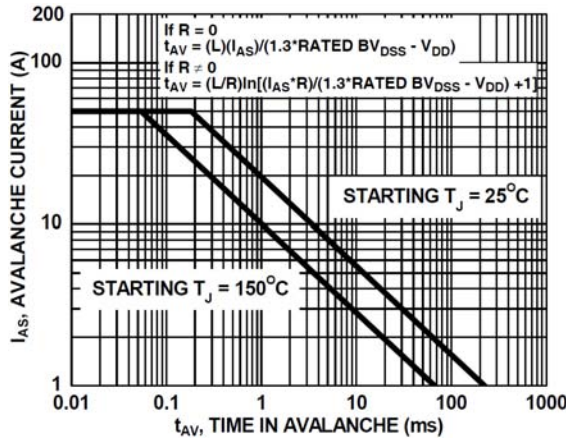
NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

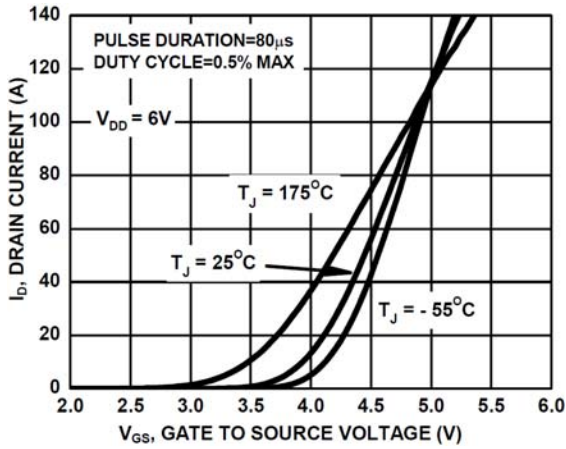Figure 6. Unclamped Inductive Switching Capability

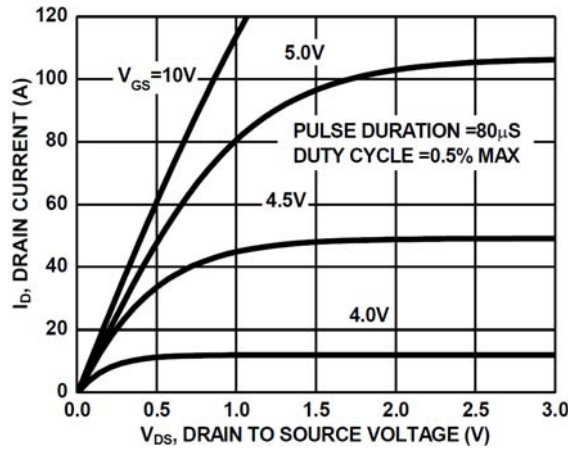Figure 7. Transfer Characteristics

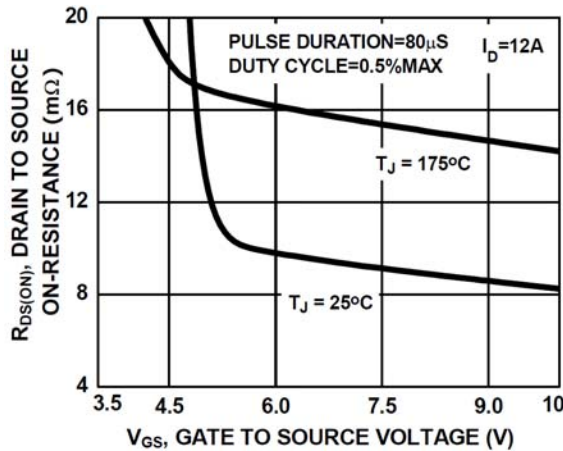Figure 8. Saturation Characteristics

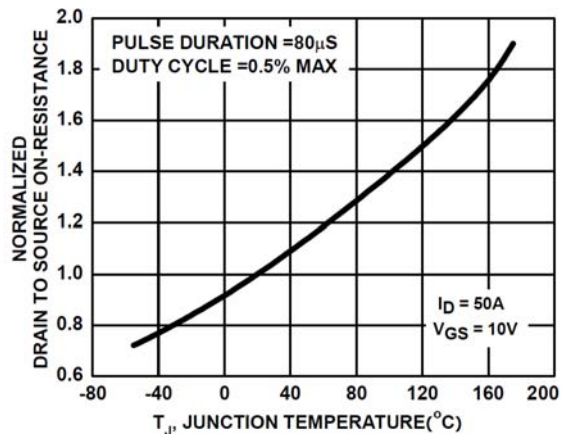Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage

Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature
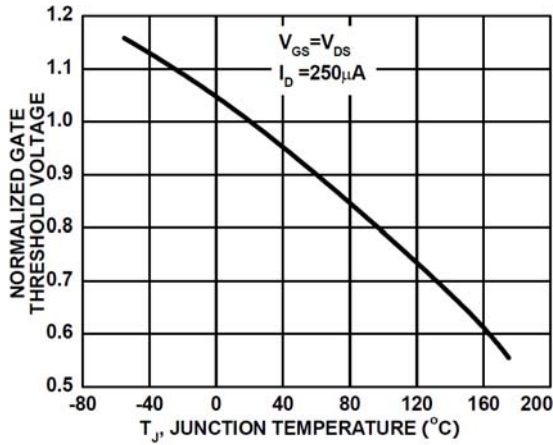
Typical Characteristics

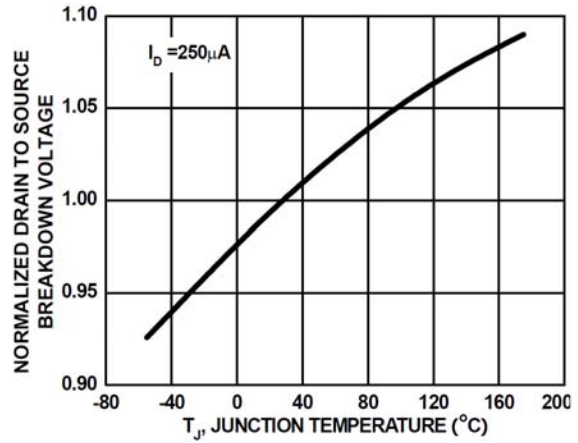**Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature**

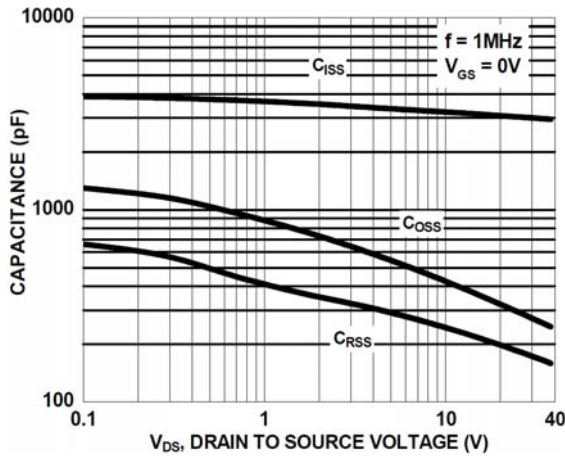**Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**

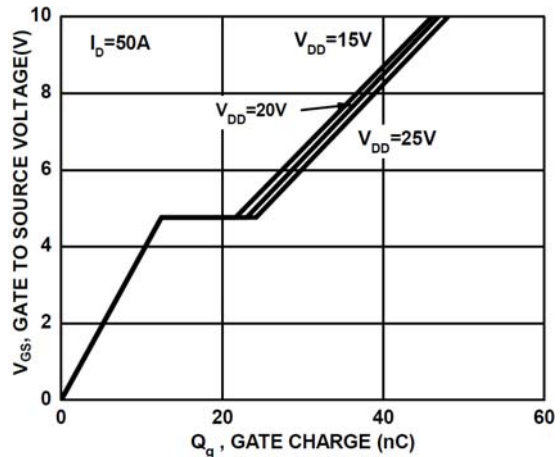**Figure 13. Capacitance vs Drain to Source Voltage**

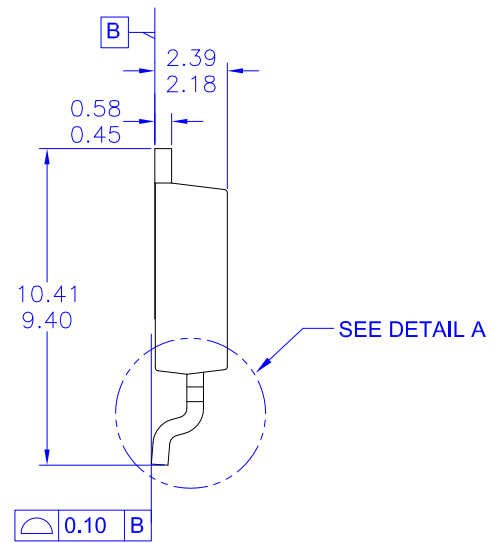**Figure 14. Gate Charge vs Gate to Source Voltage**

6.73
6.35

5.46
5.21

A

1.27
0.89

6.22
5.97

E 1.02 MAX

C

1 2 3

0.25 MAX

ISOLATED PLASTIC
BODY STUB

(0.59)

1.14
0.76

0.89
0.64

2.29

⌖ 0.25 Ⓜ AⓂ C

4.57

NON-DIODE
PRODUCTS VERSION

DIODE
PRODUCTS VERSION

5.55 MIN

4

6.50 MIN

6.40

1 3

2.85 MIN

1.25 MIN

2.28

4.56

LAND PATTERN
RECOMMENDATION

SEE
NOTE D

4.32 MIN

4

5.21 MIN

3 2 1

E

NON-DIODE
PRODUCTS VERSION

3 2 1

DIODE
PRODUCTS VERSION

B

2.39
2.18

0.58
0.45

10.41
9.40

SEE DETAIL A

⌒ 0.10 B

GAGE PLANE

0.51

0.61
0.45

10°
0°

(1.54)

1.78
1.40

0.127 MAX

(2.90)

SEATING PLANE

DETAIL A
(ROTATED -90°)
SCALE: 12X

NOTES: UNLESS OTHERWISE SPECIFIED
  A) THIS PACKAGE CONFORMS TO JEDEC, TO-252,
     ISSUE C, VARIATION AA.
  B) ALL DIMENSIONS ARE IN MILLIMETERS.
  C) DIMENSIONING AND TOLERANCING PER
     ASME Y14.5M-2009.
  D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED
     CORNERS OR EDGE PROTRUSION.
  E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
  F) DIMENSIONS ARE EXCLUSIVE OF BURS,
     MOLD FLASH AND TIE BAR EXTRUSIONS.
  G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD
     TO228P991X239-3N.
  H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11
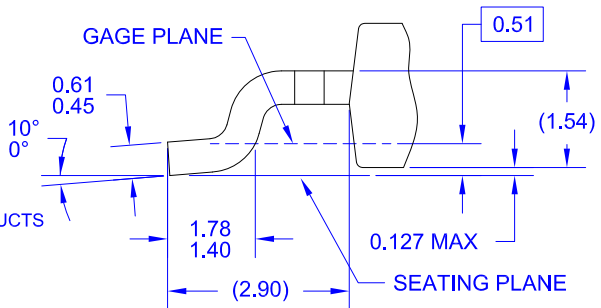
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