April 2015

FDMC86262P

P-Channel PowerTrench® MOSFET

-150 V, -2 A, 307 mΩ

Features

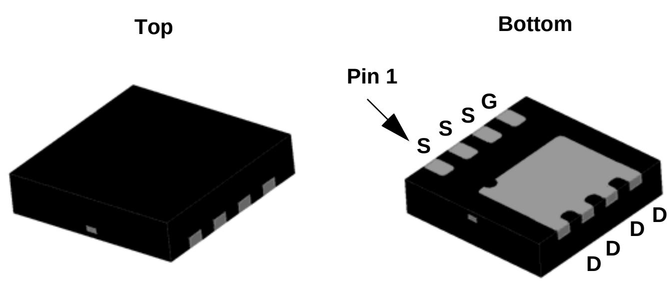
- Max $r_{DS(on)}$ = 307 mΩ at V_{GS} = -10 V, I_D = -2 A
- Max $r_{DS(on)}$ = 356 mΩ at V_{GS} = -6 V, I_D = -1.8 A
- Very Low $r_{DS(on)}$ Mid Voltage P-Channel Silicon Technology Optimised for Low Qg
- Optimised for Fast Switching Applications as well as Load Switch Applications
- 100% UIL Tested
- RoHS Compliant

General Description

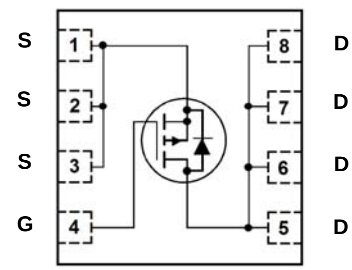
This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® technology. This very high density process is especially tailored to minimize on-state resistance and optimizad for superior switching performance.

Applications

- Active Clamp Switch
- Load Switch



MLP 3.3x3.3



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	-150	V
V_{GS}	Gate to Source Voltage	±25	V
I_D	Drain Current -Continuous T_C = 25°C (Note 5)	-8.4	A
	-Continuous T_C = 100°C (Note 5)	-5.3	
	-Continuous T_A = 25°C (Note 1a)	-2	
	-Pulsed (Note 4)	-35	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	37	mJ
P_D	Power Dissipation T_C = 25°C	40	W
	Power Dissipation T_A = 25°C (Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	3.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	53	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86262P	FDMC86262P	Power 33	13''	12 mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250 μA, V_{GS} = 0 V	-150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25°C		-86		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -120 V, V_{GS} = 0 V			-1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±25 V, V_{DS} = 0 V			±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250 μA	-2	-2.9	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25°C		5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -10 V, I_D = -2 A		241	307	mΩ
		V_{GS} = -6 V, I_D = -1.8 A		266	356	
		V_{GS} = -10 V, I_D = -2 A, T_J = 125°C		425	541	
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -2 A		5.4		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C_{iss}	Input Capacitance	V_{DS} = -75 V, V_{GS} = 0 V, f = 1MHz		632	885	pF
C_{oss}	Output Capacitance			45	65	pF
C_{rss}	Reverse Transfer Capacitance			1.3	2.0	pF
R_g	Gate Resistance		0.1	3	6	Ω

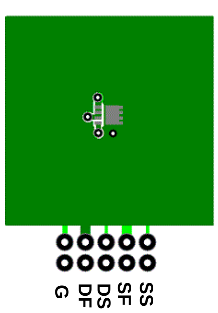
Switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -75 V, I_D = -2 A, V_{GS} = -10 V, R_{GEN} = 6 Ω		8.5	17	ns
t_r	Rise Time			2.2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			15	26	ns
t_f	Fall Time			5.6	11	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to -10 V; V_{DD} = -75 V, I_D = -2 A		9.1	13	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to -6 V; V_{DD} = -75 V, I_D = -2 A		5.6	7.9	nC
Q_{gs}	Gate to Source Charge	V_{DD} = -75 V, I_D = -2 A		2.5		nC
Q_{gd}	Gate to Drain "Miller" Charge			1.6		nC

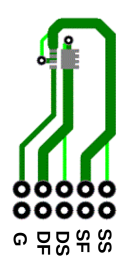
Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Source-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = -2 A (Note 2)		-0.8	-1.3	V
t_{rr}	Reverse Recovery Time	I_F = -2 A, di/dt = 100 A/μs		72	116	ns
Q_{rr}	Reverse Recovery Charge			166	266	nC

Notes:
1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 53°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 125°C/W when mounted on a minimum pad

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.
3. Starting T_J = 25°C, L = 3 mH, I_{AS} = -5 A, V_{DD} = -150 V, V_{GS} = -10 V.
4. Pulsed Id please refer to Fig 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics T_J = 25°C unless otherwise noted.

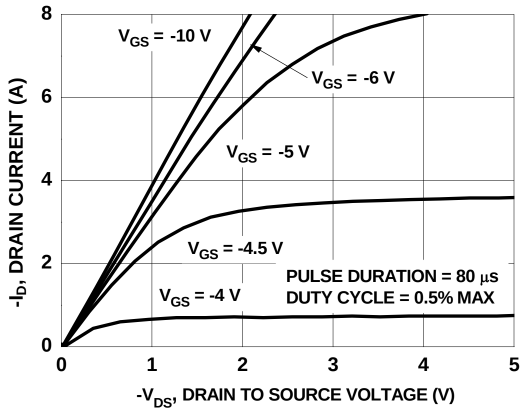


Figure 1. On Region Characteristics

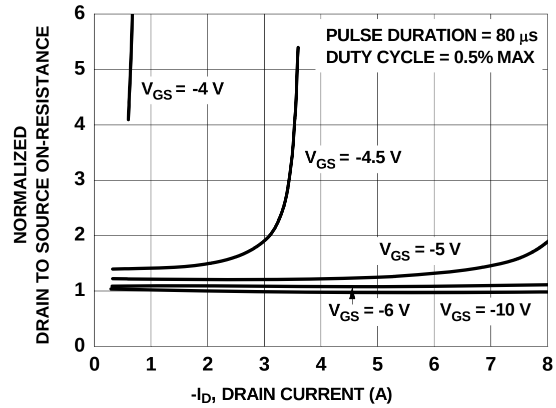


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

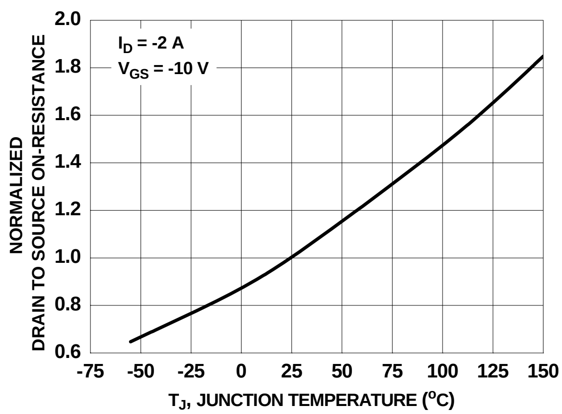


Figure 3. Normalized On Resistance vs. Junction Temperature

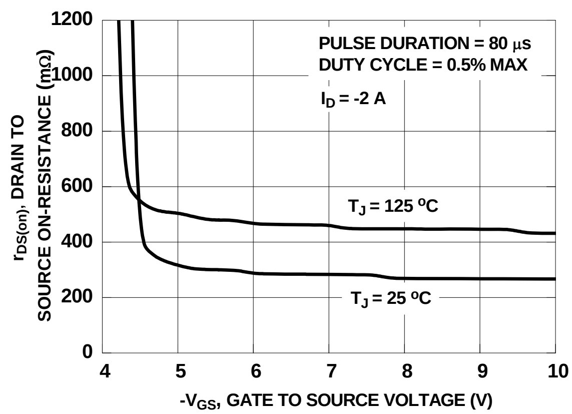


Figure 4. On-Resistance vs. Gate to Source Voltage

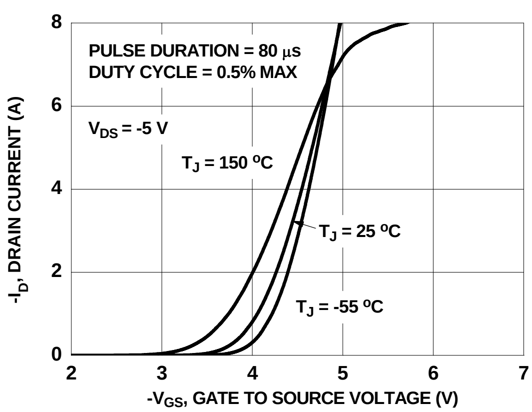


Figure 5. Transfer Characteristics

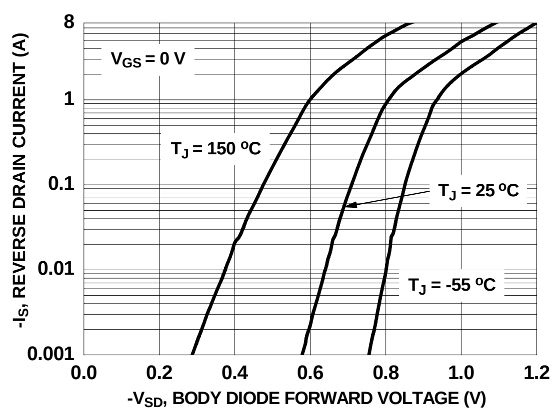


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics T_J = 25°C unless otherwise noted.

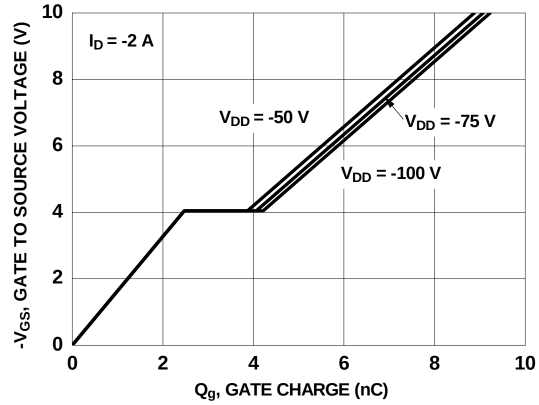


Figure 7. Gate Charge Characteristics

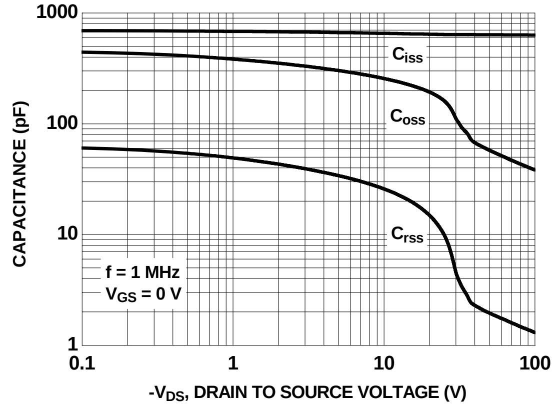


Figure 8. Capacitance vs. Drain to Source Voltage

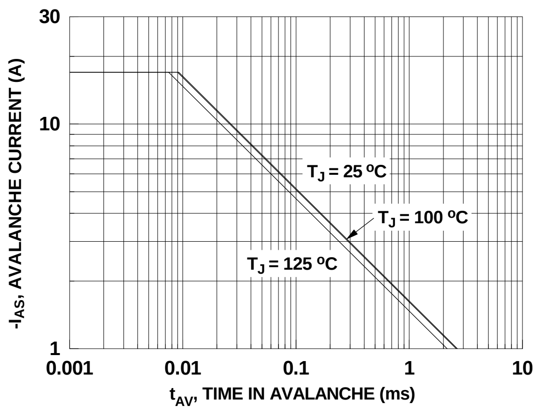


Figure 9. Unclamped Inductive Switching Capability

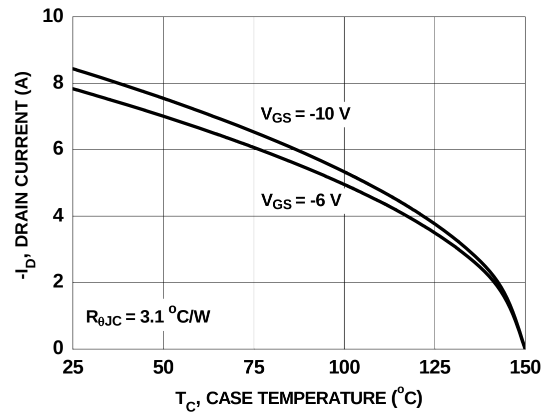


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

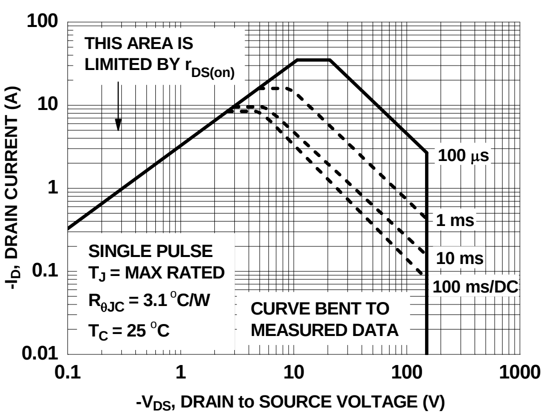


Figure 11. Forward Bias Safe Operating Area

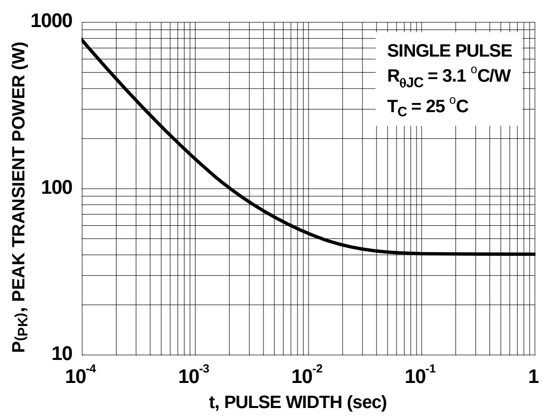


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted.

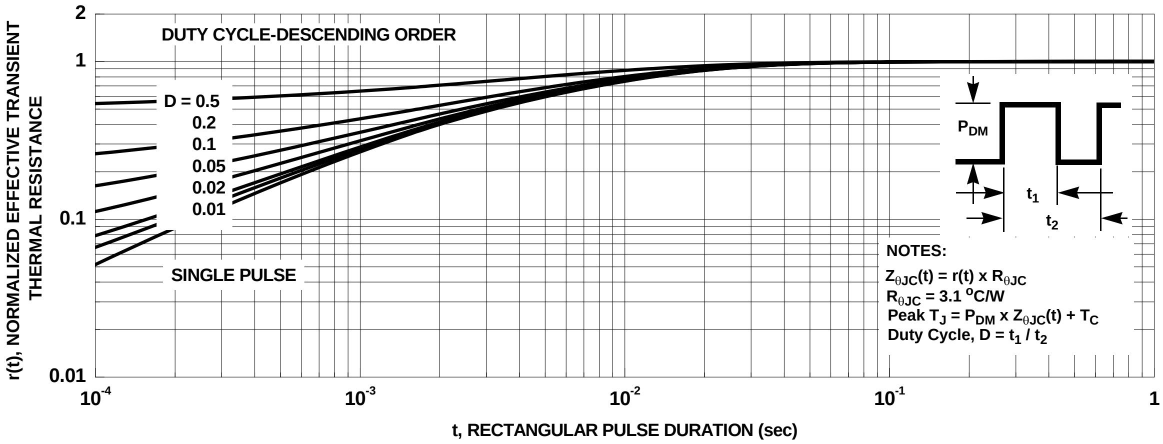
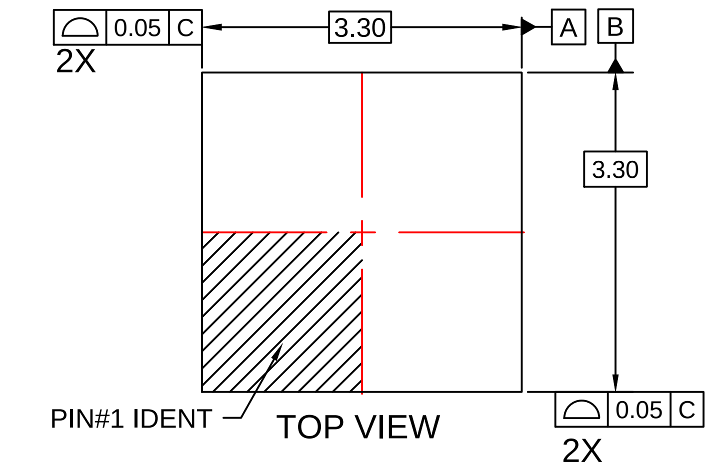
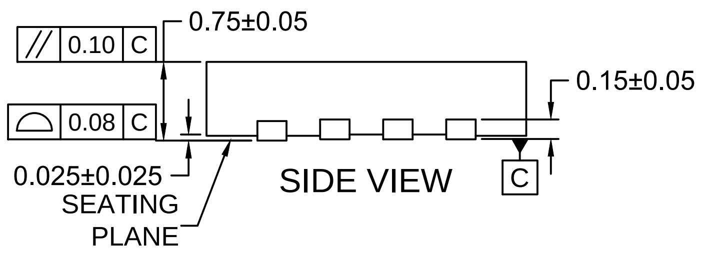


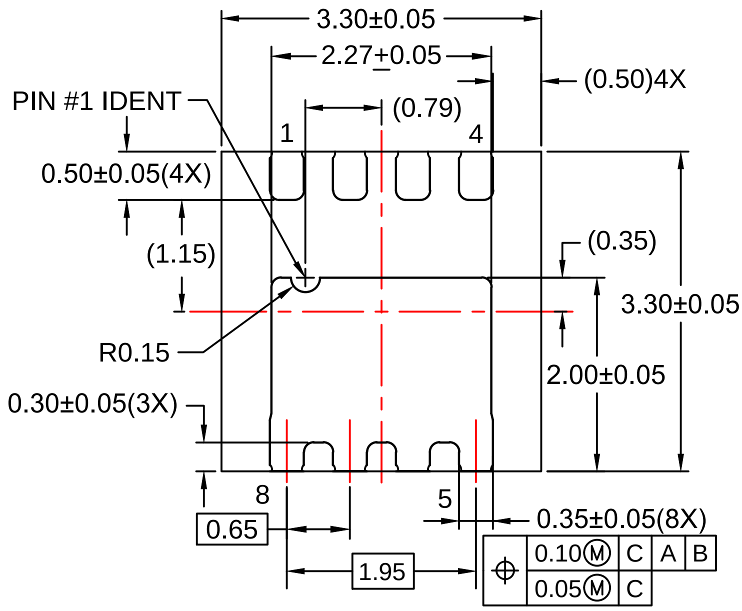
Figure 13. Junction-to-Case Transient Thermal Response Curve



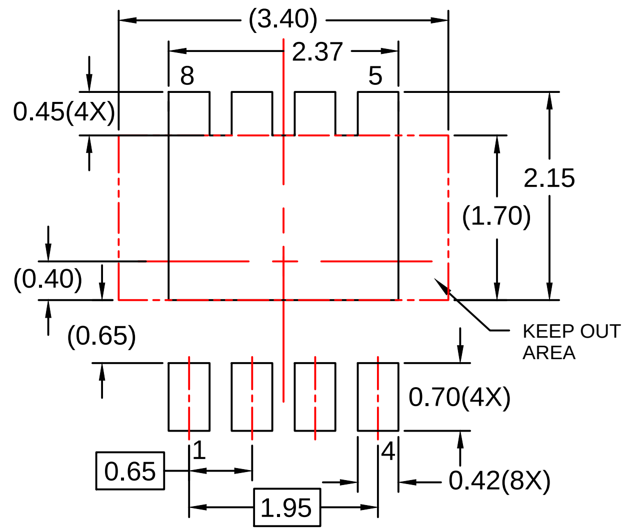
TOP VIEW



SIDE VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN

NOTES:

A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

E. DRAWING FILENAME: MKT-MLP08Srev3.

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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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