April 2015

FSA2275 — DPDT (0.5 Ω) HiFi Audio Switch w/ Negative Swing

Features

- V_{DD} Operating Range: 2.5 to 5.5 V
- External Capacitor Connection for Pop and Click Noise Suppression
- Power-Off Protection on Common Ports
- R_{ON} = 0.5 Ω (Typ.) at 2.5 V V_{DD}
- THD+N = -105 dB; 2 V_{RMS}, 20 kΩ Load; f = 1 kHz
- X_{TALK} = -134 dB at 1 V_{RMS}, 50 Ω Load; f = 1 kHz
- Off Isolation = -103 dB at 1 V_{RMS}, 50 Ω Load; f = 1 kHz
- 12-Lead UMLP 1.8 mm x 1.8 mm

Applications

- Mobile Phone, Tablet, Notebook PC, Media Player
- Docking Station, TV, Set-Top Box, LCD Monitor

Description

The FSA2275 is a high-performance, Double-Pole Double-Throw (DPDT) analog switch with negative swing audio capability. The FSA2275 features ultra-low audio R_{ON} of 0.5 Ω (typical) at 2.5 V V_{CC}. The FSA2275 operates over a V_{CC} range of 2.5 V to 5.5 V, is fabricated with sub-micron CMOS technology to achieve fast switching speeds, and is designed for break-before-make operation. To minimize pop and click during operation, the turn on ramp time is selectable using an external capacitor (C_EXT).

The FSA2275 features THD+N specifications that target a Hi-Fidelity audio quality into both 32 Ω headphones and line out type loads (>600 Ω).

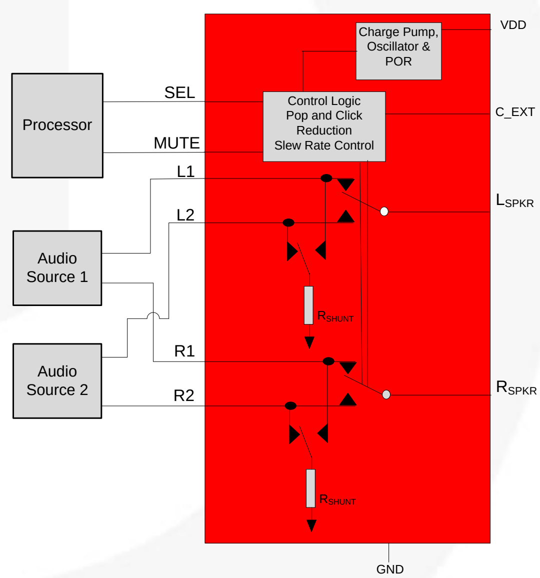


Figure 1. Application Block Diagram

Ordering Information

Part Number	Top Mark	Package Description
FSA2275UMX	NJ	12-Lead, UMLP, Quad, JEDEC MO252, 1.8 mm x1.8 mm

Pin Configuration

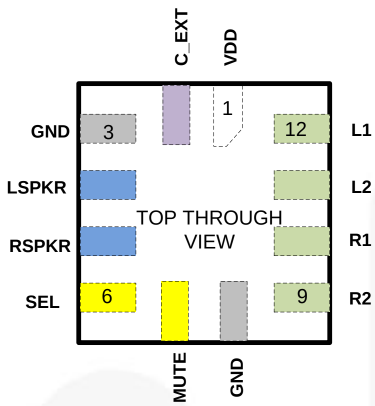


Figure 2. Pin Assignment (Top Through View)

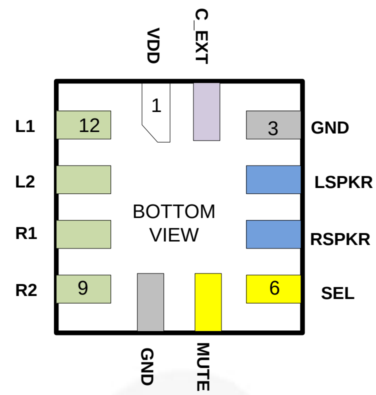


Figure 3. Pin Assignment (Bottom View)

Pin Descriptions

Pin	Name	Description
1	VDD	Power Supply (2.5 to 5.5 V)
2	C_EXT	Slow Turn On External Capacitor
3	GND	Ground
4	L_{SPKR}	Audio L_{SPPKR} Common I/O Port
5	R_{SPKR}	Audio R_{SPPKR} Common I/O Port
6	SEL	Select Pin
7	MUTE	Mute Enable - Active High
8	GND	Ground
9	R2	Audio – Right Channel Source2 I/O Port
10	R1	Audio – Right Channel Source1 I/O Port
11	L2	Audio – Left Channel Source2 I/O Port
12	L1	Audio – Left Channel Source1 I/O Port

Truth Table

Mute	SEL	Function	Resistor Terminations
0	0	L1 = L_{SPKR}; R1 = R_{SPKR}	$R_{SHUNT(s)}$ connect to L2/R2
0	1	L2 = L_{SPKR}; R2 = R_{SPKR}	$R_{SHUNT(s)}$ connect to L1/R1
1	0	L1 ≠ L_{SPKR}; L2 ≠ L_{SPKR}; R1 ≠ R_{SPKR}; R2 ≠ R_{SPKR} (All Paths Hi-Z)	$R_{SHUNT(s)}$ OPEN
1	1	L1 ≠ L_{SPKR}; L2 ≠ L_{SPKR}; R1 ≠ R_{SPKR}; R2 ≠ R_{SPKR} (All Paths Hi-Z)	$R_{SHUNT(s)}$ OPEN

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	Supply/Control Voltage		-0.3	6.0	V
V_{CNTRL}	Control Input Voltage	SEL, MUTE	-0.3	6.0	V
V_{SW}	DC Switch I/O Voltage	L1, L2, R1, R2, L_{SPKR}, R_{SPKR}	-3.5	3.5	V
I_{IK}	ESD Input Diode Current			-50	mA
I_{SW}	Switch I/O Current			700	mA
ESD	Human Body Model, ANSI/ESDA/ JEDEC JS-001-2012	All Pins	5		kV
	Charged Device Model, JEDEC: JESD22-C101		2		
	IEC 61000-4-2 System	Contact	8		
		Air Gap	15		
T_A	Absolute Maximum Operating Temperature		-40	+85	°C
T_{STG}	Storage Temperature		-65	+150	°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.5	3.3	5.5	V
V_{SW}	DC Switch I/O Voltage	L1, L2, R1, R2, L_{SPKR}, R_{SPKR}	-3.0		3.0	V
V_{CNTRL}	Control Input Voltage	SEL, MUTE	0	3.6	V_{DD}	V
I_{SW}	DC Switch I/O Current			100		mA
T_A	Ambient Operating Temperature		-40	25	+85	°C

DC Characteristics

V_{DD} = 2.5 V to 5.5 V, V_{DD} (Typ.) = 3.3 V, T_A = -40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.[1]

Symbol	Parameter	Condition	V_{DD} (V)	T_A=-40°C to +85°C			Unit
				Min.	Typ.	Max.	
V_{IH}	V_{CNTRL} Pin Input High Voltage (SEL, MUTE)	C_EXT = FLOAT		1.6		V_{DD}	V
V_{IL}	V_{CNTRL} Pin Input Low Voltage (SEL, MUTE)	C_EXT = FLOAT		0		0.4	V
I_{ON}	Switch-to-GND ON Leakage Current	L1, R1, L2, R2 = -3 V to 3 V, L_{SPKR}, R_{SPKR} = Float (I_{SW} = 0 mA) MUTE=LOW, SEL=0 or V_{DD} C_EXT = FLOAT, Figure 6	2.5 to 5.5	-1.0	0.1	1.0	µA
I_{NO_MUTE}	Switch-to-GND OFF Leakage Current (when Muted)	L1, R1, L2, R2 = -3 V to 3 V, L_{SPKR}, R_{SPKR} = Float (I_{SW} = 0 mA) MUTE = HIGH, SEL = 0 or V_{DD} C_EXT = FLOAT, Figure 5	2.5 to 5.5	-1.0	0.1	1.0	µA
I_{OFF}	Input Leakage Current[2]	L1, R1, L2, R2 = -3 V to 3 V, L_{SPKR}, R_{SPKR} = Float (I_{SW} = 0 mA) MUTE = LOW, SEL = 0 or V_{DD}, C_EXT = FLOAT	0	-1.0	0.1	1.0	µA
I_{IN}	Control Input Leakage Current[3] (SEL, MUTE)	L1, R1, L2, R2 = -3 V to 3 V, L_{SPKR}, R_{SPKR} = Float (I_{SW} = 0 mA), C_EXT = FLOAT	2.5 to 5.5	-0.5	0.1	0.5	µA
I_{DD}	V_{DD} Supply Current	MUTE = LOW, SEL = 0 or $V_{DD,}$ C_EXT = FLOAT	5.5		7	18	µA
I_{DDZ}	V_{DD} Hi-Z Supply Current	MUTE = HIGH, SEL = 0 or $V_{DD,}$ C_EXT = FLOAT	5.5			1	µA
I_{DDT}	Increase in I_{DD} per Control Voltage	MUTE = LOW, SEL = 0 or 1.8 V SEL = LOW, MUTE = 0 or 1.8 V C_EXT = FLOAT	5.5			15	µA
R_{ON}	Switch On Resistance	I_{SW} = 100 mA, V_{SW} = -3 V to 3 V C_EXT = FLOAT, Figure 4	2.5 to 5.5		0.5	1.0	Ω
ΔR_{ON}	On Resistance Matching, Channel to Channel	I_{SW} = 100 mA, V_{SW} = -3 V to 3 V C_EXT = FLOAT	2.5 to 5.5		65		mΩ
R_{FLAT}	On Resistance Flatness	I_{SW} = 100 mA, V_{SW} = -3 V to 3 V C_EXT = FLOAT	2.5 to 5.5		1	8	mΩ
R_{SHUNT}	Click and Pop Resistance (L1, L2, R1, R2, L_{SPKR}, R_{SPKR})	V_{LX_RX} = 3.0 V, MUTE = 0, SEL = 0 or V_{DD}, C_EXT = FLOAT		6	10	14	kΩ

Notes:
1. Limits over the recommended temperature operating range (T_A = -40°C to +85°C) are correlated by statistical quality.
2. Only valid for V_{SW} > 0 V.
3. $V_{MUTE} \leq V_{DD}$ + 0.3 otherwise additional input leakage current may flow.

AC Characteristics

V_{DD} = 2.5 V to 5.5 V, V_{DD} (Typ.) = 3.3 V. T_A = -40°C to 85°C. T_A (Typ.) = 25°C, unless otherwise specified

Symbol	Parameter	Condition		V_{DD} (V)	T_A=- 40°C to +85°C			Unit
					Min.	Typ.	Max.	
t_{MUTE_ON}	Enable Time (MUTE to Output)	L1 = R1 = L2 = R2 = 1.5 V, L_{SPKR} , R_{SPKR} = 50 Ω to GND SEL= 0 or V_{DD}; See Figure 7 and Figure 8	C_EXT=Float	2.5, 3.3, 5.5		0.4		ms
			C_EXT=0.1 µF			100		
t_{ON_MUTE}	Disable Time (MUTE to Output)	L1 = R1= L2 = R2 = 1.5 V, L_{SPKR} , R_{SPKR} = 50 Ω to GND, SEL = 0 or V_{DD}; See Figure 7 and Figure 8	C_EXT=Float	2.5, 3.3, 5.5		20		µs
			C_EXT=0.1 µF			20		
t_{ON_SEL}	Turn On Time (SEL to Output)	L1 (L2) = R1 (R2) = 1.5 V, L2 (L1) = R2 (R1) = 0 V L_{SPKR} , R_{SPKR} = 50 Ω to GND, SEL = 0 or V_{DD}; MUTE = 0 See Figure 7 and Figure 8	C_EXT=Float	2.5, 3.3, 5.5		0.4		ms
			C_EXT=0.1 µF			100		
t_{OFF_SEL}	Turn On Time (SEL to Output)	L1 (L2) = R1 (R2) = 1.5 V, L2 (L1) = R2 (R1) = 0 V L_{SPKR} , R_{SPKR} = 50 Ω to GND, SEL= 0 or V_{DD}; MUTE = 0 See Figure 7 and Figure 8	C_EXT=Float	2.5, 3.3, 5.5		20		µs
			C_EXT=0.1 µF			20		
t_{BBM}	Break Before Make Time (SEL to Output)	L1 (L2) = R1 (R2) = 1.5 V, L_{SPKR}, R_{SPKR} = 50 Ω to GND,SEL = 0 or V_{DD}; C_EXT = FLOAT, MUTE = 0 V; See Figure 7 and Figure 9		3.3		400		µs
$dV/dt_{\_PCS}$	Pop n Click Suppression Output Voltage Ramp Rate	L1 = L2 = +60 mV, R1 = R2 = -60 mV, L_{SPKR}, R_{SPKR} = 50 Ω to GND, SEL = 0 or V_{DD}; C_EXT = 0.1 µF, MUTE = HL Transition		3.3		4.6		V/s
O_{IRR}	Off Isolation	f = 1 kHz, R_L = 50 Ω, C_L = 0 pF, MUTE = 0 V_{SW} =1 V_{RMS} Figure 11		3.3		-103		dB
		f = 1 MHz, R_L = 50 Ω, C_L = 0 pF, MUTE = 0 V_{SW} = 1 V_{RMS} Figure 11				-92		
O_{IRRM}	Off Isolation-Muted	f = 1 kHz, R_L = 50 Ω, C_L = 0 pF, MUTE = V_{DD}; V_{SW} = 1 V_{RMS} Figure 11		3.3		-108		dB
		f = 1 MHz, R_L = 50 Ω, C_L = 0 pF, MUTE = V_{DD}; V_{SW} = 1 V_{RMS} Figure 11				-99		
X_{TALK}	Cross Talk (Adjacent)	f = 1 kHz, R_L = 50 Ω, V_{SW} = 1 V_{RMS} Figure 12		3.3		-134		dB
BW	-3 dB Bandwidth	R_L = 50 Ω Figure 10		3.3		230		MHz
PSRR	Power Supply Rejection Ratio	V_{PRSS} = V_{DD} + 100 mV_{RMS} R_L = 20 kΩ or 32 Ω (at L_{SPKR}, R_{SPKR}), MUTE = 0 or V_{DD} V_{SW} = GND or Float	f = 217 Hz	3.3		-111		dB
			f = 1 kHz			-103		
			f = 20 kHz			-89		
THD+N	Total Harmonic Distortion + Noise	R_L = 20 kΩ, f = 1 kHz, V_{SW} = 2 V_{RMS} Non-A-weighted, Figure 15		3.3		0.0006		%
						-105		dB
		R_L=600 Ω, f = 1 kHz, V_{SW} = 2 V_{RMS} Non-A-weighted, Figure 15		3.3		.0006		%
						-105		dB
		R_L = 32 Ω, f = 1 kHz, V_{SW} = 0.707 V_{RMS} (2 V_{pk-pk}) Non-A-weighted, Figure 15		3.3		0.0009		%
						-101		dB

Capacitance

Unless otherwise stated, V_{DD} = 2.5 V to 5.5 V, V_{DD} (Typ.) = 3.3 V, T_A = -40°C to 85°C, and T_A (Typ.) = 25°C.(4)

Symbol	Parameter	Condition		V_{CC} (V)	T_A=- 40°C to +85°C			Unit
					Min.	Typ.	Max.	
C_{ON}	On Capacitance (Common Port)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias MUTE = 0 V Figure 14		3.3		22		pF
C_{OFF1}	Off Capacitance (Common Port)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias MUTE = V_{DD} Figure 13		3.3		25		pF
C_{OFF2}	Off Capacitance (Non-Common Ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias MUTE = 0 V Figure 13		3.3		14		pF
C_{OFF_MUTE}	Off Capacitance - MUTED (Non-Common Ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias, MUTE = V_{DD}		3.3		14		pF
C_{CNTRL}	Control Input Pin Capacitance (MUTE, SEL)	f = 1 MHz, 100 mV_{PP}, 100 mV DC bias	SEL	0		3		pF
			MUTE			6		

Note:

4. Limits over the recommended temperature operating range (T_A=-40°C to +85°C) are correlated by statistical quality control methods.

Test Diagrams

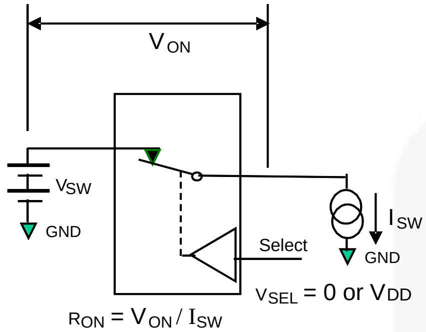


Figure 4. On Resistance

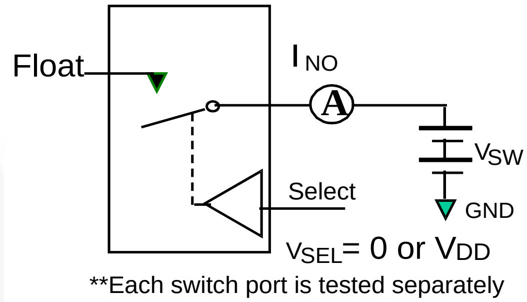


Figure 5. Off Leakage

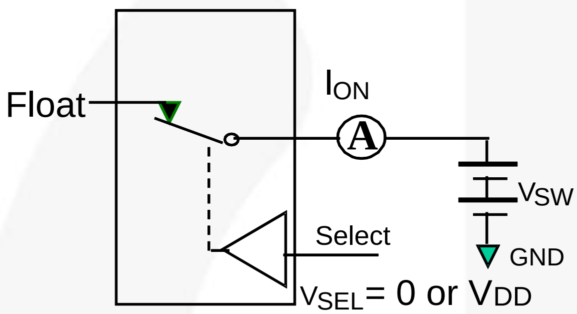


Figure 6. On Leakage

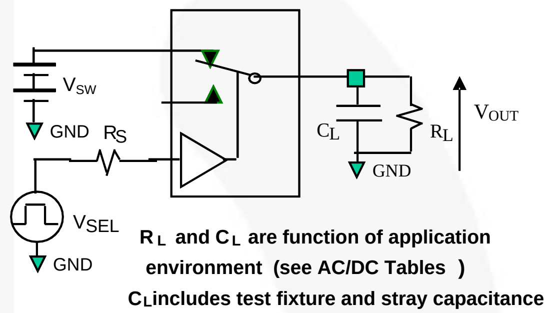


Figure 7. Test Circuit Load

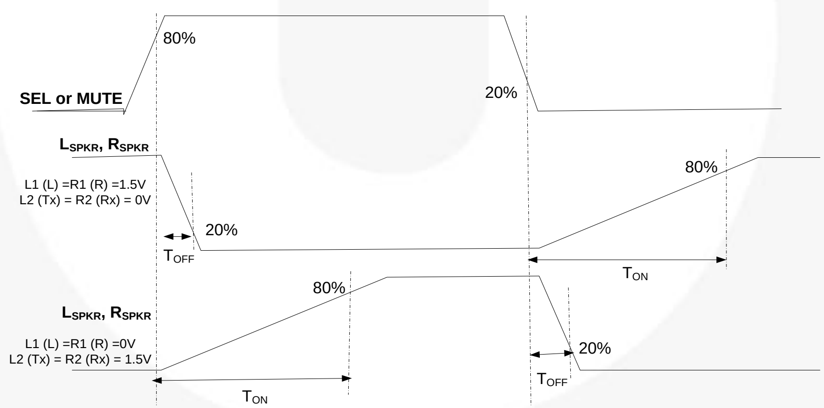


Figure 8. Turn On/Off Waveforms (SEL or MUTE to Output)

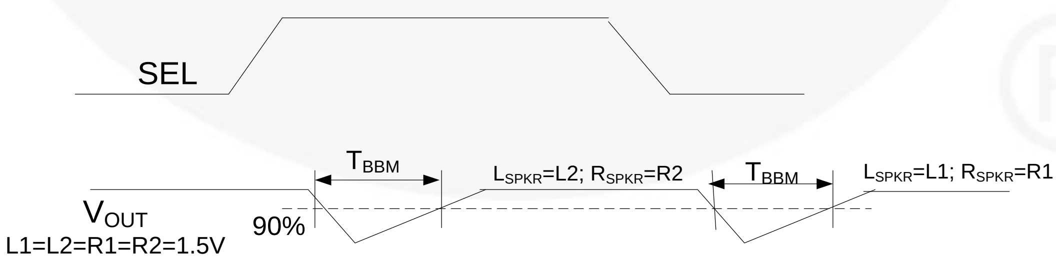


Figure 9. Break Before Make Interval Timing

Test Diagrams (Continued)

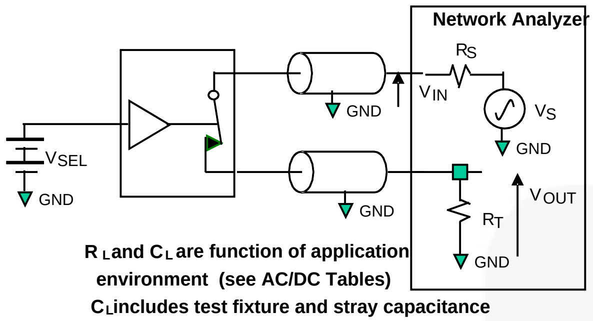


Figure 10. Bandwidth

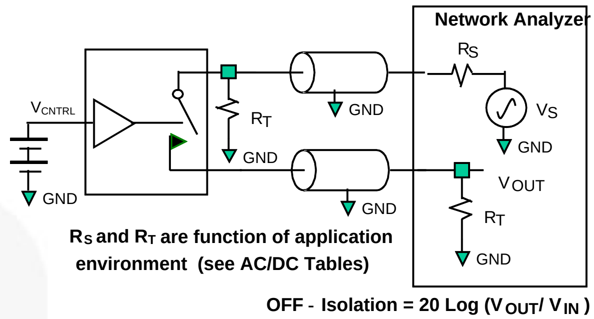


Figure 11. Channel Off Isolation

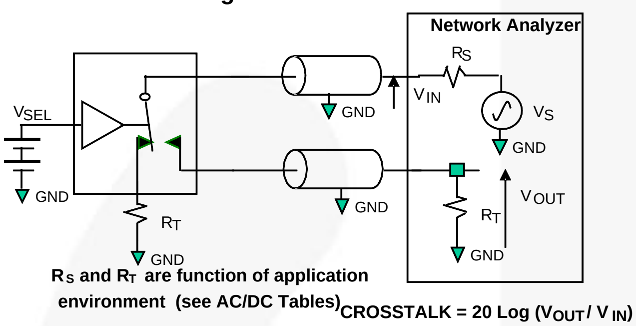


Figure 12. Adjacent Channel Crosstalk

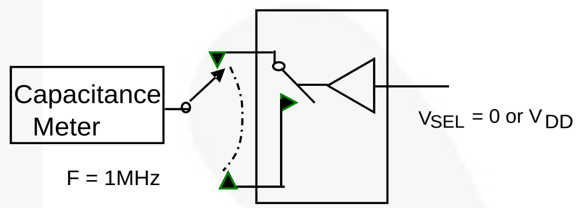


Figure 13. Channel Off Capacitance

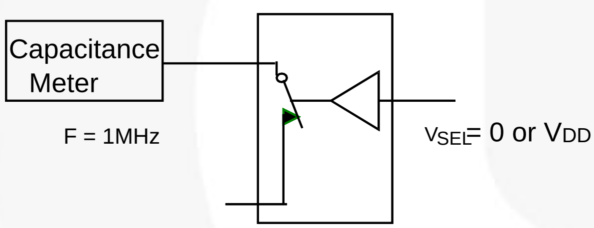


Figure 14. Channel On Capacitance

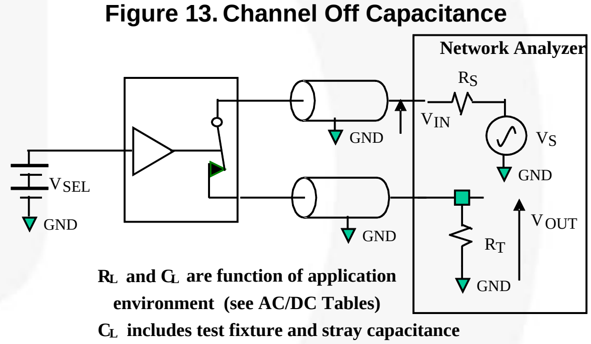
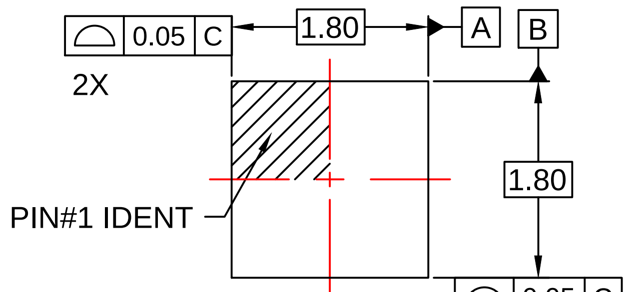
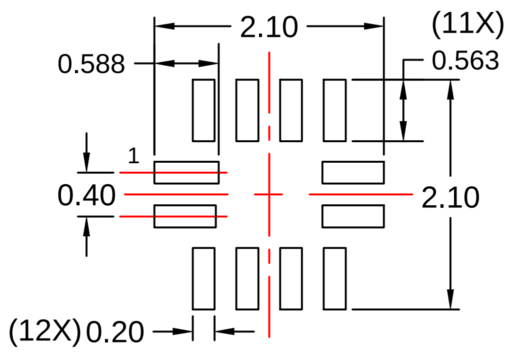


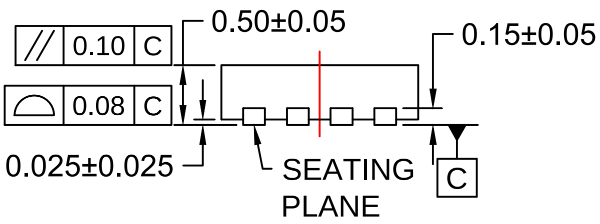
Figure 15. Total Harmonic Distortion (THD+N)



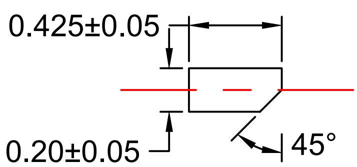
TOP VIEW



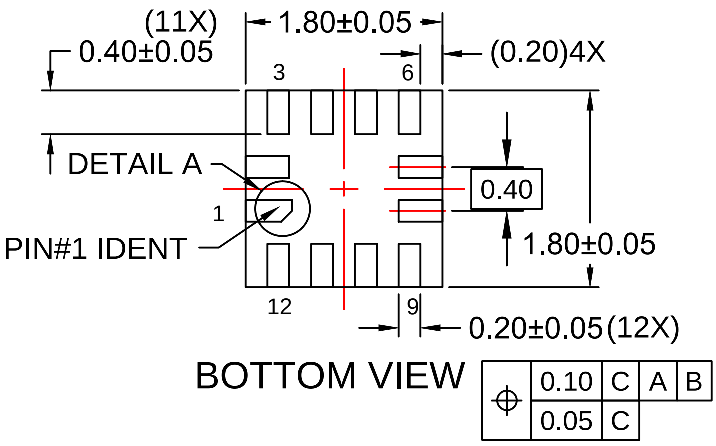
RECOMMENDED
LAND PATTERN



SIDE VIEW



DETAIL A
SCALE : 2X



BOTTOM VIEW

LEAD
OPTION 1
SCALE : 2X

LEAD
OPTION 2
SCALE : 2X

NOTES:

A. PACKAGE DOES NOT CONFORM TO ANY JEDEC STANDARD.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

E. DRAWING FILENAME: MKT-UMLP12Arev5.

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Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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