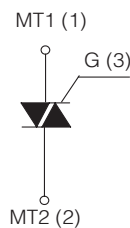
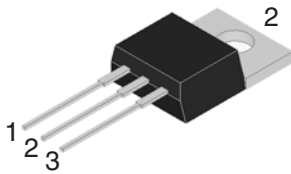


## LOGIC LEVEL TRIAC

### TO-220AB


**On-State Current**

8 Amp

**Gate Trigger Current**

&lt; 10 mA

**Off-State Voltage**

400 V ÷ 800 V

**FEATURES**

- Glass/passivated die junctions
- Medium current Triac
- Ideal for automated placement
- Low thermal resistance
- High surge current capability
- Low forward voltage drop
- Solder dip 260°C, 10s
- Component in accordance to RoHS 2011/65/EU and WEEE 2002/96/EC
- Meets MSL level 3, per J-STD-020, LF maximum peak of 260° C


**RoHS**  
COMPLIANT

**MECHANICAL DATA**

- **Case:** TO-220AB. Epoxy meets UL 94V-0 flammability rating.
- **Polarity:** As marked on the body.
- **Terminals:** Matte tin plated leads, solderable per MIL-STD-750 Method 2026, J-STD-002 and JESD22-B102. Consumer grade, meets JESD 201 class 1A whisker test.

**TYPICAL APPLICATIONS**

Logic level versions are designed to interface directly with low power drivers such as microcontrollers.

## Maximun Ratings and Electrical Characteristics at 25°C

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
$I_{T(RMS)}$	RMS On-state Current (full sine wave)	All Conduction Angle, $T_c = 95^\circ C$	8	A
$I_{TSM}$	Non-repetitive On-State Current	Full Cycle, 60 Hz ( $t = 16.7$ ms)	84	A
$I_{TSM}$	Non-repetitive On-State Current	Full Cycle, 50 Hz ( $t = 20$ ms)	80	A
$I^2t$	Fusing Current	$t_p = 10$ ms, Half Cycle	36	A <sup>2</sup> s
$I_{GM}$	Peak Gate Current	20 $\mu$ s max. $T_j = 125^\circ C$	4	A
$P_{G(AV)}$	Average Gate Power Dissipation	$T_j = 125^\circ C$	1	W
$di/dt$	Critical rate of rise of on-state current	$I_G = 2 \times I_{GT}$ , $t_r \leq 100$ ns $f = 120$ Hz, $T_j = 125^\circ C$	50	A/ $\mu$ s
$T_j$	Operating Temperature		(-40 +125)	°C
$T_{stg}$	Storage Temperature		(-40 +150)	°C
$T_{sld}$	Soldering Temperature	10s max	260	°C

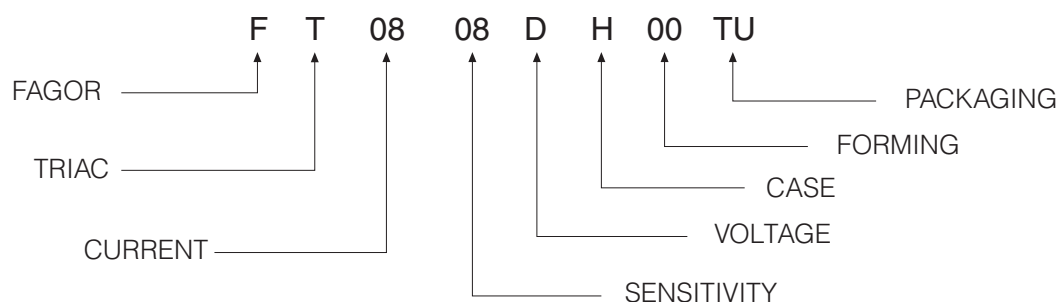
SYMBOL	PARAMETER	VOLTAGE			Unit
		D	M	N	
$V_{DRM}/V_{RRM}$	Repetitive Peak Off State Voltage	400	600	800	V

**LOGIC LEVEL TRIAC**
**Electrical Characteristics at Tamb = 25 °C**

SYMBOL	PARAMETER	CONDITIONS	Quadrant		SENSITIVITY					Unit
					03	04	07	08	09	
I <sub>GT</sub> <sup>(1)</sup>	Gate Trigger Current	V <sub>D</sub> = 12 V <sub>DC</sub> , R <sub>L</sub> = 33Ω, T <sub>j</sub> = 25 °C	Q1÷Q3	MAX	3	5	5	10	10	mA
			Q4	MAX	5		7		10	mA
V <sub>GT</sub>	Gate Trigger Voltage	V <sub>D</sub> = 12 V <sub>DC</sub> , R <sub>L</sub> = 33Ω, T <sub>j</sub> = 25 °C	Q1÷Q3	MAX	1.3					V
			Q4	MAX	1.3		1.3		1.3	V
V <sub>GD</sub>	Gate Non Trigger Voltage	V <sub>D</sub> = V <sub>DRM</sub> , R <sub>L</sub> = 3.3 KΩ, T <sub>j</sub> = 125 °C	Q1÷Q3	MIN	0.2					V
			Q4	MIN	0.2		0.2		0.2	V
I <sub>H</sub> <sup>(2)</sup>	Holding Current	I <sub>T</sub> = 100 mA, Gate open, T <sub>j</sub> = 25 °C		MAX	7	15	15	15	20	mA
I <sub>L</sub>	Latching Current	I <sub>G</sub> = 1.2 I <sub>GT</sub> , T <sub>j</sub> = 25 °C	Q1,Q3	MAX	7	25	20	25	20	mA
			Q4	MAX	7		20		20	mA
			Q2	MAX	20	30	30	30	25	mA
dV/dt <sup>(2)</sup>	Critical Rate of Voltage Rise	V <sub>D</sub> = 0.67 × V <sub>DRM</sub> , Gate open T <sub>j</sub> = 125 °C		MIN	10	40	20	40	50	V/μs
(di/dt) <sub>c</sub> <sup>(2)</sup>	Critical Rate of Current Rise	(dv/dt) <sub>c</sub> = 0.1 V/μs, T <sub>j</sub> = 125 °C		MIN	1.2	5.4	3.5	5.4	2.5	A/ms
		(dv/dt) <sub>c</sub> = 10 V/μs, T <sub>j</sub> = 125 °C		MIN	0.6	2.8	1.5	2.8	1.5	A/ms
		without snubber, T <sub>j</sub> = 125 °C		MIN						
V <sub>TM</sub> <sup>(2)</sup>	On-state Voltage	I <sub>T</sub> = 11 Amp, tp = 380 μs, T <sub>j</sub> = 25 °C		MAX	1.55					V
V <sub>t(o)</sub> <sup>(2)</sup>	Threshold Voltage	T <sub>j</sub> = 125 °C		MAX	0.85					V
r <sub>d</sub> <sup>(2)</sup>	Dynamic resistance	T <sub>j</sub> = 125 °C		MAX	50					mΩ
I <sub>DRM</sub> /I <sub>RRM</sub>	Off-State Leakage Current	V <sub>D</sub> = V <sub>DRM</sub> , T <sub>j</sub> = 125 °C		MAX	1					mA
		V <sub>R</sub> = V <sub>RRM</sub> , T <sub>j</sub> = 25 °C		MAX	5					μA
R <sub>th(j-c)</sub>	Thermal Resistance Junction-Case	for AC 360° conduction angle			1.6					°C/W
R <sub>th(j-a)</sub>	Thermal Resistance Junction-Ambient				60					°C/W

(1) Minimum I<sub>GT</sub> is guaranteed at 5% of I<sub>GT</sub> max.

(2) For either polarity of electrode MT2 voltage with reference to electrode MT1.

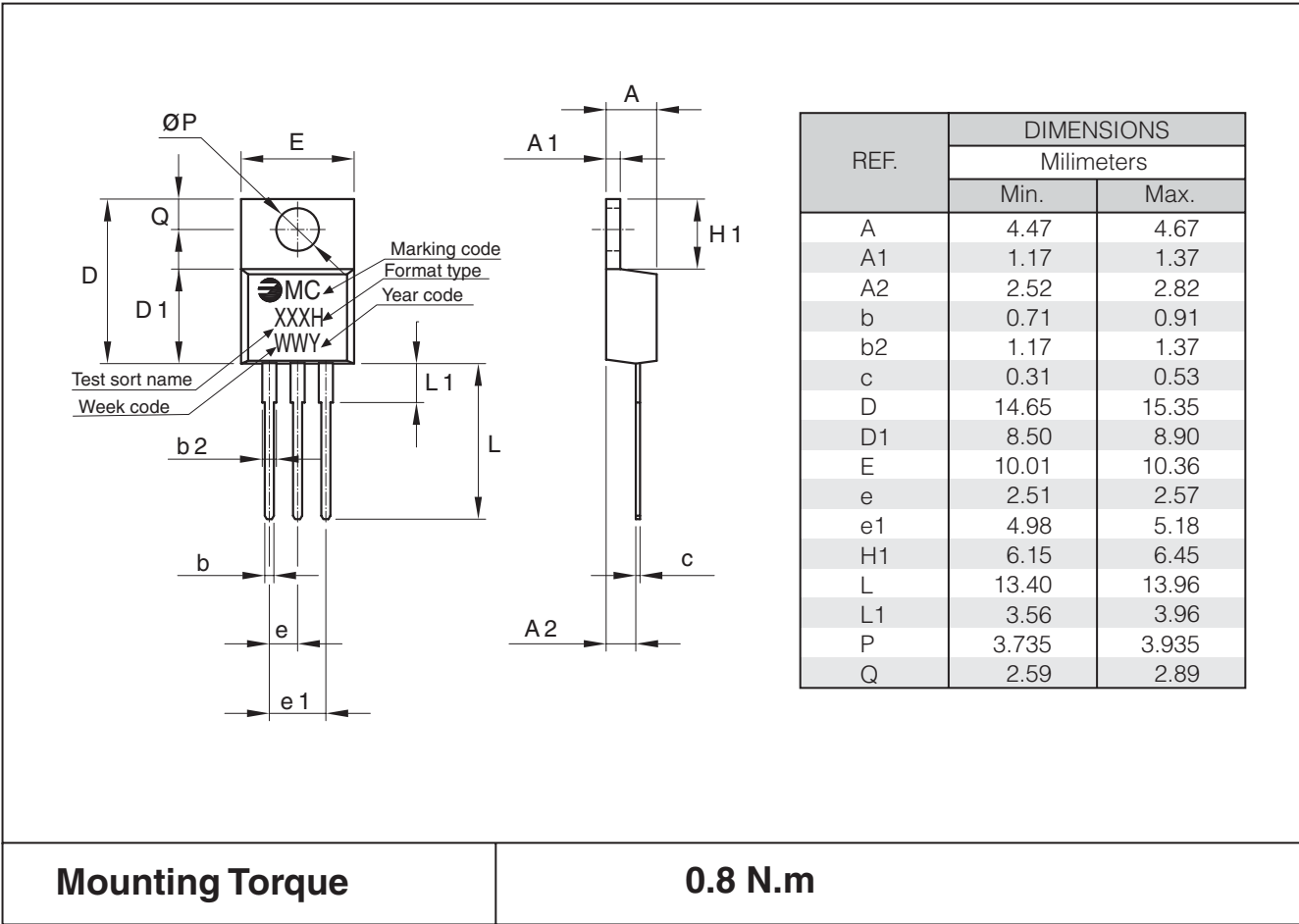
**Part Number Information**


LOGIC LEVEL TRIAC

Ordering information

PREFERRED P/N	PACKAGE CODE	DELIVERY MODE	BASE QUANTITY	UNIT WEIGHT (g)
FT0808MH 00TU	TU	TUBE	1,000	2.30

Package Outline Dimensions: (mm) TO-220AB



## LOGIC LEVEL TRIAC

### Ratings and Characteristics (Ta 25 °C unless otherwise noted)

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle).

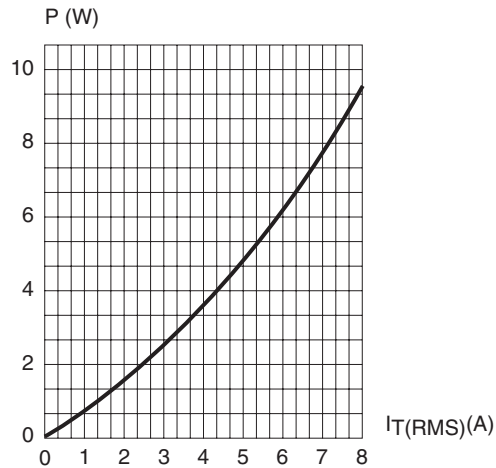


Fig. 2: RMS on-state current versus case temperature (full cycle).

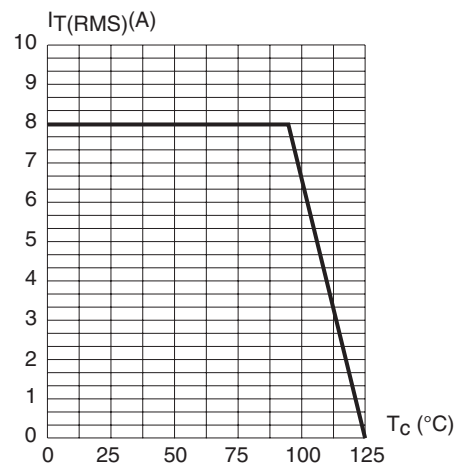


Fig. 3: Relative variation of thermal impedance versus pulse duration.

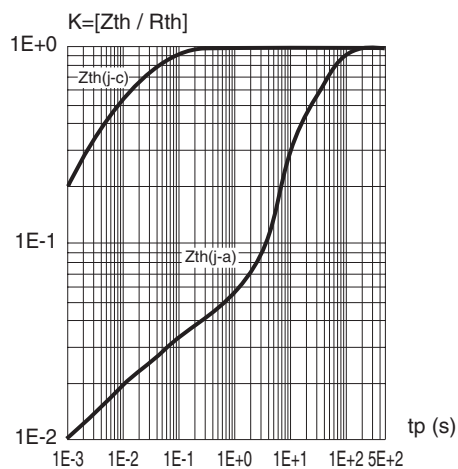


Fig. 4: On-state characteristics (maximum values)

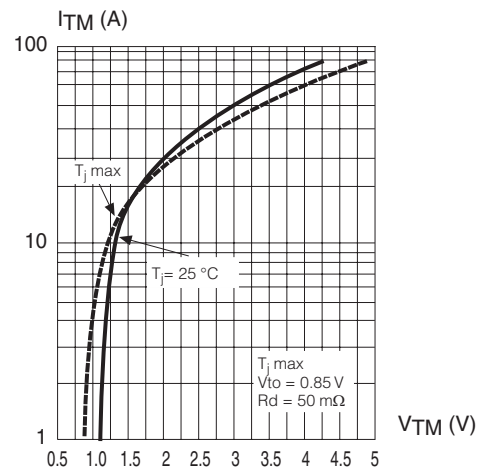


Fig. 5: Surge peak on-state current versus number of cycles

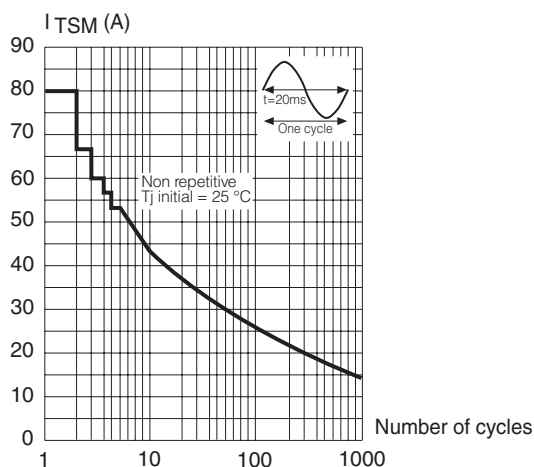
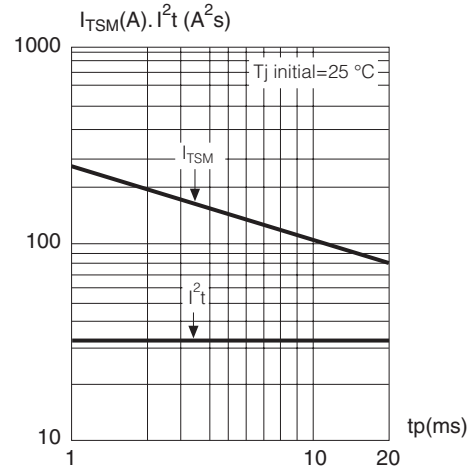


Fig. 6: Non repetitive surge peak on-state current for a sinusoidal pulse with width:  $t_p < 10$  ms, and corresponding value of  $I^2 t$ .



## LOGIC LEVEL TRIAC

### Ratings and Characteristics (Ta 25 °C unless otherwise noted)

Fig. 7: Relative variation of gate trigger current, holding current and latching versus junction temperature (typical values)

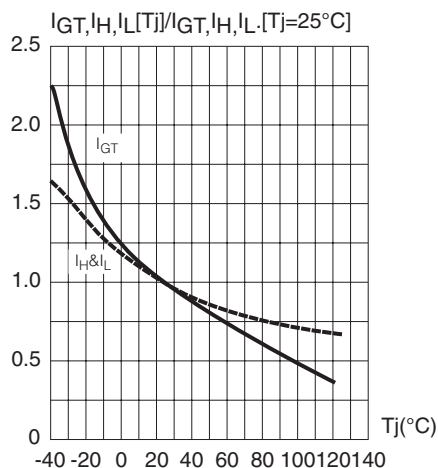


Fig. 8: Relative variation of critical rate of decrease of main current versus junction temperature

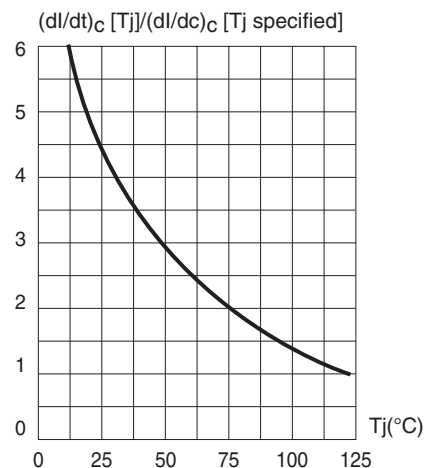
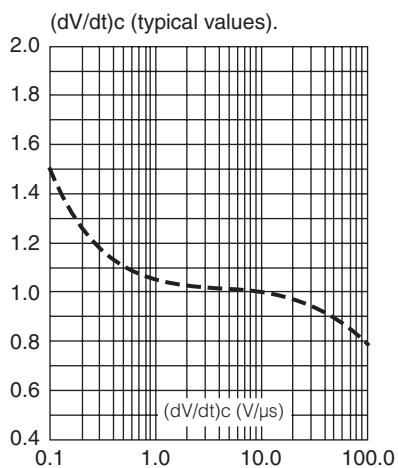


Fig. 9: Relative variation of critical rate of decrease of main current versus



**LOGIC LEVEL TRIAC****Revision History**

Date	Revision	Description of Changes
14-Jun-2011	0	Original Data Sheet
23-Mar-2017	1	200V and 700V eliminated

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