1 Mb High Speed Quad SPI MRAM

FEATURES

- High bandwidth – Read and Write at 52MB/sec
- Quad I/O with the use of dual purpose pins to maintain a low pin count
- Operates in both standard, single SPI mode and high speed quad SPI mode
- Fast quad Read and Write with quad address input and quad I/O
- Intended for next generation RAID controllers, server system logs, storage device buffers, and embedded system data and program memory
- Data is non-volatile with retention greater than 20 years
- Automatic data protection on power loss
- Unlimited write endurance
- Low-current sleep mode
- Dual 3.3v V_{DD} / 1.8v V_{DDQ} power supply
- Tamper Detect function will detect possible data modification from outside magnetic fields.
- Quad Peripheral Interface (QPI) mode is supported to enhance system performance for Execute in Place (XIP) operation.
- MSL Level 3.

RoHS

16-SOIC

24-BGA

DESCRIPTION

The MR10Q010 is the ideal memory solution for applications that must store and retrieve data and programs quickly using a small number of pins, low power, and choice of a 24-ball BGA or a 16-pin SOIC package. The four I/O's in Quad SPI mode allow very fast reads and writes, making it an attractive alternative to conventional parallel data bus interfaces in next generation RAID controllers, server system logs, storage device buffers, and embedded system data and program memory.

Using Everspin's patented MRAM technology, both reads and writes can occur randomly in memory with no delay between writes.

Standard Serial Peripheral Interface (SPI), Quad SPI and Quad Peripheral Interface (QPI) modes are supported at a clock rate up to 104MHz. XIP operation is supported for Read commands in all three modes.

The MR10Q010 Quad SPI MRAM is organized as 131,072 words of 8 bits.

Operational Overview

Mode	Command Set	Utility Commands	XIP Command Operation
SPI Mode	Read 40MHz. Write, Fast Read 104MHz	Write Enable/Disable, Sleep Mode, Read/Write Status Register, Tamper Detect, Read Device ID, Enable QPI Mode	Fast Read
Quad SPI Mode	Quad I/O mode Read/Write data, or both address and data	None.	Fast Read Quad Output, Fast Read Quad Address and Data
QPI Mode	Enables command instruction entry in quad I/O mode. (2 clocks)	Disable QPI Mode.	Fast Read, Fast Read Quad Output, Fast Read Quad Address and Data

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OVERVIEW

The Serial Peripheral Interface, SPI, is becoming increasingly popular in system design due to the reduced pin count of the serial interface and increasing data bandwidth offered when compared against x8 or x16 parallel interface architectures. The SPI interface has evolved from a single data line to a four data line, or quad architecture. This interface provides a data bandwidth in excess of 50Mbytes/sec.

SPI is currently well-established in microcontroller/microprocessor based systems. The Everspin family of single I/O SPI MRAM is popular in smart meter applications and a variety of other embedded systems. However, the 40MHz limitation with a single data I/O may be too slow for higher performance applications such as the next generation RAID controllers, server system logs, and storage device buffers .

Operating at 52MB/second for both Read and Write the Everspin 1Mb Quad I/O SPI MRAM will meet the needs of these applications. And as a non-volatile memory with over 20 years of data retention, this SPI memory family is equally suited for embedded system data and program memory.

The Quad Peripheral Interface, QPI, mode provides a lower overhead to load commands, which will improve system throughput when operating in an Execute in Place, XIP, environment. This added feature will make the device attractive in embedded applications that store program code in an external memory. QPI effectively increases the effective clock rate and, when combined with Quad SPI instructions, Quad SPI memory performance will outstrip asynchronous parallel memories.

Table 1 – Operational Parameters Summary

Density	Interface	Voltage (V)	Read/ Write	Active Current R/W (mA)	Standby Current (mA)	Sleep Current (µA)	Package
1 Mb	104MHz Quad SPI	3.3v V_{DD} 1.8v V_{DDQ}	52MB/sec	60/100	8.0	100	16-SOIC

Operation in 3.3v Data Bus Systems - Evaluation Board Available

The Everspin MR10Q010 Quad SPI Serial MRAM requires a 3.3v V_{DD} power supply and is designed to operate on a 1.8v I/O bus. Adapting the MR10Q010 to operate on a 3.3v data bus can be done by interfacing it to the bus through a level translator.

An evaluation board is available to test this adaptation of the MR10Q010 in an existing system. It can be connected to the bus at the board position currently occupied by a SPI or Quad SPI E^2PROM and operate with the MR10Q010 I/O levels translated for operation on a 3.3v bus.

Contact Everspin for more information about the MR10Q010 3.3v evaluation board and adapting your 3.3v bus system to operate with MR10Q010 MRAM.

Figure 1 – MR10Q010 Block Diagram

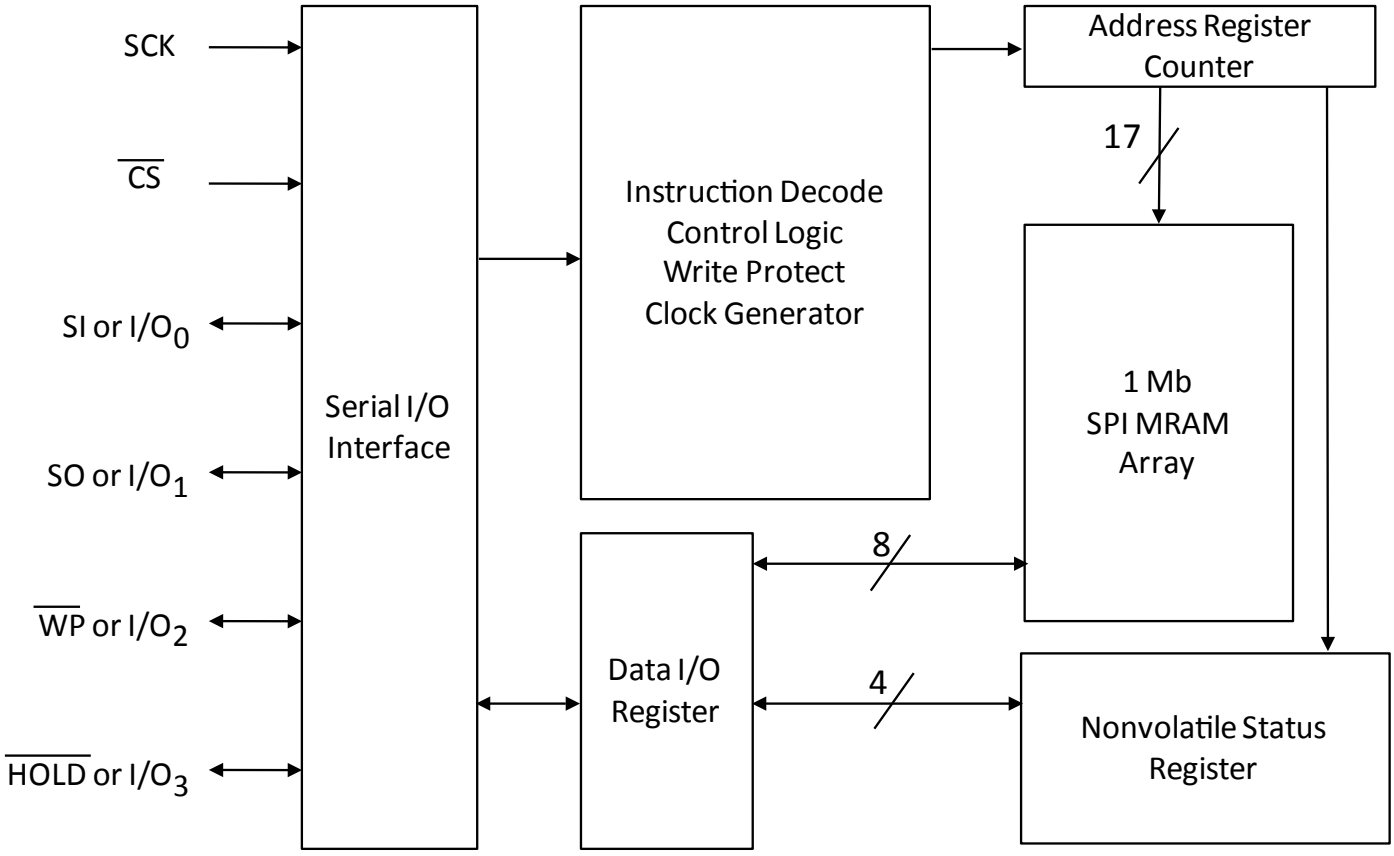


Figure 2 – System Configuration

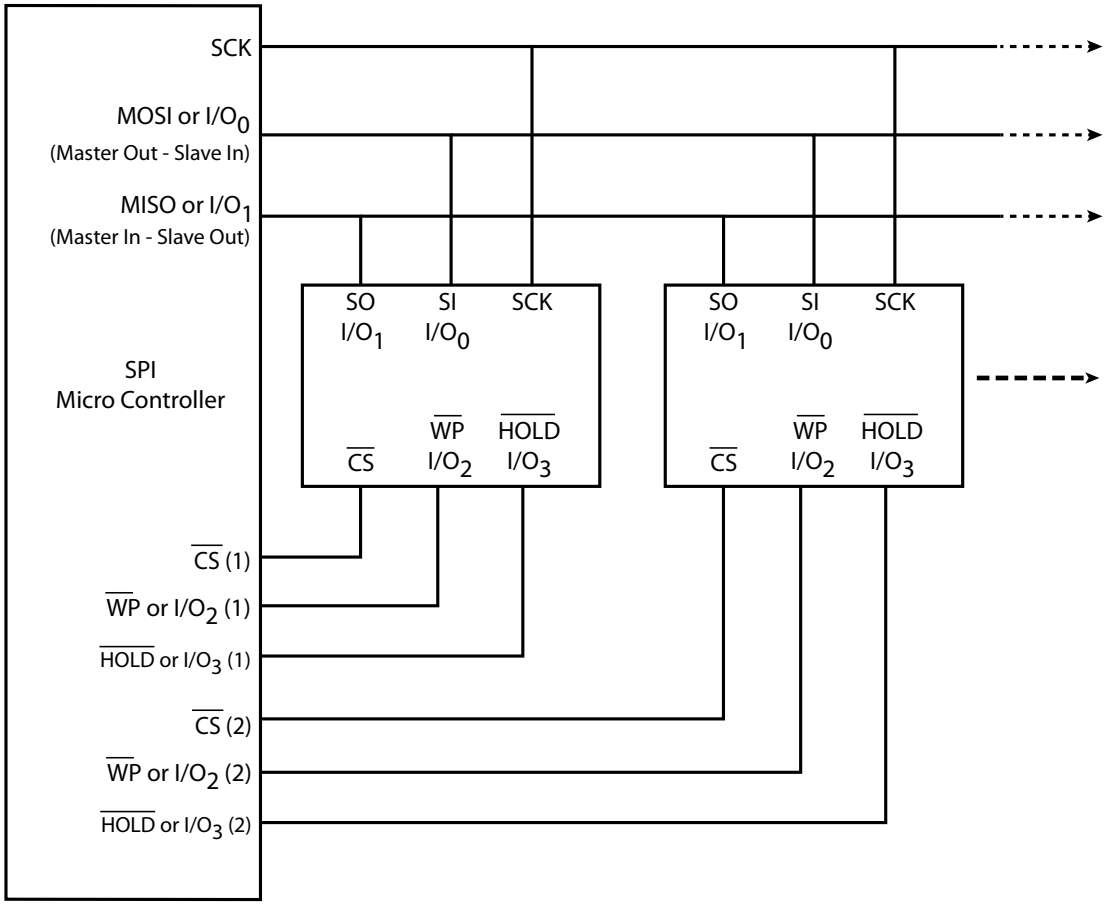


Figure 3 – 16-SOIC Package Pin Assignments

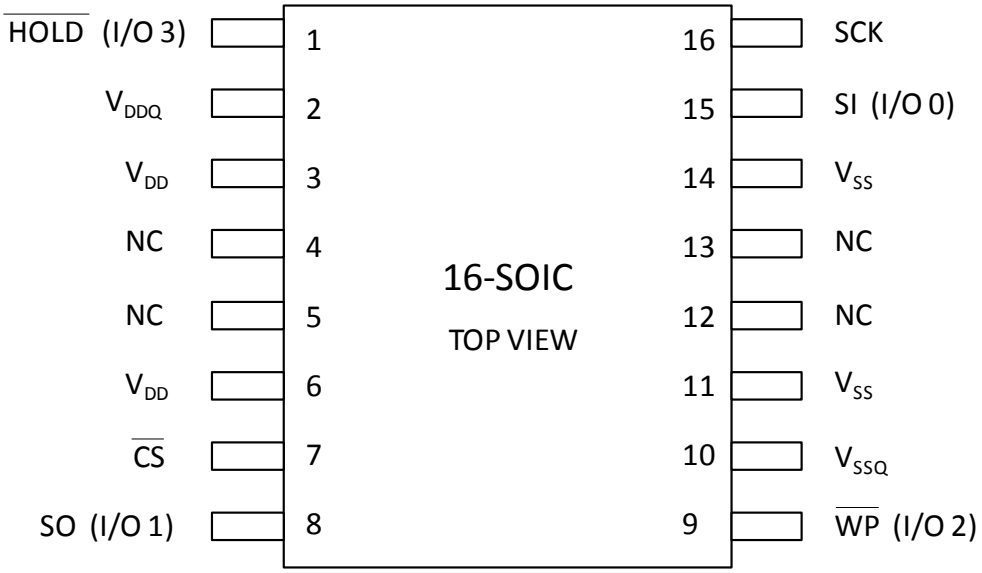


Table 2 – 16-SOIC Pin Functions

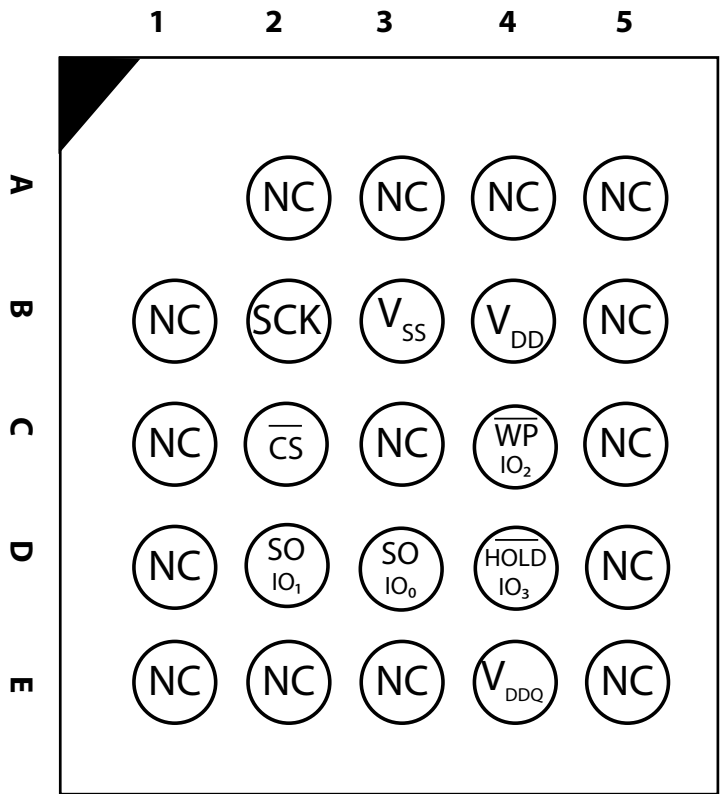
Signal Name	Pin	SPI Mode	Quad SPI Mode [1]	Description
$\overline{CS}$	7	Chip Select	Chip Select	An active low chip select for the serial MRAM. When chip select is high, the memory is powered down to minimize standby power, inputs are ignored and the serial output pin is Hi-Z. Multiple serial memories can share a common set of data pins by using a unique chip select for each memory.
SO (I/O_1)	8	Serial Output	I/O_1	SPI Mode: The data output pin is driven during a read operation and remains Hi-Z at all other times. SO is Hi-Z when $\overline{HOLD}$ is low. Data transitions on the data output occur on the falling edge of SCK. Quad SPI Mode: Bidirectional I/O to serially write instructions, addresses or data to the device on the rising edge of SCK or read data output from the device on the falling edge of SCK.

Table continues on next page.

16-SOIC Pin Functions - Continued

Signal Name	Pin	SPI Mode	Quad SPI Mode [1]	Description
$\overline{WP}$ (I/O_2)	9	Write Protect	I/O_2	SPI Mode: A low on the write protect input prevents write operations to the Status Register. Quad SPI Mode: Bidirectional I/O to serially write instructions, addresses or data to the device on the rising edge of SCK or read data output from the device on the falling edge of SCK.
V_{SS}	11, 14	Ground	Ground	Power supply ground pin.
V_{SSQ}	10	Ground	Ground	I/O Voltage ground pin.
SI (I/O_0)	15	Serial Input	I/O_0	SPI Mode: All data is input to the device through this pin. This pin is sampled on the rising edge of SCK and ignored at other times. SI can be tied to SO to create a single bidirectional data bus if desired. Quad SPI Mode: Bidirectional I/O to serially write instructions, addresses or data to the device on the rising edge of SCK or read data output from the device on the falling edge of SCK.
SCK	16	Clock	Clock	Synchronizes the operation of the MRAM. The clock can operate up to 104 MHz to shift commands, address, and data into the memory. Inputs are captured on the rising edge of clock. Data outputs from the MRAM occur on the falling edge of clock. The serial MRAM supports both SPI Mode 0 (CPOL=0, CPHA=0) and Mode 3 (CPOL=1, CPHA=1). In Mode 0, the clock is normally low. In Mode 3, the clock is normally high. Memory operation is static so the clock can be stopped at any time.
$\overline{HOLD}$ (I/O_3)	1	$\overline{HOLD}$	I/O_3	SPI Mode: A low on the $\overline{HOLD}$ pin interrupts a memory operation for another task. When $\overline{HOLD}$ is low, the current operation is suspended. The device will ignore transitions on the $\overline{CS}$ and SCK when $\overline{HOLD}$ is low. All transitions of $\overline{HOLD}$ must occur while $\overline{CS}$ is low. Quad SPI Mode: Bidirectional I/O to serially write instructions, addresses or data to the device on the rising edge of SCK or read data output from the device on the falling edge of SCK.
V_{DD}	3, 6	Power Supply	Power Supply	Power supply voltage from +3.0 to +3.6 volts.
V_{DDQ}	2	I/O Bus Power Supply	I/O Bus Power Supply	I/O Bus supply voltage from +1.7 volts to +1.9 volts.

Figure 4 – 24-BGA Package Ball Assignments



- 24-ball BGA package.
- 8mm x 6mm package outline.
- Serial NOR Flash pinout compatible.
- V_{DDQ} on ball E4 to support 1.8v I/O.
- No V_{SSQ} ball.

Table 3 – 24-BGA Ball Functions

Signal Name	Ball	SPI Mode	Quad SPI Mode [1]	Description
$\overline{CS}$	C2	Chip Select	Chip Select	An active low chip select for the serial MRAM. When chip select is high, the memory is powered down to minimize standby power, inputs are ignored and the serial output pin is Hi-Z. Multiple serial memories can share a common set of data pins by using a unique chip select for each memory.
SO (I/O_1)	D2	Serial Output	I/O_1	SPI Mode: The data output pin is driven during a read operation and remains Hi-Z at all other times. SO is Hi-Z when $\overline{HOLD}$ is low. Data transitions on the data output occur on the falling edge of SCK. Quad SPI Mode: Bidirectional I/O to serially write instructions, addresses or data to the device on the rising edge of SCK or read data output from the device on the falling edge of SCK.

Table continues on next page.

24-BGA Ball Functions - Continued

Signal Name	Ball	SPI Mode	Quad SPI Mode [1]	Description
$\overline{WP}$ (I/O_2)	C4	Write Protect	I/O_2	SPI Mode: A low on the write protect input prevents write operations to the Status Register. Quad SPI Mode: Bidirectional I/O to serially write instructions, addresses or data to the device on the rising edge of SCK or read data output from the device on the falling edge of SCK.
V_{SS}	B3	Ground	Ground	Power supply ground pin.
SI (I/O_0)	D3	Serial Input	I/O_0	SPI Mode: All data is input to the device through this pin. This pin is sampled on the rising edge of SCK and ignored at other times. SI can be tied to SO to create a single bidirectional data bus if desired. Quad SPI Mode: Bidirectional I/O to serially write instructions, addresses or data to the device on the rising edge of SCK or read data output from the device on the falling edge of SCK.
SCK	B2	Clock	Clock	Synchronizes the operation of the MRAM. The clock can operate up to 104 MHz to shift commands, address, and data into the memory. Inputs are captured on the rising edge of clock. Data outputs from the MRAM occur on the falling edge of clock. The serial MRAM supports both SPI Mode 0 (CPOL=0, CPHA=0) and Mode 3 (CPOL=1, CPHA=1). In Mode 0, the clock is normally low. In Mode 3, the clock is normally high. Memory operation is static so the clock can be stopped at any time.
$\overline{HOLD}$ (I/O_3)	D4	$\overline{HOLD}$	I/O_3	SPI Mode: A low on the $\overline{HOLD}$ pin interrupts a memory operation for another task. When $\overline{HOLD}$ is low, the current operation is suspended. The device will ignore transitions on the $\overline{CS}$ and SCK when $\overline{HOLD}$ is low. All transitions of $\overline{HOLD}$ must occur while $\overline{CS}$ is low. Quad SPI Mode: Bidirectional I/O to serially write instructions, addresses or data to the device on the rising edge of SCK or read data output from the device on the falling edge of SCK.
V_{DD}	B4	Power Supply	Power Supply	Power supply voltage from +3.0 to +3.6 volts.
V_{DDQ}	E4	I/O Bus Power Supply	I/O Bus Power Supply	I/O Bus supply voltage from +1.7 volts to +1.9 volts.

STATUS REGISTER

The status register consists of the 8 bits shown in Table 3 below.

The Status Register Write Disable bit (SRWD, Bit 7) is used in conjunction with the Write Enable Latch (WEL, bit 1) and the Write Protection pin ($\overline{WP}$) to provide hardware memory block protection. Their usage for memory block protection is defined in "Table 5 – Memory Protection Modes". The Status Register Write Disable bit is non-volatile and will remain set whenever power is removed from the memory. The WEL bit (Bit 7) is volatile and set by the Write Enable command. It is set to "0" at power up and reset to "0" when recovering from a loss of power.

The status of memory block protection is indicated by the states of bits BP0 and BP1 (Bits 2 and 3) and are also defined in "Table 5 – Memory Protection Modes" on page 15. BP0 and BP1 are non-volatile and remain set if power is removed from the memory.

The QPI Mode bit (Bit 6) indicates whether the memory is in QPI mode or not. Its value is set when the Enable QPI (EQPI) or Disable QPI (DQPI) commands are invoked. Logic "1" indicates QPI mode is enabled. The QPI Mode Bit is volatile and set to "0" at power up and reset to "0" when recovering from a loss of power.

The fast writing speed of the MR10Q010 does not require write status bit information (Normally Bit 0). The state of reserved bits 4, 5, and 0 can be modified by the user but do not affect memory operation.

All bits in the status register are pre-set at the factory to the "0" state.

Non-reserved Status Register bits are non-volatile with the exception of the WEL and QPI Mode which are reset to 0 upon power cycling.

Table 4 – Status Register Bit Definitions

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRWD (Non volatile)	QPI Mode (Volatile)	R2	R1	BP1 (Non-Volatile)	BP0 (Non-Volatile)	WEL (Volatile)	R0

Bit Definitions:

7 - SRWD - Status Register Write Disable

6 - QPI Mode bit. Logic 1 = The device is in QPI Mode. Set by the Enable QPI (page 40) and Disable QPI Commands (page 41). Cannot be modified by the Write Status Register Command (page 21). Reset to "0" upon any power cycling.

5 - R2 - Reserved bit 2

4 - R1 - Reserved bit 1

3 - BP1 - Block Protect bit 1

2 - BP0 - Block Protect bit 0

1 - WEL - Write Enable Latch bit. Set by the Write Enable (page 19) Command. Reset to "0" upon any power cycling.

0 - R0 - Reserved bit 0. This is the "Write in Progress" bit for many memory devices. For MR10Q010, the "Write in progress" bit (bit 0) is not written by the memory because there is no write delay with MRAM.

Memory Protection Modes

When WEL is reset to 0, writes to all blocks and the status register are protected. When WEL is set to 1, BP0 and BP1 determine which memory blocks are protected. While SRWD is reset to 0 and WEL is set to 1, status register bits BP0 and BP1 can be modified. Once SRWD is set to 1, $\overline{WP}$ must be high to modify SRWD, BP0 and BP1.

Table 5 – Memory Protection Modes

WEL	SRWD	$\overline{WP}$	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Writable	Writable
1	1	Low	Protected	Writable	Protected
1	1	High	Protected	Writable	Writable

Block Protection Modes

The memory enters hardware block protection when the $\overline{WP}$ input is low and the Status Register Write Disable (SRWD) Bit is set to 1. The memory leaves hardware block protection only when the $\overline{WP}$ pin goes high. While $\overline{WP}$ is low, the write protection blocks for the memory are determined by the status register bits BP0 and BP1 and cannot be modified without taking the $\overline{WP}$ signal high again.

If the $\overline{WP}$ signal is high (independent of the status of SRWD Bit), the memory is in software protection mode. This means that block write protection is controlled solely by the status register BP0 and BP1 block write protect bits and this information can be modified using the WRSR command.

Table 6 – Block Memory Write Protection

Status Register		Memory Contents	
BP1	BP0	Protected Area	Unprotected Area
0	0	None	All Memory
0	1	Upper Quarter	Lower Three-Quarters
1	0	Upper Half	Lower Half
1	1	All	None

SPI COMMUNICATIONS PROTOCOL

The MR10Q010 can be operated in either SPI Mode 0 (CPOL=0, CPHA =0) or SPI Mode 3 (CPOL=1, CPHA=1). For both modes, inputs are captured on the rising edge of the clock and data outputs occur on the falling edge of the clock. When not conveying data, SCK remains low for Mode 0; while in Mode 3, SCK is high. The memory determines the mode of operation (Mode 0 or Mode 3) based upon the state of the SCK when $\overline{CS}$ falls.

All memory transactions start when $\overline{CS}$ is brought low to the memory. The first byte is a command code. Depending upon the command, subsequent bytes of address are input. Data is either input or output. There is only one command performed per $\overline{CS}$ active period. $\overline{CS}$ must go inactive before another command can be accepted. To ensure proper part operation according to specifications, it is necessary to terminate each access by raising $\overline{CS}$ at the end of a byte (a multiple of 8 clock cycles from $\overline{CS}$ dropping to avoid partial or aborted accesses.

SPI MODE COMMANDS

All memory transactions start when $\overline{CS}$ is brought low, selecting the memory. The first byte is an 8-bit command code in hexadecimal. The subsequent 24 bits entered are address input. Following the address input (except for the FREAD command) the device will read/write data beginning at the address entered.

For the FREAD command the Mode Byte must be entered following the address. The Mode Byte will either set or reset the XIP mode. See "Execute in Place (XIP) Mode" on page 42.

There is only one command performed per $\overline{CS}$ active period. $\overline{CS}$ must go inactive before another command can be accepted. Note: To avoid partial or aborted accesses, memory access must remain active ($\overline{CS}$ low) for a multiple of 8 clocks from $\overline{CS}$ going low (the end of a byte.)

At power up, the default operational mode is SPI mode.

Table 7 – SPI Mode Commands Overview

SPI Mode Commands Overview

Name	Operation	Code	Description
RDSR	Read Status Register	05h	Returns the contents of the 8 Status Register bits.
WREN	Write Enable	06h	Sets the Write Enable Latch (WEL) bit in the status register to 1.
WRDI	Write Disable	04h	Sets the Write Enable Latch (WEL) bit in the status register to 0.
WRSR	Write Status Register	01h	Writes new values to the entire Status Register.
READ	Read Data Bytes	03h	Continuously reads data bytes starting at an initial address specified.
FREAD [1]	Fast Read Data Bytes	0Bh	High-speed READ with XIP operation option.
WRITE	Write Data Bytes	02h	Continuously writes data bytes starting at an address specified.
SLEEP	Enter Sleep Mode	B9h	Initiates Sleep Mode.
WAKE	Exit Sleep Mode	ABh	Terminates Sleep Mode.
TDET	Tamper Detect	17h	Returns 4 data bytes indicating corrupted or uncorrupted memory.
RDID	Read ID	4Bh	Returns the Everspin device ID assigned by JEDEC.

Notes:

1. FREAD has the option of using XIP operational mode. See "Execute in Place (XIP) Mode" on page 42 for details of XIP mode with the FREAD command.

Read Status Register (RDSR)

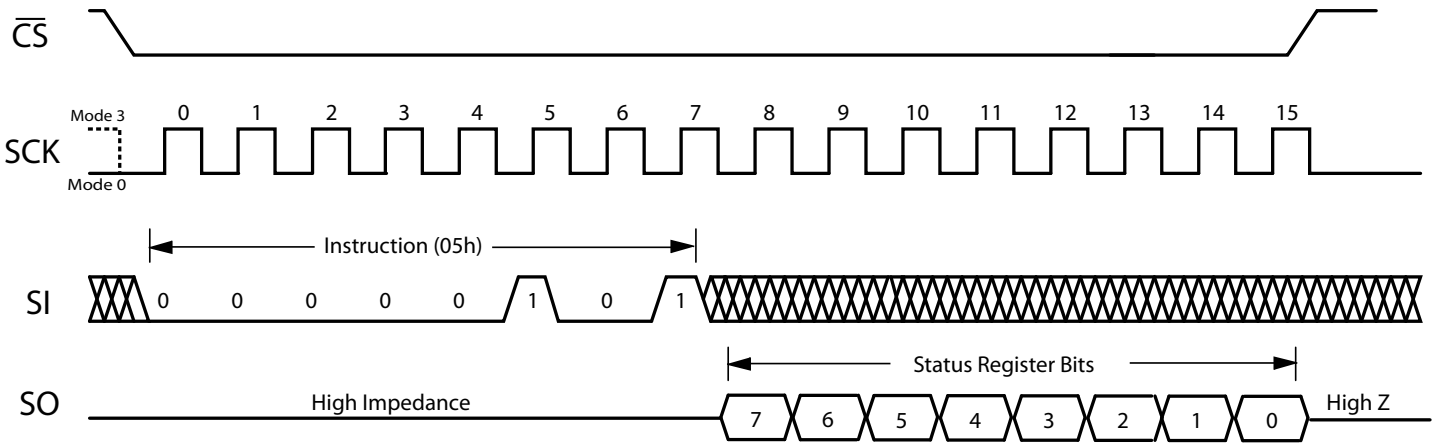
The Status Register can be read at any time to check the status of the Write Enable Latch Bit, status register Write Protect Bit, QPI mode, and the block write protect bits. The RDSR command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high.

See "Table 3 – Status Register Bit Definitions" on page 11 for Status Register Bit definitions.

Figure 5 – Read Status Register (RDSR) Command Operation

		Clock Number [2]					
Name	**Operation**	0 - 7 [1]	8 - 15	16 - 23	24 - 31	32 - 39	40 - *n*
RDSR	Read Status Register	05h	S7-S0 [3]	-	-	-	-

Notes:
1. Clocks 0 - 7 are the command byte.
2. See "AC Timing Parameters" on page 61 for timing requirements.
3. See "Table 3 – Status Register Bit Definitions" on page 11 for status register bit definitions.



Write Enable (WREN)

The Write Enable (WREN) command sets the Write Enable Latch Bit (WEL) in the status register (Bit 1). The Write Enable Latch must be set prior to writing in the status register or the memory. The WREN command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high.

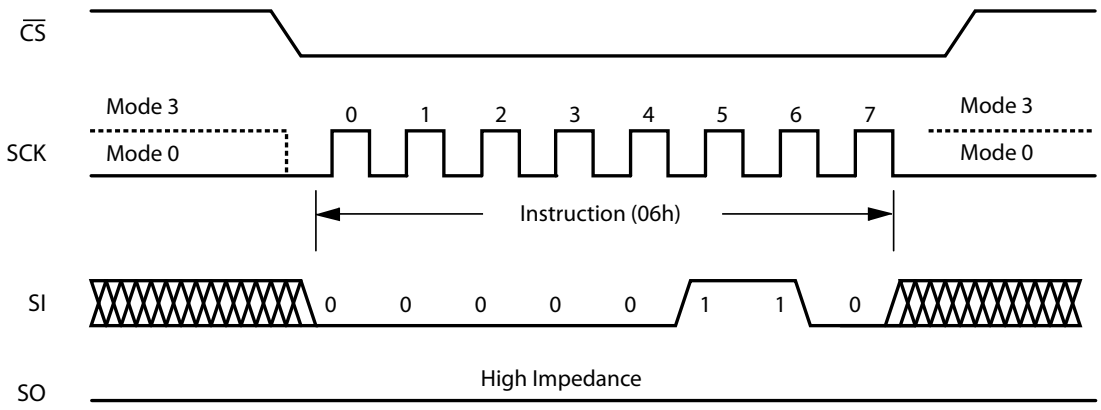
See "Table 3 – Status Register Bit Definitions" on page 11 for Status Register Bit definitions.

Figure 6 – Write Enable (WREN) Command Operation

		Clock Number [1]					
Name	**Operation**	0 - 7 [2]	8 - 15	16 - 23	24 - 31	32 - 39	40 - *n*
WREN	Write Enable	06h	-	-	-	-	-

Notes:

1. See "AC Timing Parameters" on page 61 for timing requirements.
2. Clocks 0 - 7 are the command byte.



Write Disable (WRDI)

The Write Disable (WRDI) command resets the Write Enable Latch (WEL) bit in the status register (bit 1) to 0. This prevents writes to status register or memory. The WRDI command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high.

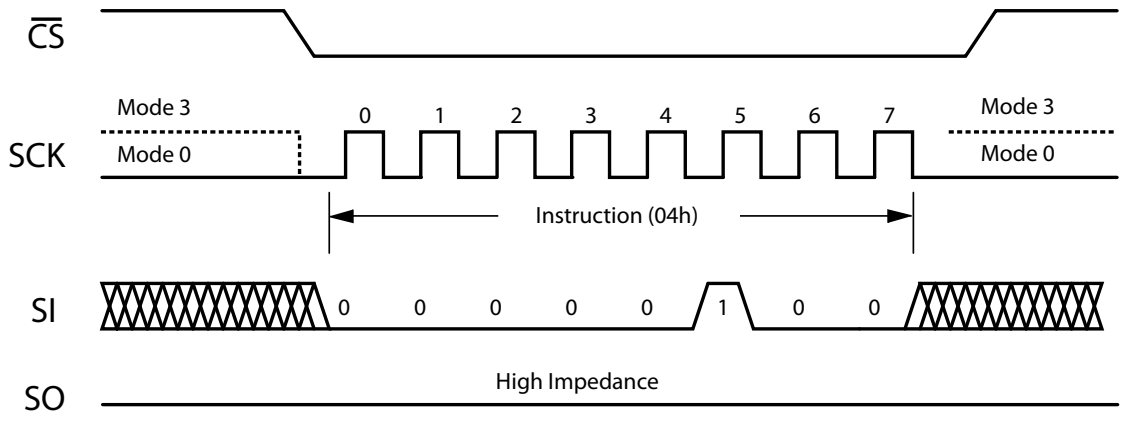
The Write Enable Latch (WEL) is reset to 0 on power-up or when the WRDI command is completed.

See "Table 3 – Status Register Bit Definitions" on page 11 for Status Register bit definitions.

Figure 7 – Write Disable (WRDI) Command Operation

		Clock Number [1]					
Name	**Operation**	0 - 7 [2]	8 - 15	16 - 23	24 - 31	32 - 39	40 - *n*
WRDI	Write Disable	04h	-	-	-	-	-

Notes:
1. See "AC Timing Parameters" on page 61 for timing requirements.
2. Clocks 0 - 7 are the command byte.



Write Status Register (WRSR)

The Write Status Register (WRSR) command allows new values for certain bits to be written to the Status Register. The WRSR command cannot be executed unless the Write Enable Latch (WEL) has been set to 1 by executing a WREN command while pin $\overline{WP}$ the SRWD Bit correspond to values that make the status register writable as seen in Table 5 on page 15.

QPI Mode Bit, Bit 6, and the WEL Bit, Bit 0, are set by other commands and cannot be changed by this command.

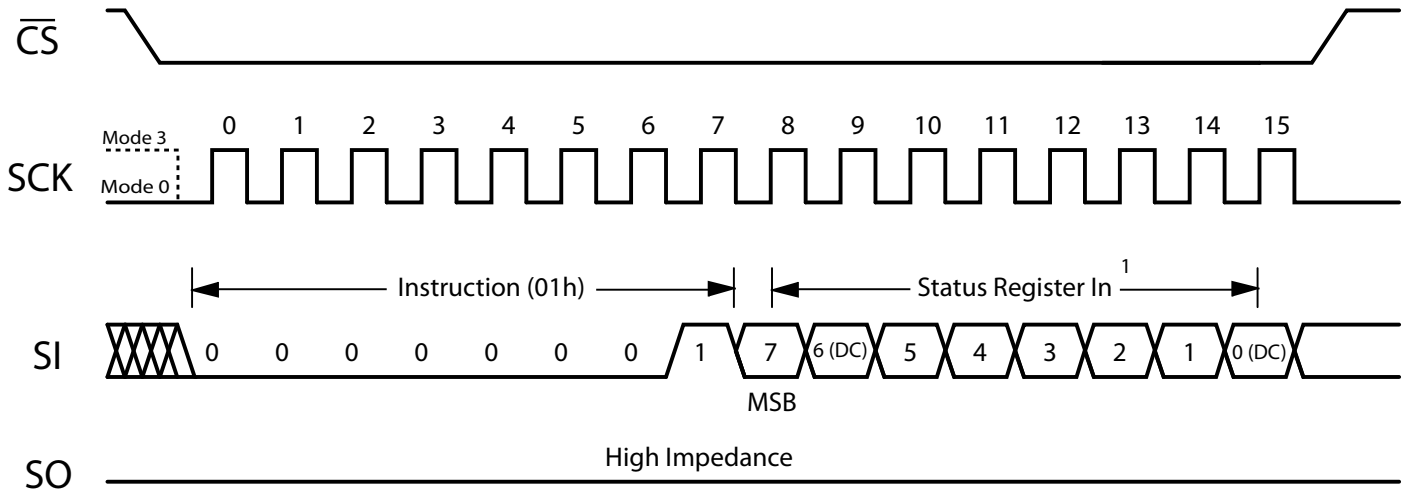
The WRSR command is entered by driving $\overline{CS}$ low, sending the command code and status register write data byte, and then driving $\overline{CS}$ high.

Figure 8 – Write Status Register (WRSR) Command Operation

		Clock Number					
Name	**Operation**	0 - 7 [1]	8 - 15 [2]	16 - 23	24 - 31	32 - 39	40 - *n*
WRSR	Write Status Register	01h	S7-S0	-	-	-	-

Notes:

1. Clocks 0 - 7 are the command byte.
2. Neither the QPI Mode Bit, Bit 6, or the WEL Bit, bit 0, can be changed by this command.



Notes:

1. Neither the QPI Mode Bit, Bit 6, or the WEL Bit, bit 0, can be changed by this command. Treat as Don't Care.

Read Data Bytes (READ)

The Read Data Bytes (READ) command allows data bytes to be continuously read starting at an initial address specified by the 24-bit address entry. The data bytes are read out sequentially from memory until the read operation is terminated by bringing $\overline{CS}$ high. The entire memory can be read in a single command. The address counter will roll over to 0000H when the address reaches the top of memory.

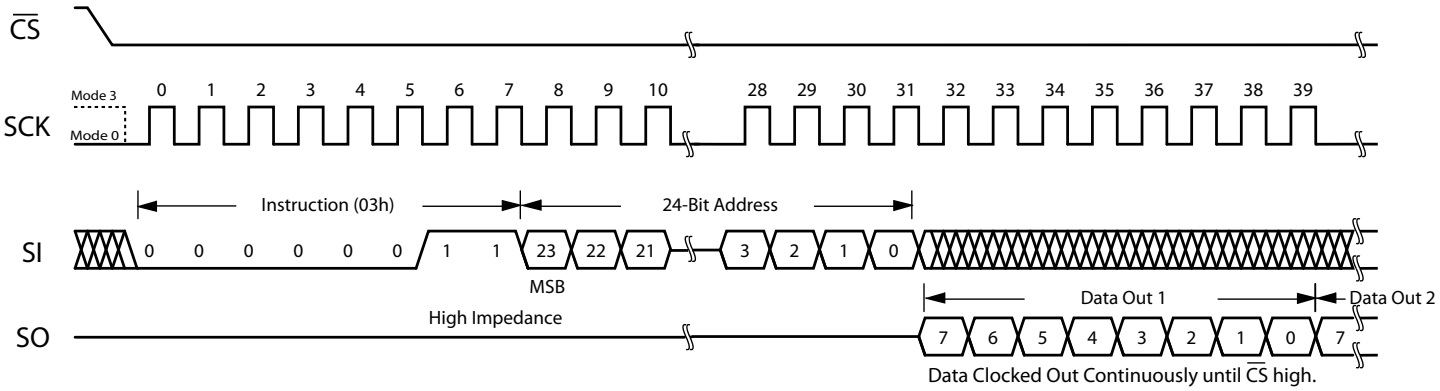
The READ command is entered by driving $\overline{CS}$ low and sending the command code. The memory drives the read data bytes on the SO pin. Reads continue as long as the memory is clocked. (Maximum READ clock frequency 40MHz.) The command is terminated by bringing $\overline{CS}$ high.

Figure 9 – Read Data Bytes (READ) Command Operation

		Clock Number					
Name	**Operation**	0 - 7 [1]	8 - 15	16 - 23	24 - 31	32 - 39	40 - *n*
READ	Read Data Bytes	03h	A23-A16	A15-A8	A7-A0	D7-D0, until $\overline{CS}$ high	

Notes:

1. Clocks 0 - 7 are the command byte.
2. For timing details, see "Figure 35 – Synchronous Data Timing (READ)" on page 63.



Fast Read Data Bytes (FREAD)

The Fast Read Data Bytes FREAD command is similar to the READ command except that the device can be operated at the highest frequency (f_{SCK} = 104MHz) and the command has an XIP operation option. For more detail on the XIP option, see "Table 13 – XIP Mode with FREAD Command" on page 43.

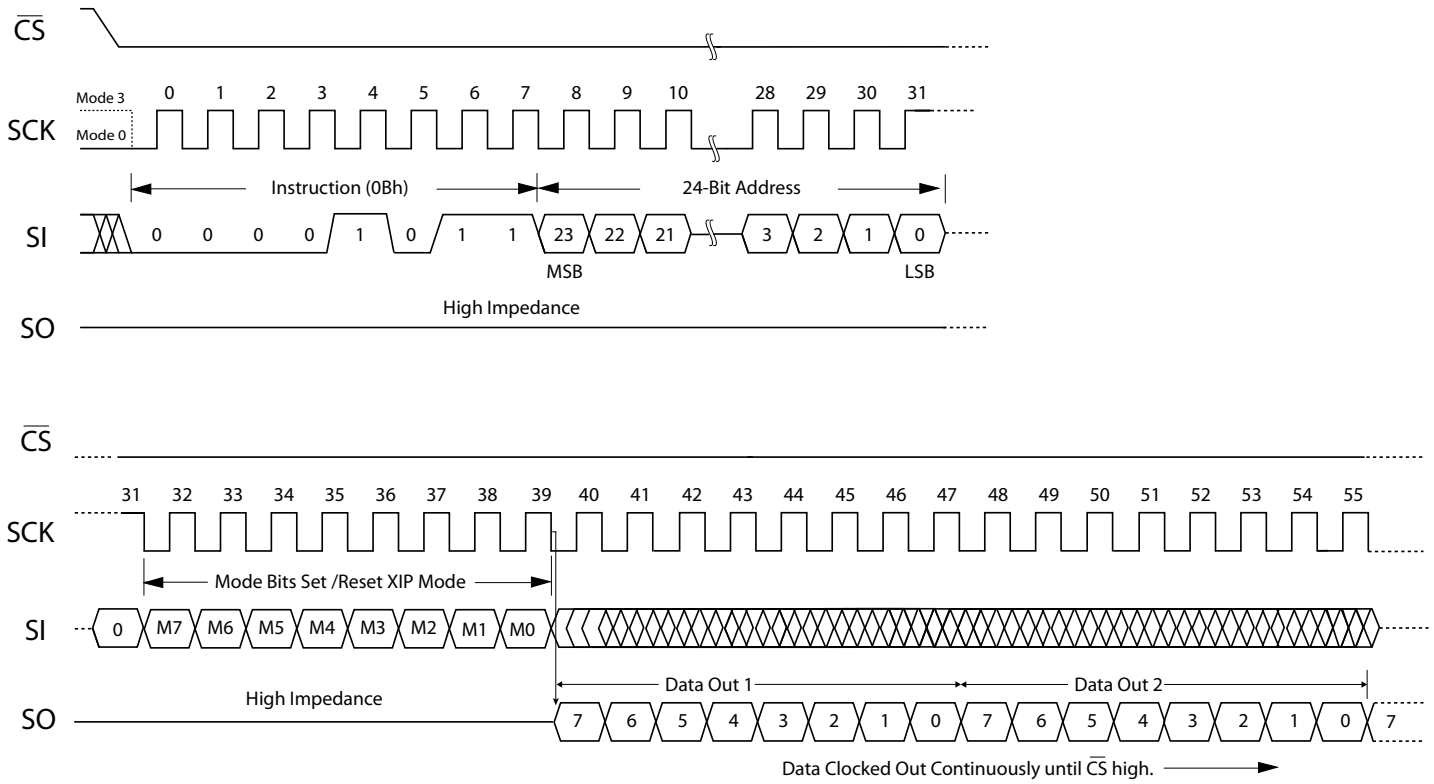
The FREAD command is entered by driving $\overline{CS}$ low and sending the command code. The memory drives the read data bytes on the SO pin. Reads continue as long as the memory is clocked. The command is terminated by bringing $\overline{CS}$ high.

Figure 10 – Fast Read Data Bytes (FREAD) Command Operation

		Clock Number					
Name	**Operation**	0 - 7 [1]	8 - 15	16 - 23	24 - 31	32 - 39	40 - *n*
FREAD	Fast Read Data Bytes	0Bh	A23-A16	A15-A8	A7-A0	Mode bits [2] (7-0)	D7-D0, until $\overline{CS}$ high

Notes:

1. Clocks 0 - 7 are the command byte.
2. Mode Byte to Set/Reset XIP operation. Set/Continue XIP Mode = EFh. Reset XIP Mode FFh (exit XIP). See "Execute in Place (XIP) Mode" on page 42 for more detailed information on XIP operation with FREAD.
3. For timing details, see "Figure 36 – Synchronous Data Timing Fast Read (FREAD)" on page 63.



Write Data Bytes (WRITE)

The Write Data Bytes (WRITE) command allows data bytes to be written starting at an address specified by the 24-bit address. The data bytes are written sequentially in memory until the write operation is terminated by bringing $\overline{CS}$ high. The entire memory can be written in a single command. The address counter will roll over to 0000h when the address reaches the top of memory.

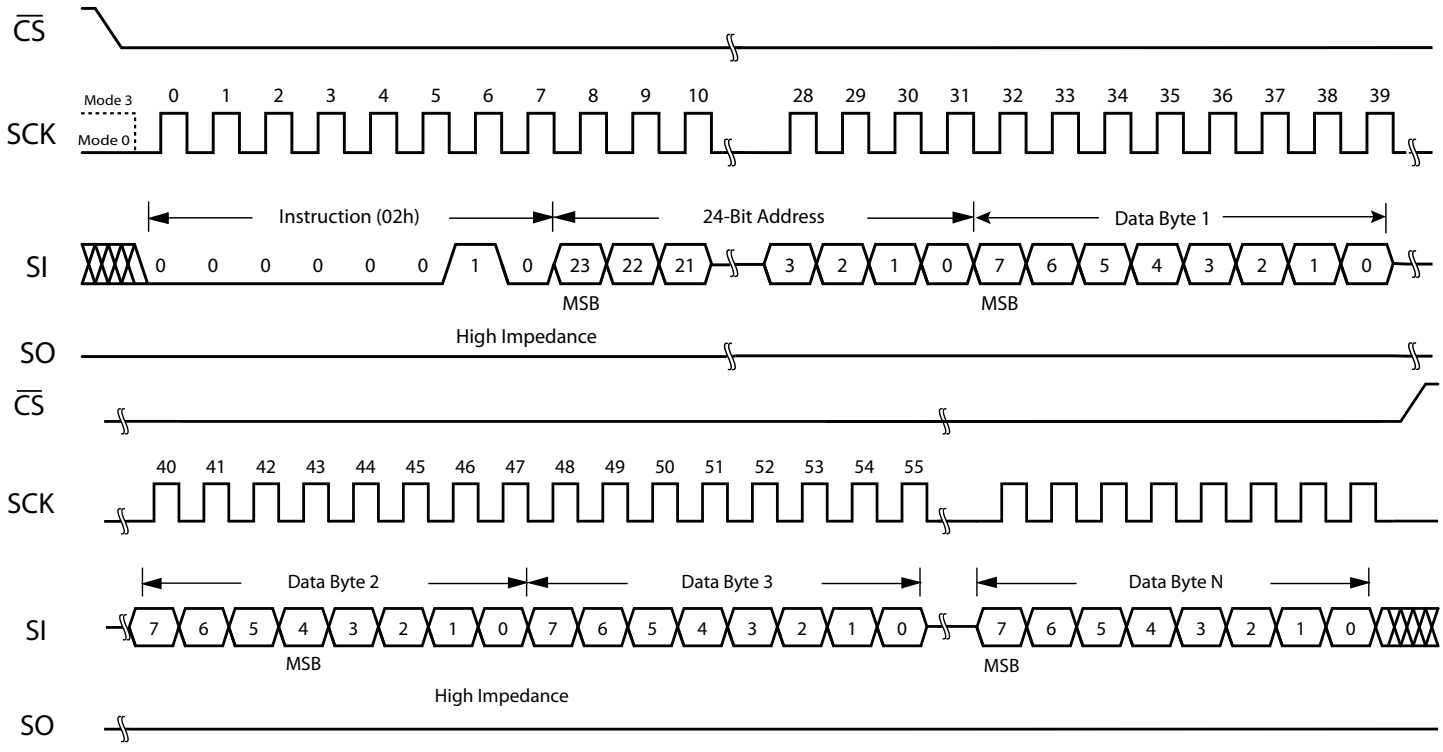
MRAM is a random access memory rather than a page, sector, or block organized memory so it is ideal for both program and data storage. Unlike EEPROM or Flash Memory, MRAM can write data bytes continuously at its maximum rated clock speed without write delays or data polling. Back to back WRITE commands to any random location in memory can be executed without write delay.

The WRITE command is entered by driving $\overline{CS}$ low, sending the command code, and then sequential write data bytes. Writes continue as long as the memory is clocked. The command is terminated by bringing $\overline{CS}$ high.

Figure 11 – Write Data Bytes (WRITE) Command Operation

		Clock Number					
Name	**Operation**	0 - 7 [1]	8 - 15	16 - 23	24 - 31	32 - 39	40 - *n*
WRITE	Write Data Bytes	02h	A23-A16	A15-A8	A7-A0	D7-D0, until $\overline{CS}$ high	

Notes:
1. Clocks 0 - 7 are the command byte.
2. For timing details see "Figure 37 – Synchronous Data Timing (WRITE)" on page 64.



Enter Sleep Mode (SLEEP)

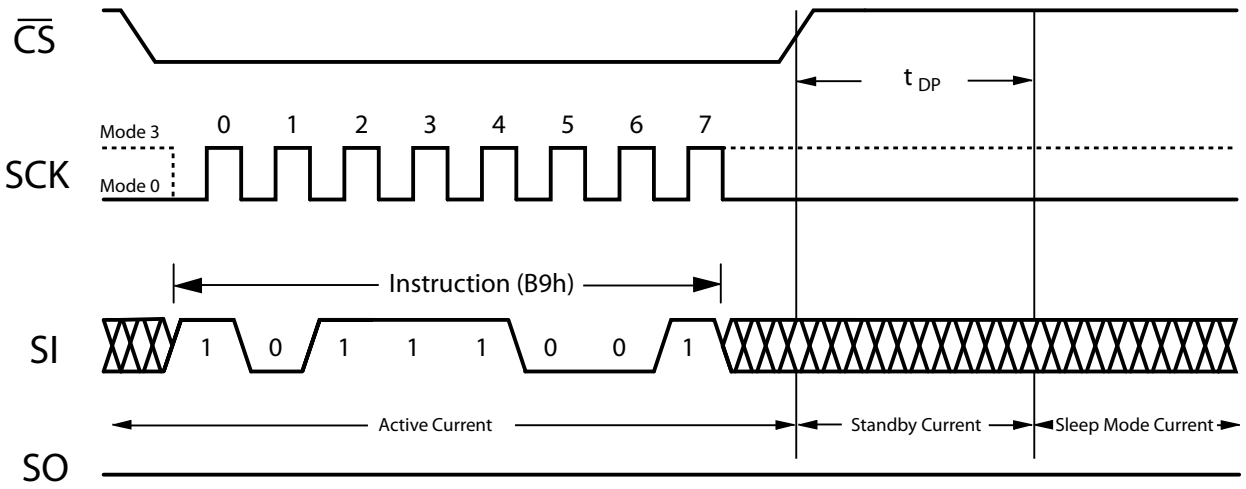
The Enter Sleep Mode (SLEEP) command turns off all MRAM power regulators in order to reduce the overall chip standby power to 15 µA typical. The SLEEP command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high. The standby current is achieved after time, ^{t}DP. See "Table 23 – AC Timing Parameters" on page 61 for the ^{t}DP value.

If power is removed when the part is in sleep mode, upon power restoration, the part enters normal standby. The only valid command following SLEEP mode entry is a WAKE command.

Figure 12 – Enter Sleep Mode (SLEEP) Command Operation

		Clock Number					
Name	**Operation**	0 - 7 [1]	8 - 15	16 - 23	24 - 31	32 - 39	40 - *n*
SLEEP	Enter Sleep Mode	B9h	-	-	-	-	-

Notes:
1. Clocks 0 - 7 are the command byte.



Exit Sleep Mode (WAKE)

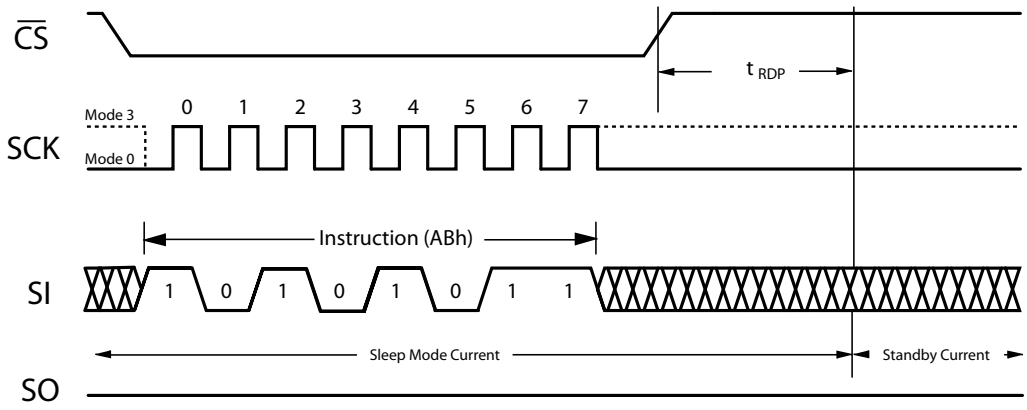
The Exit Sleep Mode (WAKE) command turns on internal MRAM power regulators to allow normal operation. The WAKE command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high. The memory returns to standby mode after ^{t}RDP. See "Table 23 – AC Timing Parameters" on page 61 for the ^{t}RPD value.

The $\overline{CS}$ pin must remain high until the ^{t}RDP period is over. WAKE must be executed after sleep mode entry and prior to any other command when the device is in Sleep mode.

Figure 13 – Exit Sleep Mode (WAKE) Command Operation

		Clock Number					
Name	**Operation**	0 - 7 [1]	8 - 15	16 - 23	24 - 31	32 - 39	40 - *n*
WAKE	Exit Sleep Mode	ABh	-	-	-	-	-

Notes:
1. Clocks 0 - 7 are the command byte.



Tamper Detect (TDET)

The Tamper Detect command is used to check whether the memory contents have been corrupted by exposure to external magnetic fields. The command is invoked by entering the command code followed by the 8-bit Mode Byte. The device reads dedicated pre-programmed memory bits located around the memory physical array. The contents of these bits are compared to reference bits that are hard programmed into the device via a metal mask. The result of the comparison is returned in 32 status bits of data on SO beginning after the last Mode Byte clock.

All 0's in the 32 TDET status bits indicates that the tamper check bits are correct against the reference bits and the memory has not been corrupted. Presence of any 1's in the 32-bit string indicates that at least one of the check bits does not match its reference bit and the memory contents have likely been corrupted.

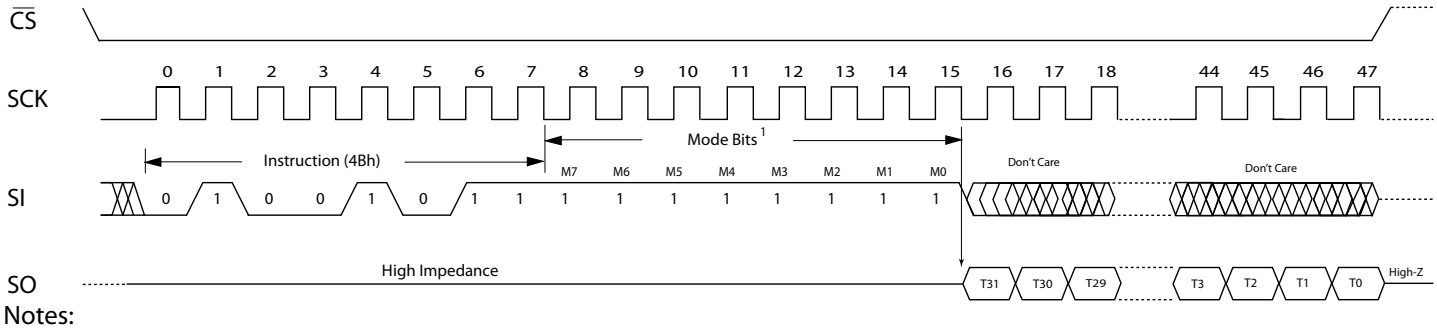
Following $\overline{CS}$ high, any new command can be entered on the next access, except another TDET command. If it is necessary to immediately enter another TDET command, a Tamper Detect Exit (TDETX) command must be issued first to reset the device for another Tamper Detect sequence.

Figure 14 – Tamper Detect (TDET) Command Operation

		Clock Number			
Name	**Operation**	0 - 7 [1]	8 - 15	16 - 47	48 - *n*
TDET	Tamper Detect	17h	Mode Byte bits 7 - 0 [3]	T31 - T0 [2]	$\overline{CS}$ high

Notes:

1. Clocks 0 - 7 are the command byte.
2. 32 Tamper Detect indication bits. Any 1's present in the 32-bit string indicate probable corruption of the memory contents.
3. In the TDET command operation, the Mode Byte is used as a time delay to read the check and reference bits. The Mode Byte must be set to FFh.



Notes:

1. In the TDET command operation, the Mode Byte must be set to FFh.

Tamper Detect Exit (TDETX)

After running a TDET command, any other command can be run as the next command, except another TDET command. If another TDET command is to be run, then the Tamper Detect Exit (TDETX) command must be run first to reset the device. This is necessary *only* if immediately running another TDET command. See "Tamper Detect (TDET)" on page 27.

Figure 15 – Tamper Detect Exit (TDETX) Command Operation

		Clock Number	
Name	**Operation**	0 - 7 [1]	8 - *n* [2]
TDETX	Tamper Detect Exit	07h	$\overline{CS}$ high. Any command can be entered on next access.

Notes:
1. Clocks 0 - 7 are the command byte.
2. After $\overline{CS}$ goes high any other command can be given on the next access.

Read ID (RDID)

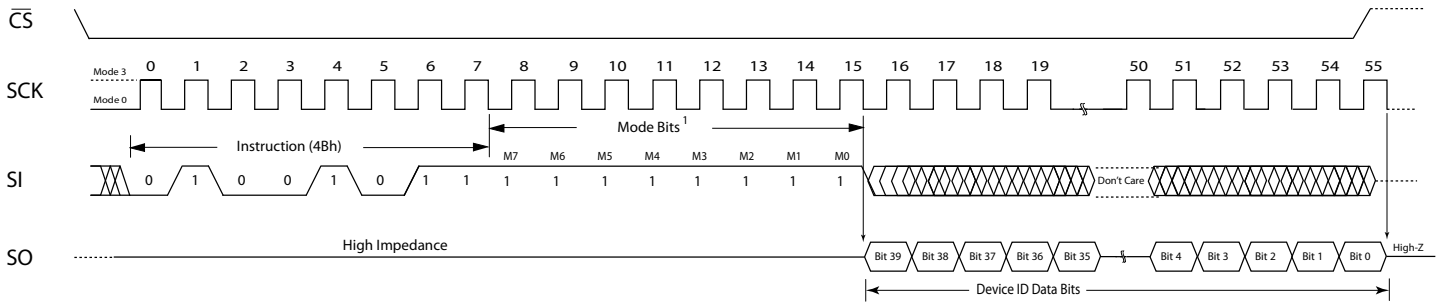
The Read Device ID command (RDID) returns 40 bits of information that identify the Everspin device. The command is invoked with $\overline{CS}$ low, and sending command code 4Bh on the Serial Input (SI) pin. See "Figure 16 – Read ID (RDID) Command Operation" below. After 8 clocks for the Mode Byte, 40 bits of data uniquely identifying the Everspin device are returned on the Serial Out (SO) pin. See "Table 8 – Device ID for MR10Q010". If $\overline{CS}$ remains low after reading the 40 ID bits, additional clocks with $\overline{CS}$ low will return zeros on SO until $\overline{CS}$ goes high.

Figure 16 – Read ID (RDID) Command Operation

		Clock Number					
Name	**Operation**	0 - 7 [1]	8 - 15	16 - 23	24 - 31	32 - 39	40 - *n*
RDID	Read ID	4Bh	Mode Byte [2] Bits 7 - 0	Device ID [3] Clocks 16 - 55			

Notes:

1. Clocks 0 - 7 are the command byte.
2. In the RDID command operation, the Mode Byte is used as a time delay to read the device ID bits. The Mode Byte must be set to FFh.
3. For the Everspin device ID codes, see "Table 8 – Device ID for MR10Q010" on page 30.



Notes:

1. In the RDID command operation, the Mode Byte must be set to FFh.

Table 8 – Device ID for MR10Q010

RDID Device ID for MR10Q010							
Bit #	**39 - 24**	**23 - 20**	**19 - 16**	**15 - 12**	**11 - 8**	**7 - 4**	**3 - 0**
Meaning	**Manufacturer's ID (JEP 106AH)**	**Technology**	**Interface**	**Speed**	**Density**	**Voltage**	**Die Rev**
MR10Q010	6Bh, eighth bank	Toggle MRAM	Quad IO SPI	104MHz	1 Mb	3.3v V_{DD} / 1.8v V_{DDQ}	A
Binary	0000_0111_0110_1011	0001	0001	0001	0001	0001	0001

Complete Hexadecimal and Binary Device ID for MR10Q010	
Hexadecimal	076B111111
Binary	0000_0111_0110_1011_0001_0001_0001_0001_0001_0001

QUAD SPI MODE COMMANDS

Quad SPI commands allow data to be transferred to or from the device at least four times the rate of conventional SPI mode. When using Quad SPI commands the DI and DO pins become bidirectional IO_0 and IO_1, and the $\overline{WP}$ and $\overline{HOLD}$ pins become IO_2 and IO_3 respectively. Address and data information can be input to the device on four IO's and data output can be read from four IO's, offering a significant improvement in continuous and random access transfers. XIP mode operation is available for FRQO and FRQAD commands.

Quad SPI Mode Commands Overview

Table 9 – Quad SPI Mode Commands Overview

Name	Operation	Code	Description
FRQO [1]	Fast Read Quad Output	6Bh	Initial address entry on IO_0, returns data continuously in Quad SPI Mode on all four I/O. Has XIP operation option.
FWQD	Fast Write Quad Data	32h	Initial address entry on IO_0, writes data continuously in Quad SPI Mode on all four I/O.
FRQAD [1]	Fast Read Quad Address and Data	EBh	Initial address entry on all four IO's, returns data continuously in quad mode on all four I/O's. Has XIP operation option.
FWQAD	Fast Write Quad Address and Data	12h	Initial address entry on all four IO's, writes data continuously in quad mode on all four I/O's.

Notes:
1. XIP mode option. See "Execute in Place (XIP) Mode" on page 42 for details of how to use FRQD and FRQAD in XIP mode.

Fast Read Quad Output (FRQO)

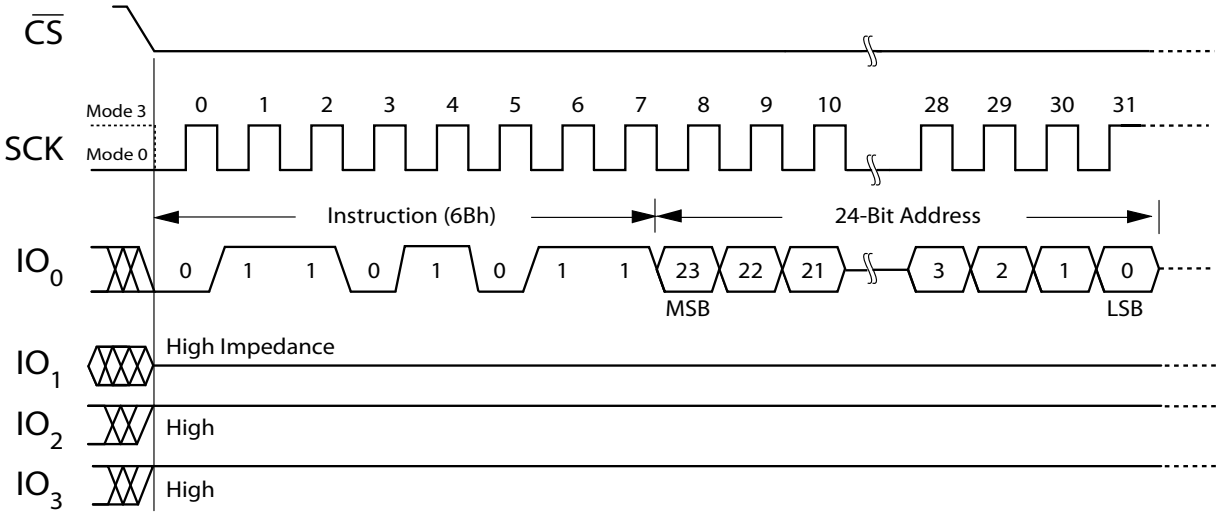
The Fast Read Quad Output (6Bh) command is similar to the Fast Read Output except that a data byte is output on the four I/O pins, requiring only two clocks. An XIP mode is available for this command. See "Table 14 – XIP Operation with FRQO Command" on page 47 for more information about XIP mode operation. The I/O pins should be high impedance prior to the falling edge of the first Mode clock. The FRQO command is entered by driving $\overline{CS}$ low and sending the command code. The memory drives the read data bytes on the IO pins. Reads continue as long as the memory is clocked. The command is terminated by bringing $\overline{CS}$ high.

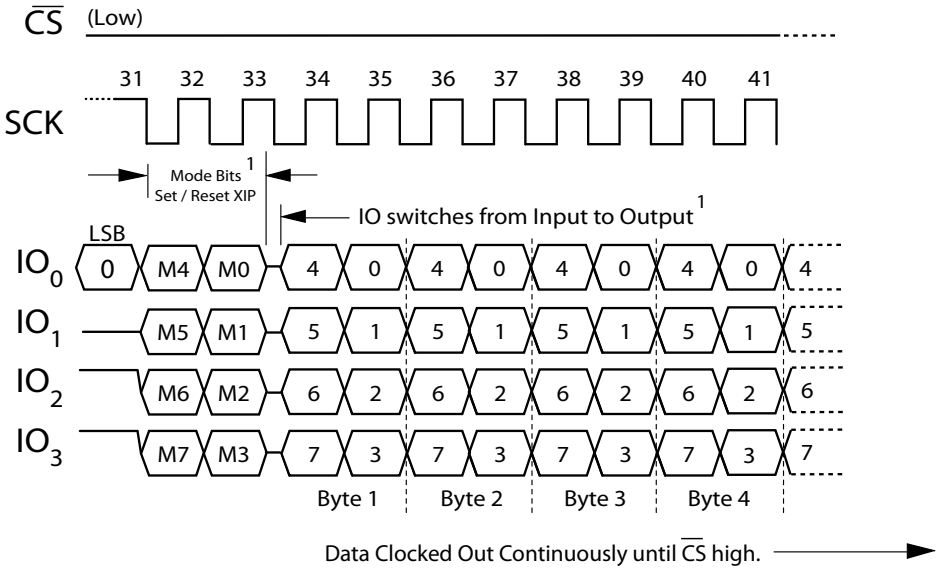
Commmand Operation and Timing next page.

Figure 17 – Fast Read Quad Output (FRQO) Command Operation

		Clock Number						
Name	**Title**	0 - 7 [1]	8 - 15	16 - 23	24 - 31	32 - 33	34 - 35	36 - *n*
FRQO	Fast Read Quad Output	6Bh	A23-A16	A15 - A8	A7- A0	M7- M0 [2]	D7 - D0, until $\overline{CS}$ high [3]	

Notes:
1. Clocks 0 - 7 are the command byte. All commands and address bits on I/O_0.
2. Mode Byte. See "Execute in Place (XIP) Mode" on page 42 for more information on XIP operation with FRQO.
3. Quad Mode data output. I/O_0 switches from Input to Output. I/O_{1-3} active outputs until $\overline{CS}$ returns high. ^tCSH must be observed for valid output when bringing $\overline{CS}$ high.





Note:
1. The I/O pins should be high impedance prior to the falling edge of the second mode clock.

Fast Read Quad Address and Data (FRQAD)

The Fast Read Quad Address and Data (FRQAD) command is similar to the FRQO command except that the address bits are loaded into the four I/O's, requiring six clocks instead of 24. The data bytes also are read from the four I/O's as shown in Figure 18 below. An XIP operating mode is available for this command. See "Table 15 – XIP Operation with FRQAD Command" on page 51 for more information on the XIP operating mode for this command. The FRQAD command is entered by driving $\overline{CS}$ low and sending the command code. The memory drives the read data bytes on the IO pins. Reads continue as long as the memory is clocked. The command is terminated by bringing $\overline{CS}$ high.

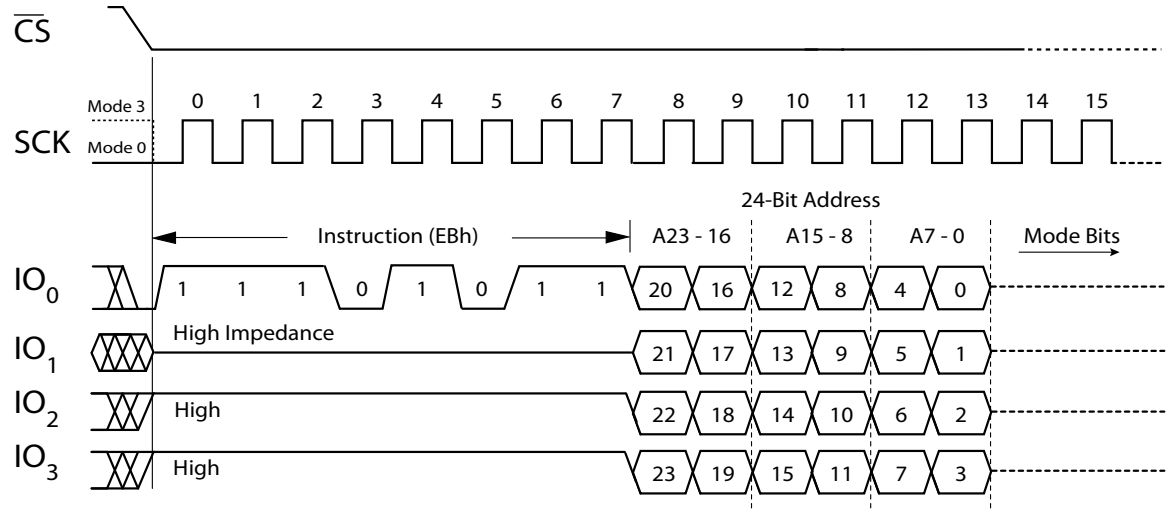
Commmand Operation and Timing next page.

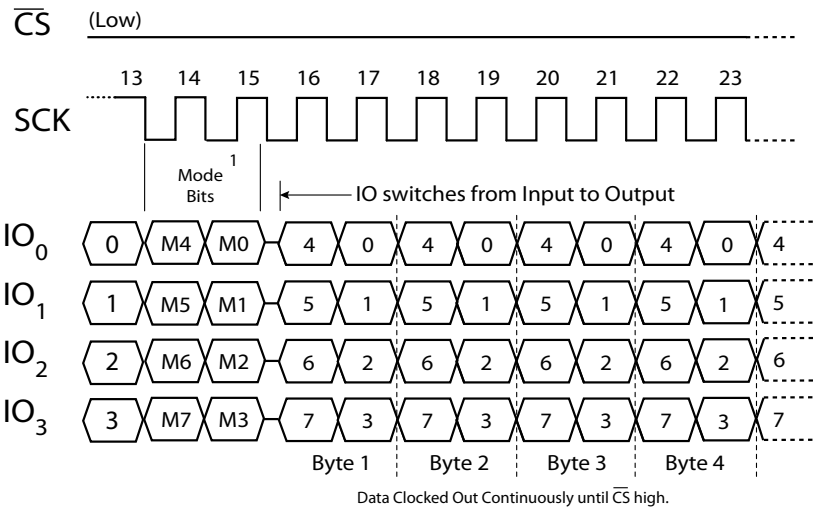
Figure 18 – Fast Read Quad Address and Data (FRQAD) Command Operation

		Clock Number				
Name	**Description**	0 - 7 [1]	8 - 13 [4]	14- 15 [2]	16 - 17	18 - *n*
FRQAD	Fast Read Quad Address and Data	EBh	A23 - A0	M7 - M0 [2]	D7 - D0 every two clocks until $\overline{CS}$ high [3]	

Notes:

1. Clocks 0 - 7 are the command byte. All commands and address bits on I/O_0.
2. Mode Byte. See "Execute in Place (XIP) Mode" on page 42 for more information on XIP operation with FRQAD.
3. Quad Mode data output. I/O_0 switches from Input to Output. I/O_{1-3} active outputs until $\overline{CS}$ returns high. ^tCSH must be observed for valid output when bringing $\overline{CS}$ high.
4. For timing details, see "Figure 38 – Synchronous Data Timing Fast Write Quad Data and Fast Write Quad Address and Data (FWQD and FWQAD)" on page 64.





Note:

1. The I/O pins should be high impedance prior to the falling edge of the second mode clock.

Fast Write Quad Data (FWQD)

The Fast Write Quad Data FWQD command provides a high speed write capability to the memory using four I/O's for data input. The FWQD command can operate at the highest frequency, $^{f}SCK = 104MHz$.

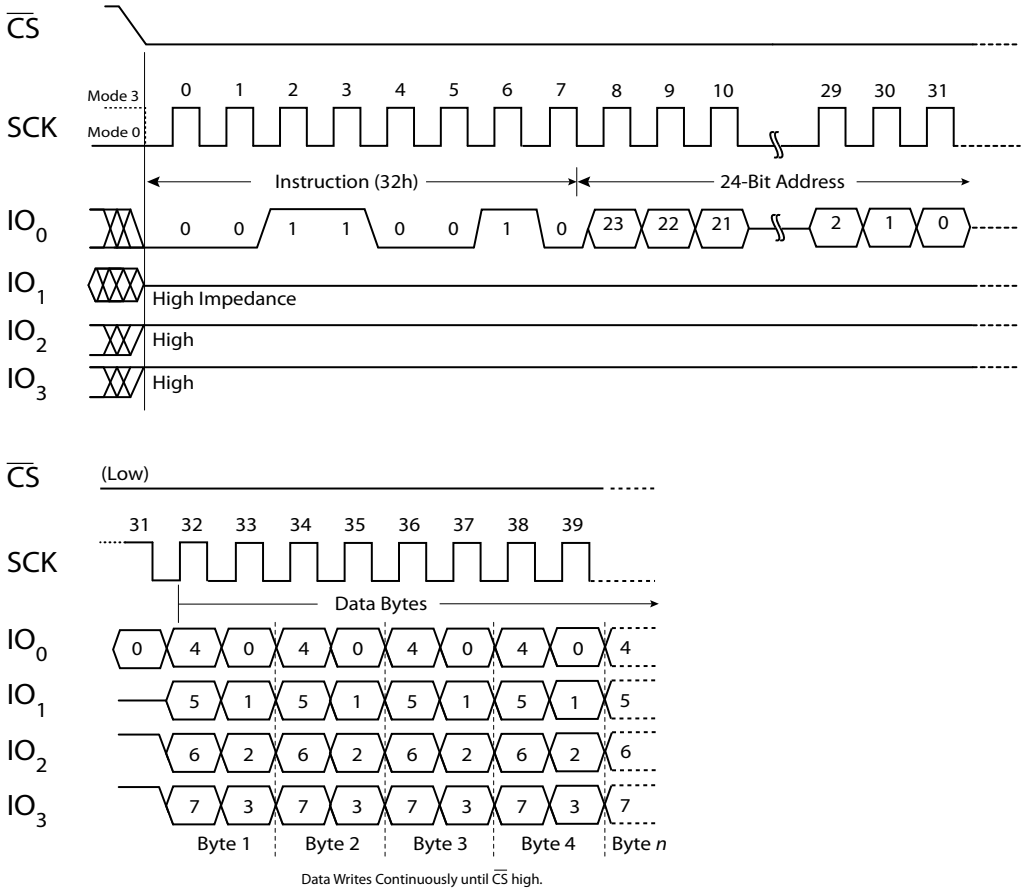
The FWQD command is entered by driving $\overline{CS}$ low and sending the command code (32h). Data is input on all four I/O's and Writes continue as long as the memory is clocked. The command is terminated by bringing $\overline{CS}$ high.

Figure 19 – Fast Write Quad Data (FWQD) Command Operation

		Clock Number						
Name	**Title**	0 - 7 [1]	8 - 15	16 - 23	24 - 31	32 - 33	34 - 35	36 - *n*
FWQD	Fast Write Quad Data	32h	A23-A16	A15 - A8	A7- A0	D7 - D0 every two clocks until $\overline{CS}$ high [2]		

Notes:

1. Clocks 0 - 7 are the command byte. All commands and address bits on I/O_0.
2. Quad Mode address input. I/O_0 remains input. I/O_{1-3} active inputs until $\overline{CS}$ returns high.
3. For timing details, see "Figure 38 – Synchronous Data Timing Fast Write Quad Data and Fast Write Quad Address and Data (FWQD and FWQAD)" on page 64.



Fast Write Quad Address and Data (FWQAD)

The Fast Write Quad Address and Data Command (FWQAD) provides a very fast write at both the highest frequency and fewest clock cycles. The 24-bit address is input on all four I/O's, reducing the number of clock cycles. The data bytes to be written are also input on all four I/O's following the address bits. The FWQAD command can operate at the highest frequency, $^{f}SCK = 104MHz$.

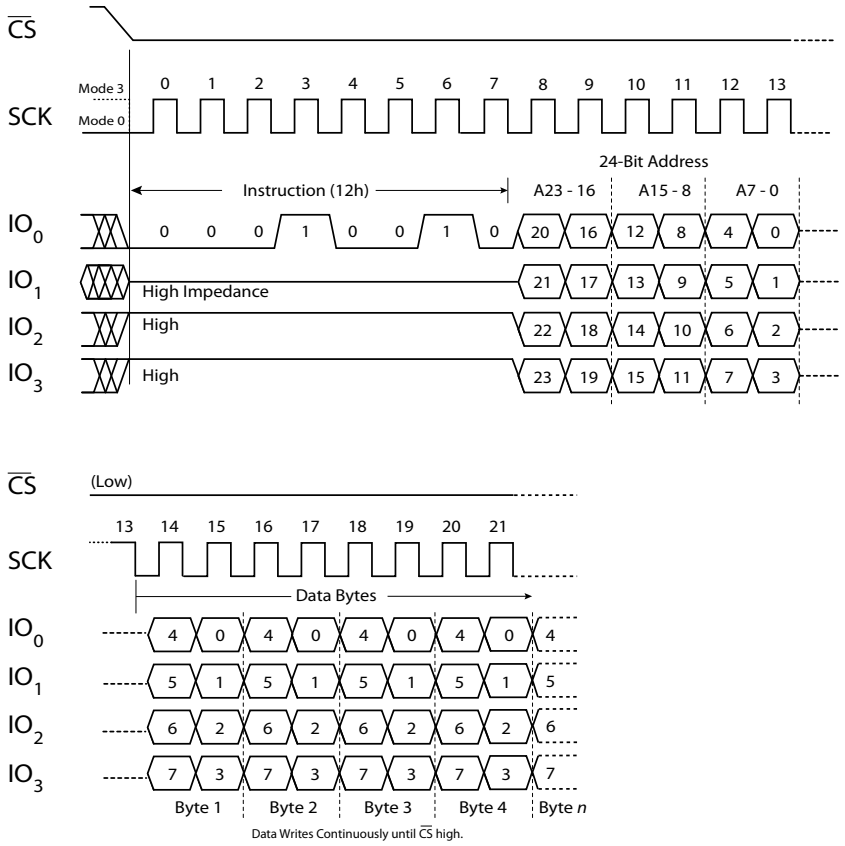
The FWQAD command is entered by driving $\overline{CS}$ low and sending the command code (12h). Data are input on all four I/O's and Writes continue as long as the memory is clocked. The command is terminated by bringing $\overline{CS}$ high.

Figure 20 – Fast Write Quad Address and Data (FWQAD) Command Operation

		Clock Number			
Name	**Description**	0 - 7 [1]	8 - 13 [4]	14 - 15 [2]	16 - *n*
FWQAD	Fast Write Quad Address and Data	12h	A23 - A0	D7 - D0 every two clocks until $\overline{CS}$ high [2]	

Notes:

1. Clocks 0 - 7 are the command byte. All commands and address bits on I/O_0.
2. Quad Mode address input. I/O_0 remains input. I/O_{1-3} active inputs until $\overline{CS}$ returns high.



QPI MODE

QPI Mode is designed to reduce command entry overhead in an XIP environment. QPI mode allows the instruction code to be entered on all four I/O's, which reduces the number of clock cycles required for command entry to two from eight. Otherwise, all SPI or Quad SPI commands operate normally.

In SPI or Quad SPI mode device operation is determined by which command is entered. To operate in QPI Mode, the device must be specifically placed into QPI Mode by invoking the Enable QPI Command. When in QPI Mode, the Status Register Bit 6 is set to 1 and will reset to 0 when either power is removed from the device or the QPI Mode is exited with an DQPI command.

At power up, QPI mode is disabled.

Table 10 – SPI Mode Command Structures in QPI Mode

		Clock Number					
Name	**Description**	0 - 1 [1]	2 - 9	10 - 17	18 - 25	26 - 33	34 - *n*
RDSR	Read Status Register	05h	S7-S0	-	-	-	-
WREN	Write Enable	06h	-	-	-	-	-
WRDI	Write Disable	04h	-	-	-	-	-
WRSR	Write Status Register	01h	S7-S0	-	-	-	-
READ	Read Data Bytes	03h	A23-A16	A15-A8	A7-A0	D7-D0 until $\overline{CS}$ high	
FREAD	Fast Read Data Bytes	08h	A23-A16	A15-A8	A7-A0	M7 - M0 [2]	D7-D0 until $\overline{CS}$ high
WRITE	Write Data Bytes	02h	A23-A16	A15-A8	A7-A0	D7-D0 until $\overline{CS}$ high	
SLEEP	Enter Sleep Mode	B9h	-	-	-	-	-
WAKE	Exit Sleep Mode	ABh	-	-	-	-	-
TDET	Tamper Detect	17h	M7 - M0 [3]	T7 - T0			
RDID	Read ID	4Bh	M7 - M0 [3]	Device ID 40 bits			
DQPI	Disable QPI	FFh	-	-	-	-	-

Notes:
1. Clocks 0 - 1 are the command bits while in QPI mode.
2. M7 - M0 is the Mode Byte to Set/Reset XIP Mode. Set XIP Mode = EFh; Reset XIP Mode = FFh.
3. Mode Byte must be FFh for TDET and RDID.

Table 11 – Quad SPI Mode Command Structures in QPI Mode

		Clock Number					
Name	**Description**	0 - 1 [1]	2 - 9	10 - 17	18 - 25	26 - 27	28 - *n*
DQPI	Disable QPI	FFh	-	-	-	-	-
FRQO	Fast Read Quad Output	6Bh	A23-A16	A15-A8	A7-A0	M7 - M0 [2]	D7-D0 until $\overline{CS}$ high
FWQD	Fast Write Quad Data	32h	A23-A16	A15-A8	A7-A0	D7-D0 until $\overline{CS}$ high	
		Clock Number					
Name	**Description**	0 - 1 [1]	2 - 3	4 - 5	6 - 7	8 - 9	10 - *n*
FRQAD	Fast Read Quad Address and Data	EBh	A23-A16	A15-A8	A7-A0	M7 - M0 [2]	D7-D0 until $\overline{CS}$ high
FWQAD	Fast Write Quad Address and Data	12h	A23-A16	A15-A8	A7-A0	D7-D0 until $\overline{CS}$ high	

Notes:

1. Clocks 0 - 1 are the command bits while in QPI mode.
2. Mode Byte. Set/Reset XIP operating mode. See "Execute in Place (XIP) Mode" on page 42.

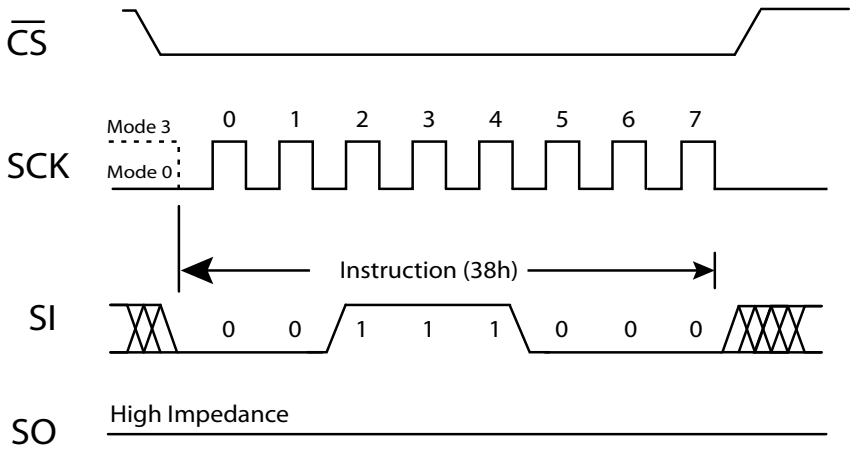
Enable QPI (EQPI) Command

The Enable QPI command is used to enter the device into QPI mode. The command code, 38h, is entered on the DI pin. The command is entered by driving $\overline{CS}$ low and sending the command code. The command is terminated by driving $\overline{CS}$ high. When in QPI Mode, the Status Register Bit 6 is set to "1" and the device stays in QPI mode until a power-on reset or the Disable QPI command is entered.

Figure 21 – Enable QPI Mode (EQPI) Command Operation

		Clock Number		
Name	**Description**	0 - 7 [1]	8	9 - *n*
EQPI	Enable QPI Mode	38h	$\overline{CS}$ high	In QPI Mode

Notes:
1. Clocks 0 - 7 are the command byte.



Disable QPI (DQPI) Command

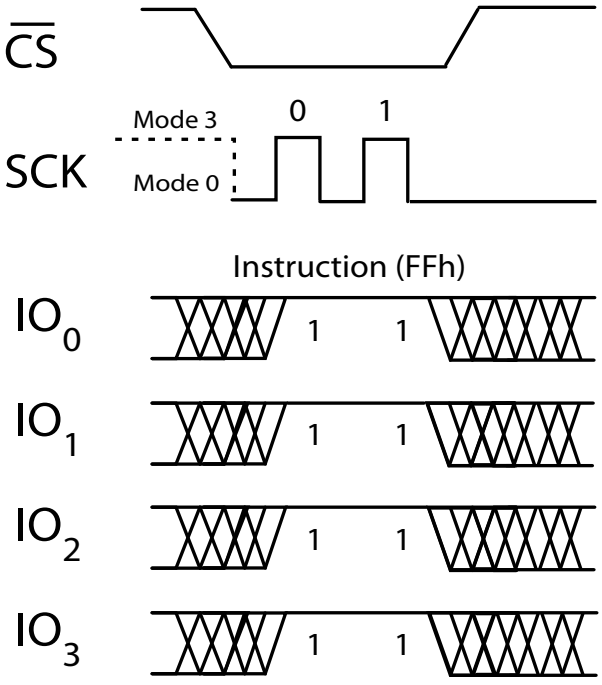
The Disable QPI command is used to exit QPI mode and return to the standard SPI/Quad SPI mode and set the Status Register Bit 6 to "0".

The command code FFh is entered on all four IO's in just two clock cycles as shown below. The command is entered by driving $\overline{CS}$ low and sending the command code. The command is terminated by driving $\overline{CS}$ high.

Figure 22 – Disable QPI Mode (DQPI) Command Timing

		Clock Number		
Name	**Description**	0 - 1 [1]	2	9 - *n*
DQPI	Disable QPI Mode	FFh	$\overline{CS}$ high	Now in SPI / Quad SPI Mode

Notes:
1. Clocks 0 - 1 are the command byte on all four I/O.



EXECUTE IN PLACE (XIP) MODE

Execute in Place (XIP) mode provides faster read operations by not requiring a command code for each new starting address during consecutive reads. This improves random access time and eliminates the need to shadow code onto RAM for fast execution. The read commands supported in XIP mode are FREAD (SPI Mode), FRQO, and FRQAD (both Quad SPI Mode commands).

XIP may be run when in QPI mode. Entering or exiting XIP mode will not affect other aspects of QPI mode operation. The device will stay in QPI mode until QPI is disabled with the DQPI command.

XIP mode for these commands is Set or Reset by entering the Mode Byte as shown in "Table 12 – Mode Byte Definitions to Set/Reset XIP Mode" on page 42 below.

In XIP Mode it is possible to perform a series of reads beginning at different addresses without having to load the command code for every new starting address / $\overline{CS}$ cycle. XIP can be entered or exited during these commands at any time and in any sequence. If it is necessary to perform another operation, not supported by XIP, such as a write, then XIP must be exited before the new command code is entered for the desired operation.

Table 12 – Mode Byte Definitions to Set/Reset XIP Mode

XIP Operation	Hex	M7	M6	M5	M4	M3	M2	M1	M0
Set/Continue	EF	1	1	1	0	1	1	1	1
Reset/Stop (Default)	FF	1	1	1	1	1	1	1	1

Table 13 – XIP Mode with FREAD Command

Initial Command		Clock Number				
SPI Mode		0 - 7 [1]	8 - 31	32 - 39	40 - 47	48 - *n*
QPI Mode		0 - 1 [1]	3 - 26	27 - 34	35 - 42	43 - *n*
FREAD	Fast Read Data Bytes	0Bh	A23-A0	M7 - M0 [2]	D7 - D0	Read Next Byte
			24-bit Address	Set XIP Mode [3]	Read Data Byte	Repeat until $\overline{CS}$ goes high.

Notes:

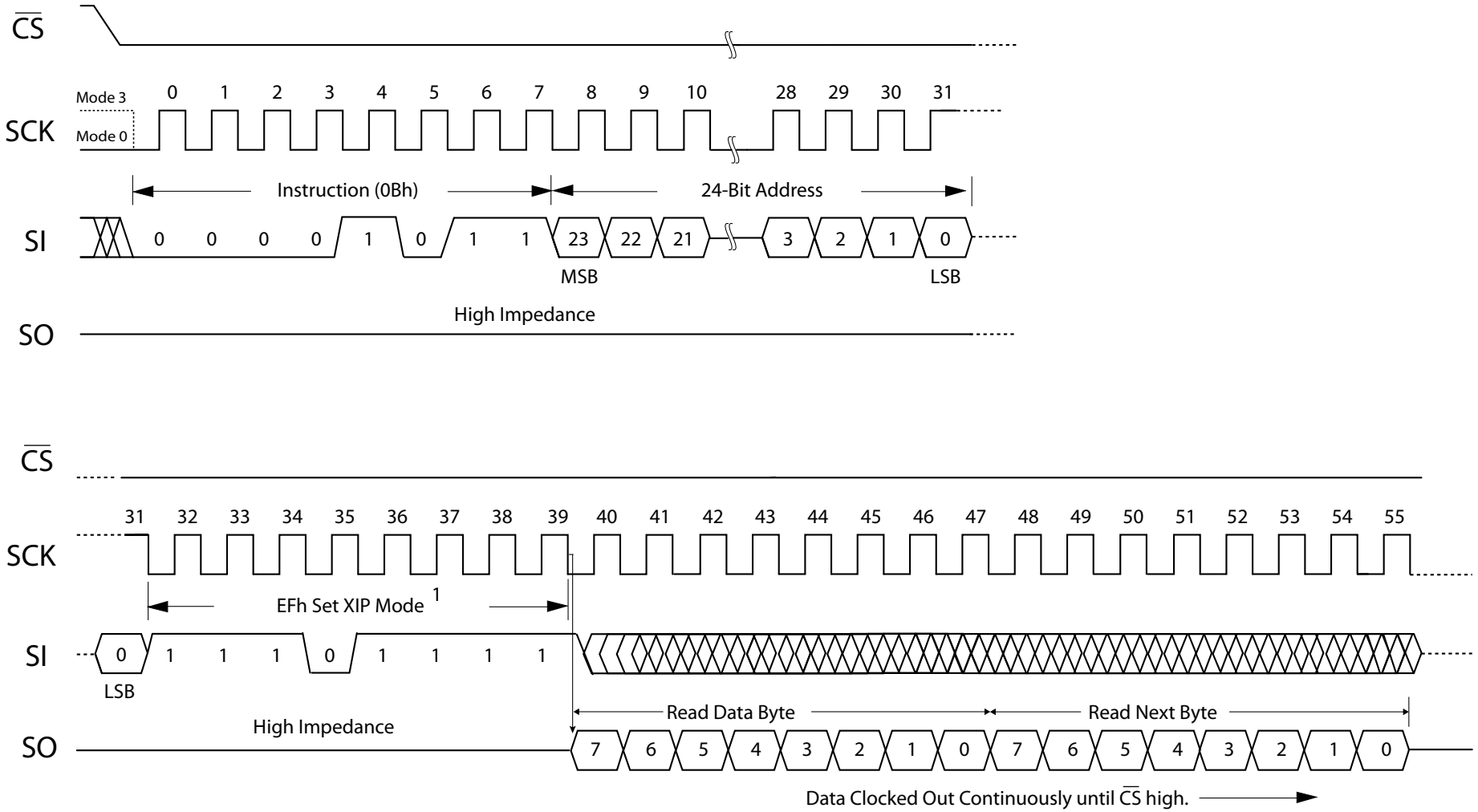
1. Command code eight bits.
2. Mode Byte will Set/Reset the XIP mode. See "Table 12 – Mode Byte Definitions to Set/Reset XIP Mode" on page 42 above for the Set/Reset XIP mode bit definitions.
3. If the XIP mode is not Set on the initial command, the command operates in normal SPI Mode until $\overline{CS}$ high. And, on the next new address, the FREAD the command must be reentered. If XIP Mode has been Set during this initial command entry, the command still operates normally until $\overline{CS}$ goes high. But on the next $\overline{CS}$ low, the device remains in FREAD Command mode. No command is entered and the initial read address is entered on the first clock. See the table below.

If XIP Set - Next $\overline{CS}$ ***Low***		Clock Number			
Either SPI or QPI Mode		0 - 23 [1]	24 - 31	32 - 39	40 - *n*
FREAD	Fast Read Data Bytes	A23-A0	M7 - M0	D7 - D0	Read Next Byte
If XIP Mode is Set, the Command need not be reentered. Initial 24-bit address entry begins on the first clock.		24-bit Address	Set/Reset XIP Mode	Read Data Byte	Repeat until $\overline{CS}$ goes high.

Notes:

1. In XIP mode, the last command code sent remains in effect. The starting address is entered beginning on the first clock after $\overline{CS}$ low.
2. If XIP Mode is Reset, the device is out of XIP mode and any command may be entered on the next access.

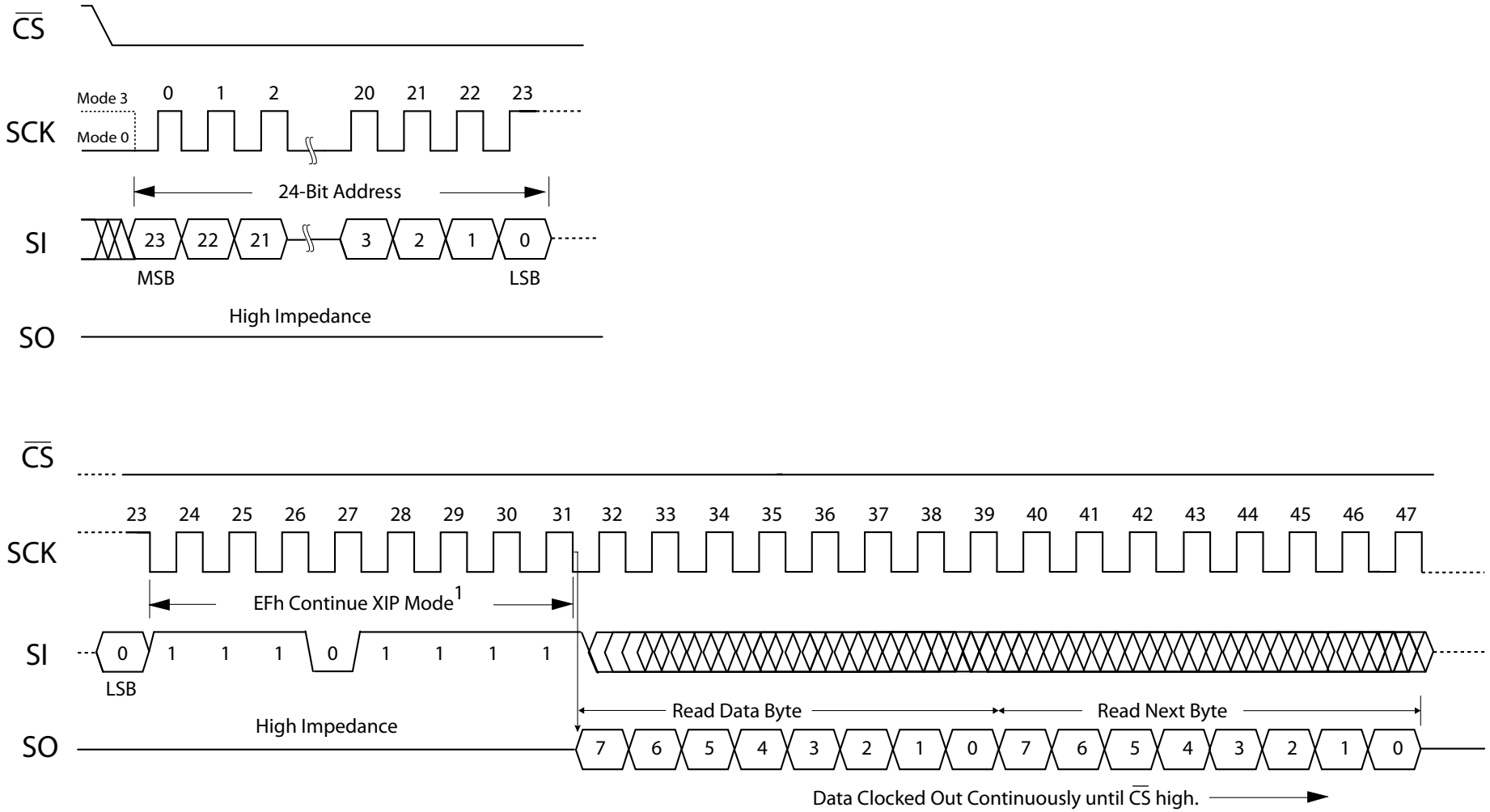
Figure 23 – FREAD Command- Set XIP Mode - Initial Access



Note:

1. Initial FREAD access, XIP mode set for next access.

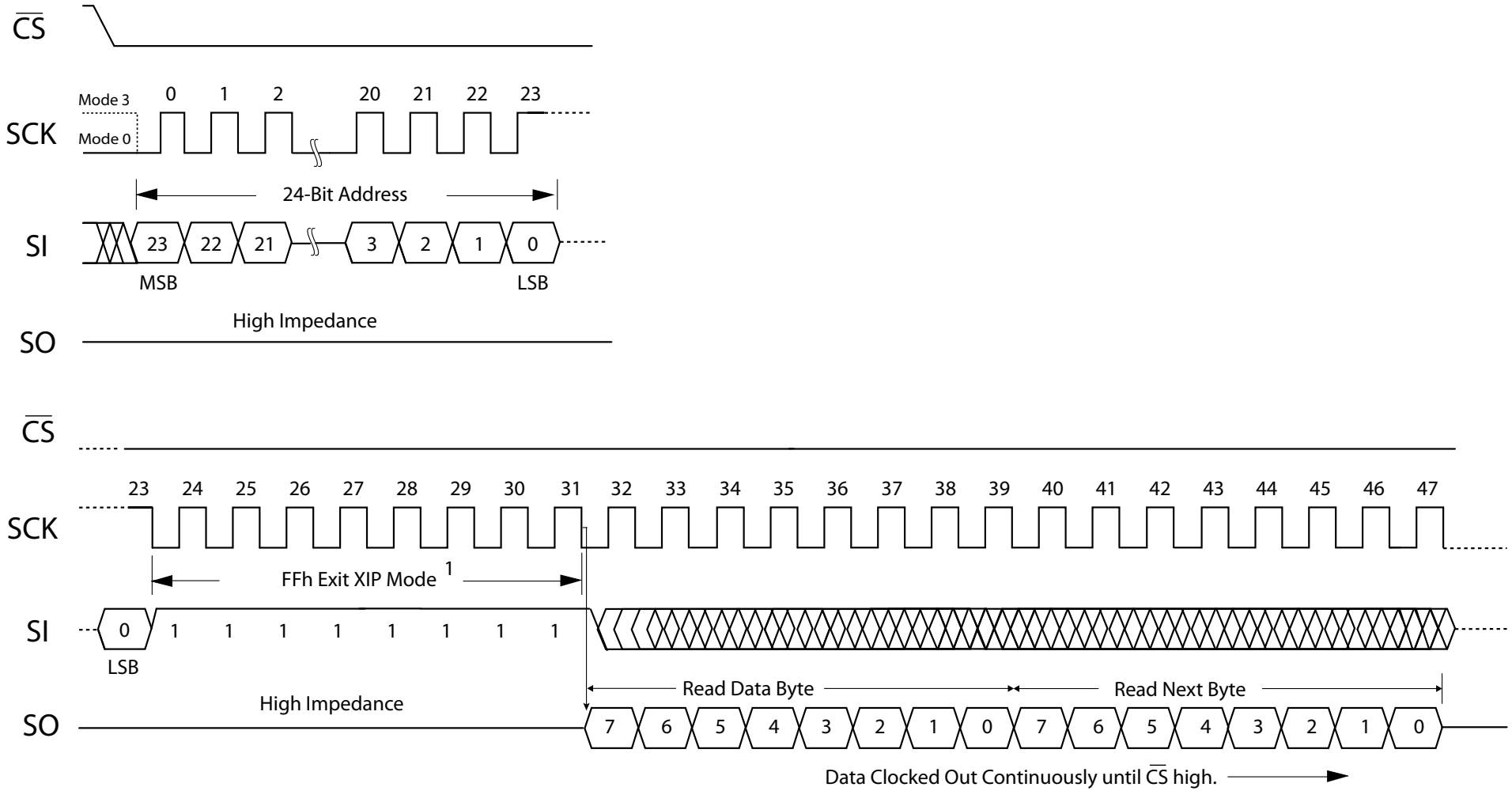
Figure 24 – FREAD Command - XIP Mode Set - Next Access



Note:

1. Continue FREAD in XIP Mode after this access.

Figure 25 – FREAD Command - XIP Mode Exit



Note:

1. XIP Mode code FFh: Reset XIP Mode. After this access a comnmand must be entered on the next access. Any new command may be entered, including the original command.

Table 14 – XIP Operation with FRQO Command

Initial Command		Clock Number				
Quad SPI Mode		0 - 7 [1]	8 - 31	32 - 33	34 - 35	36 - *n*
QPI Mode		0 - 1 [1]	2 - 25	26 - 27	28 - 29	30 - *n*
FRQO	Fast Read Quad Output	6Bh	A23-A0	M7 - M0 [2]	D7 - D0	Read Next Byte
			24-bit Address	Set XIP Mode [3]	Read Data Byte	Repeat until $\overline{CS}$ goes high.

Notes:

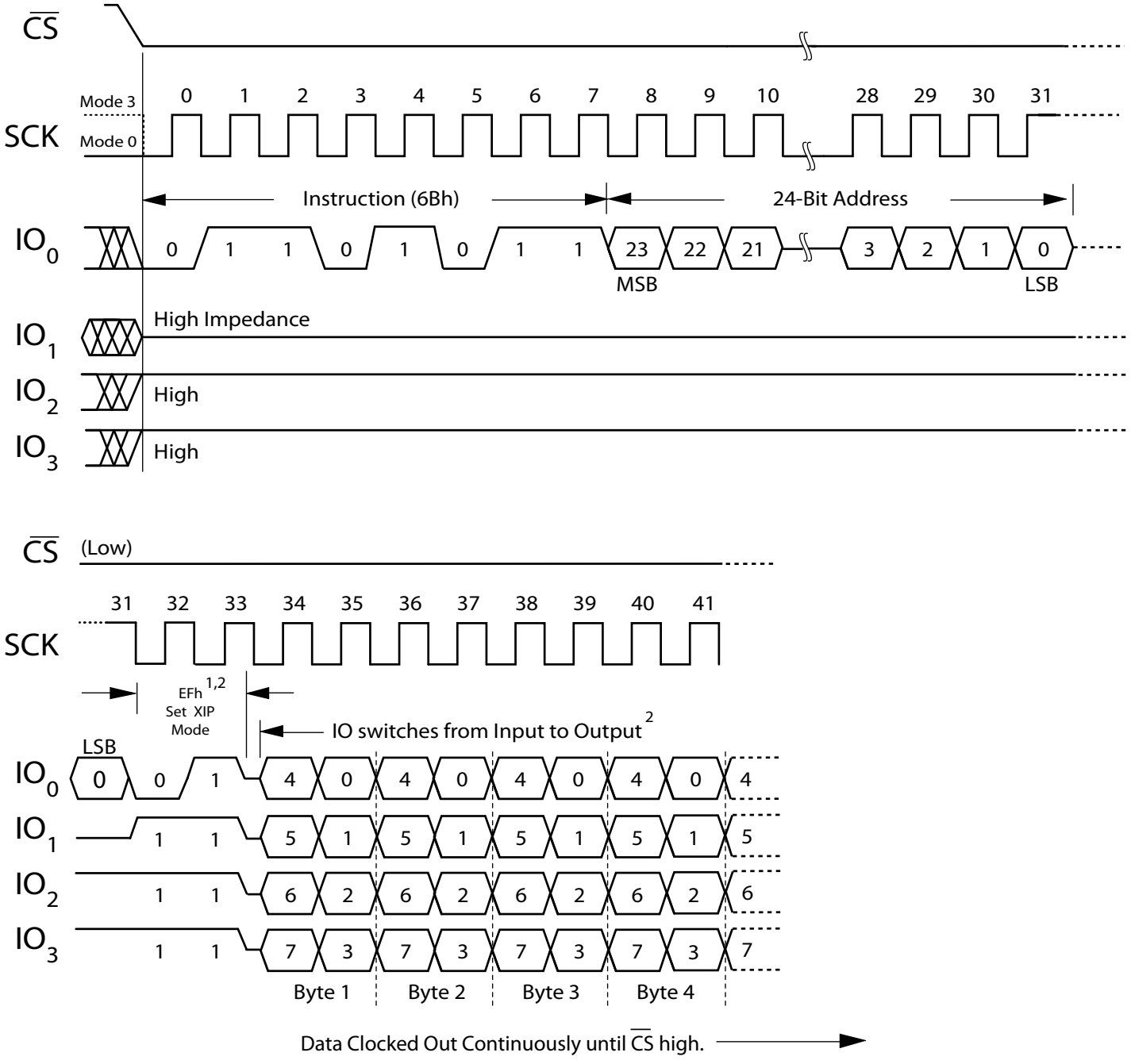
1. Command code eight bits.
2. Mode Byte entered Set/Reset the XIP mode. See "Table 12 – Mode Byte Definitions to Set/Reset XIP Mode" on page 42 above for the Set/Reset XIP mode bit definitions.
3. If the XIP mode is not set on the initial command, the command operates in normal SPI Mode until $\overline{CS}$ high. And, on the next FRQO the command must be reentered. If XIP has been set during this initial command entry, the command still operates normally until $\overline{CS}$ goes high. But on the next $\overline{CS}$ low, the device remains in FRQO Command mode, and the initial read address is entered on the first clock. See the table below.

If XIP Set - Next $\overline{CS}$ Low					
Either Quad SPI or QPI Mode		0 - 23	24 - 25	26 - 27	28 - *n*
FRQO Set	Fast Read Quad Output	A23-A0	M7 - M0	D7 - D0	Read Next Byte
If XIP Mode is Set, the Command need not be reentered. Initial 24-bit address entry begins on the first clock.		24-bit Address	Set/Reset XIP Mode	Read Data Byte	Repeat until $\overline{CS}$ goes high.

Notes:

1. In XIP operating mode, the last command code sent remains in effect and no command entry is required on the next access.

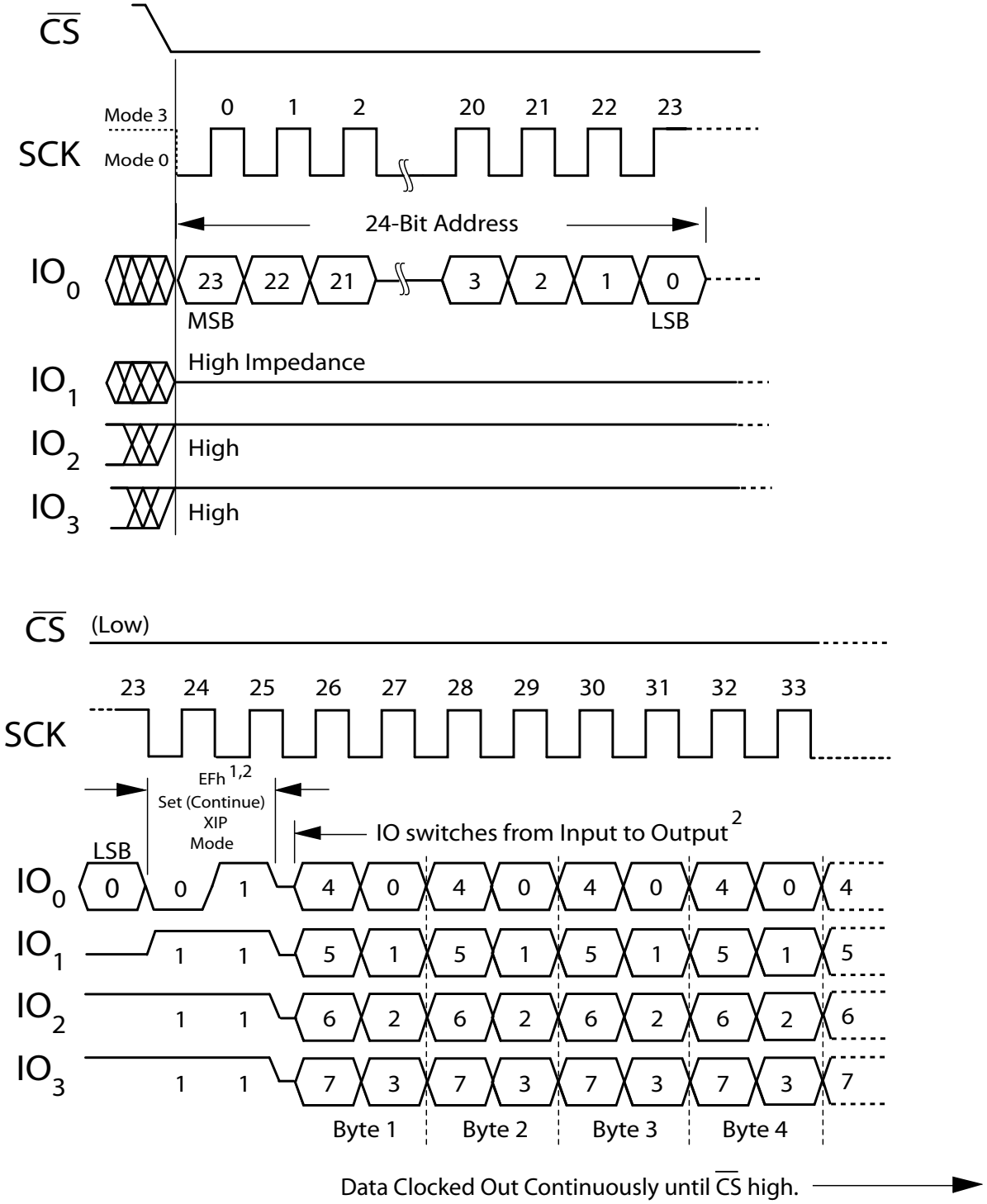
Figure 26 – FRQO Command - Set XIP Mode - Initial Access



Notes:

1. Initial access, XIP Mode Byte set for next access.
2. The I/O pins should be high impedance prior to the falling edge of the second mode clock.

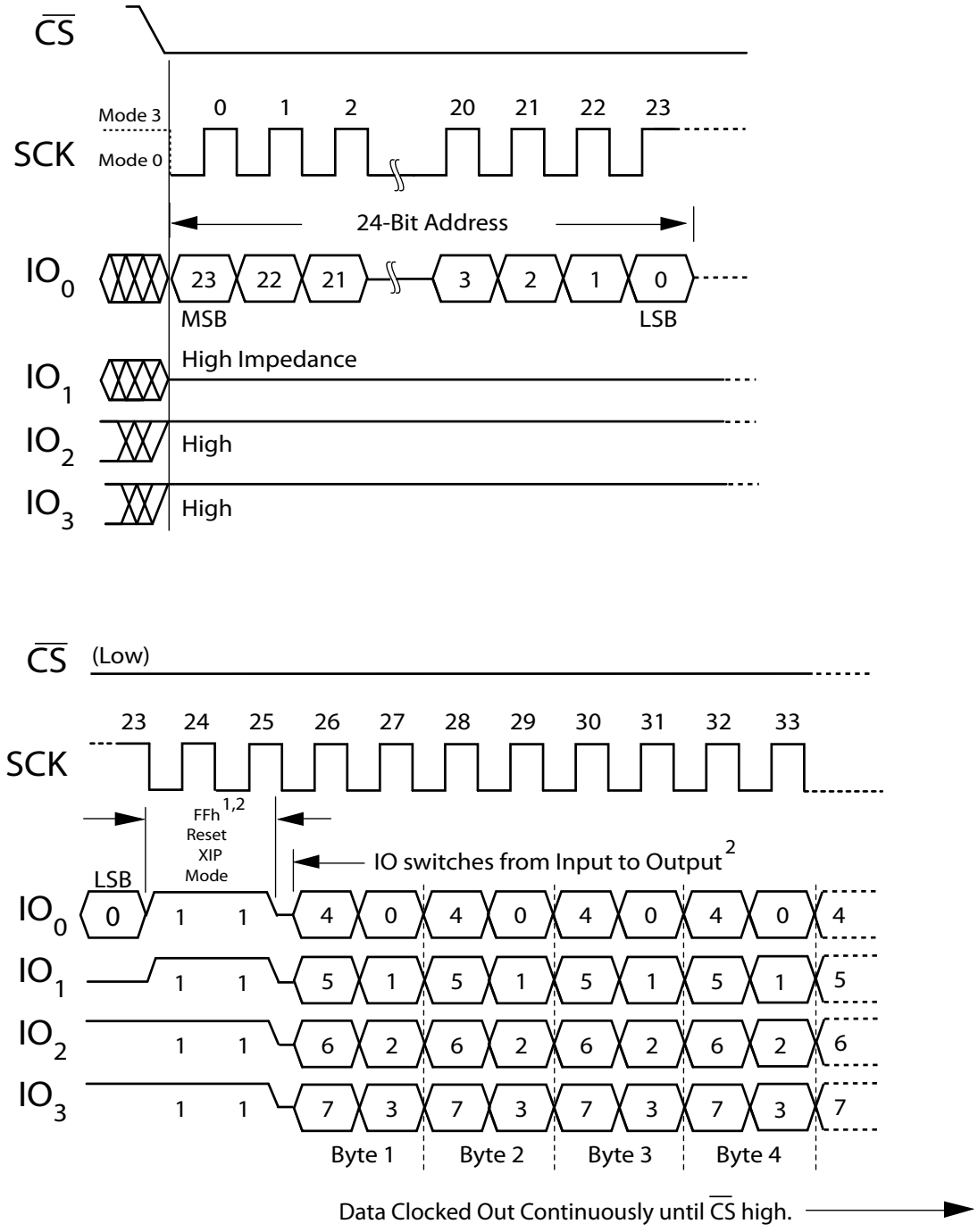
Figure 27 – FRQO Command - XIP Mode Set - Next Access



Notes:

1. Next access, set to continue XIP Mode.
2. The I/O pins should be high impedance prior to the falling edge of the second mode clock.

Figure 28 – FRQO Command - XIP Mode Exit



Notes:

1. XIP Mode Byte FFh. Exit XIP Mode.
2. The I/O pins should be high impedance prior to the falling edge of the second mode clock.
3. After this access a command must be entered on the next access. Any new command may be entered, including the original command.

Table 15 – XIP Operation with FRQAD Command

Initial Command		Clock Number				
Quad SPI Mode		0 - 7 [1]	8 - 13	14 - 15	16 - 17	18 - *n*
QPI Mode		0 - 1 [1]	2 - 7	8 - 9	10 - 11	12 - *n*
FRQAD	Fast Read Quad Address and Data	EBh	A23-A0	M7 - M0 [2]	D7 - D0	Read Next Byte
			24-bit Address	Set XIP Mode [3]	Read Data Byte	Repeat until $\overline{CS}$ goes high.

Notes:

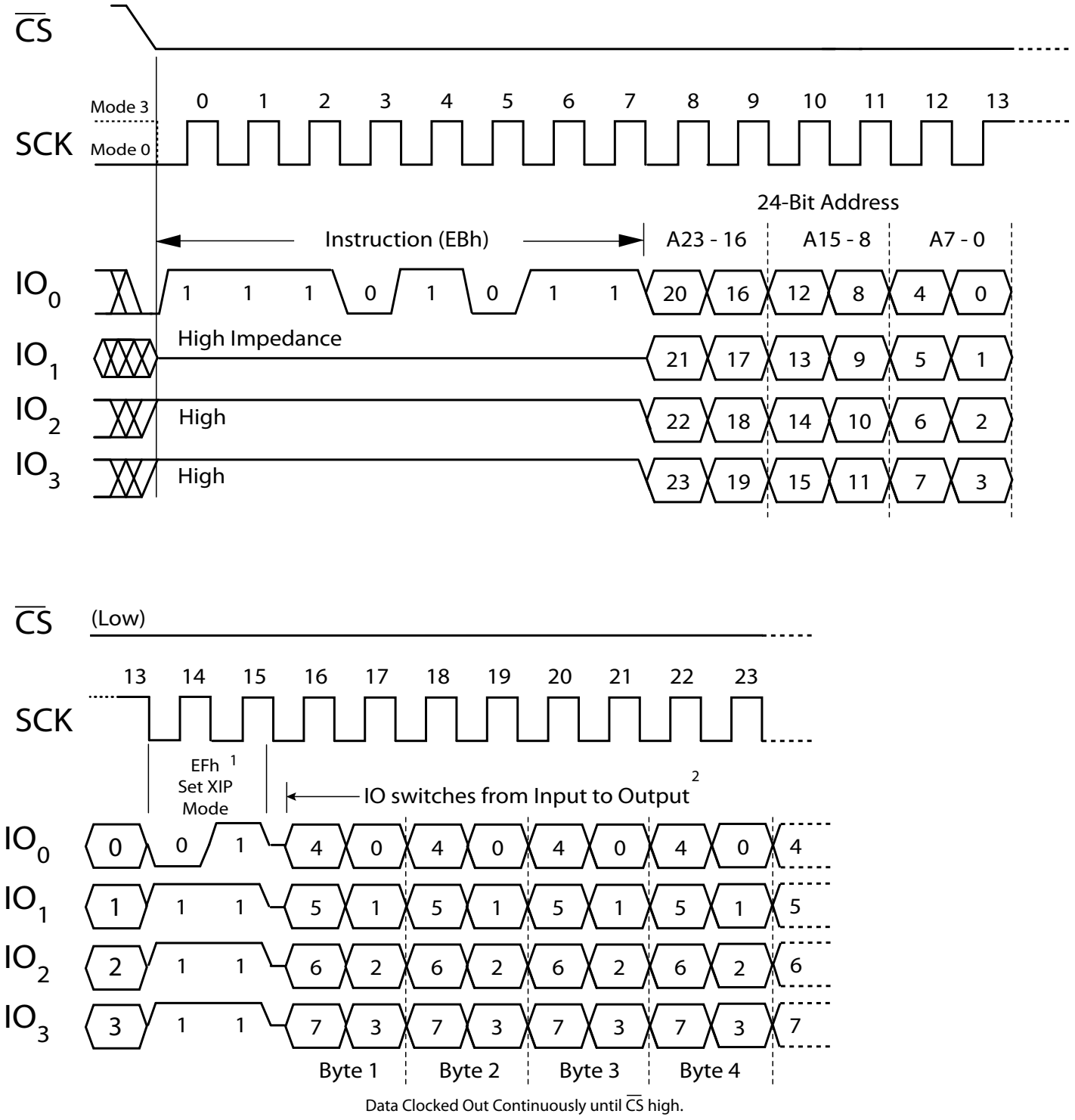
1. Command code eight bits.
2. Mode Byte entered Set/Reset the XIP mode. See "Table 12 – Mode Byte Definitions to Set/Reset XIP Mode" on page 42 above for the Set/Reset XIP mode bit definitions.
3. If the XIP mode is not set on the initial command, the command operates in normal SPI Mode until $\overline{CS}$ high. And, on the next FRQAD the command must be reentered. If XIP has been set during this initial command entry, the command still operates normally until $\overline{CS}$ goes high. But on the next $\overline{CS}$ low, the device remains in FREAD Command mode, and the initial read address is entered on the first clock. See the table below.

If XIP Set - Next $\overline{CS}$ Low					
Either Quad SPI or QPI Mode		0 - 5	6 - 7	8 - 9	10 - *n*
FRQAD Set	Fast Read Quad Address and Data	A23-A0	M7 - M0	D7 - D0	Read Next Byte
If XIP Mode is Set, the Command need not be reentered. Initial 24-bit address entry begins on the first clock.		24-bit Address	Set/Reset XIP Mode	Read Data Byte	Repeat until $\overline{CS}$ goes high.

Notes:

1. In XIP operating mode, the last command code sent remains in effect and no command entry is required on the next access.

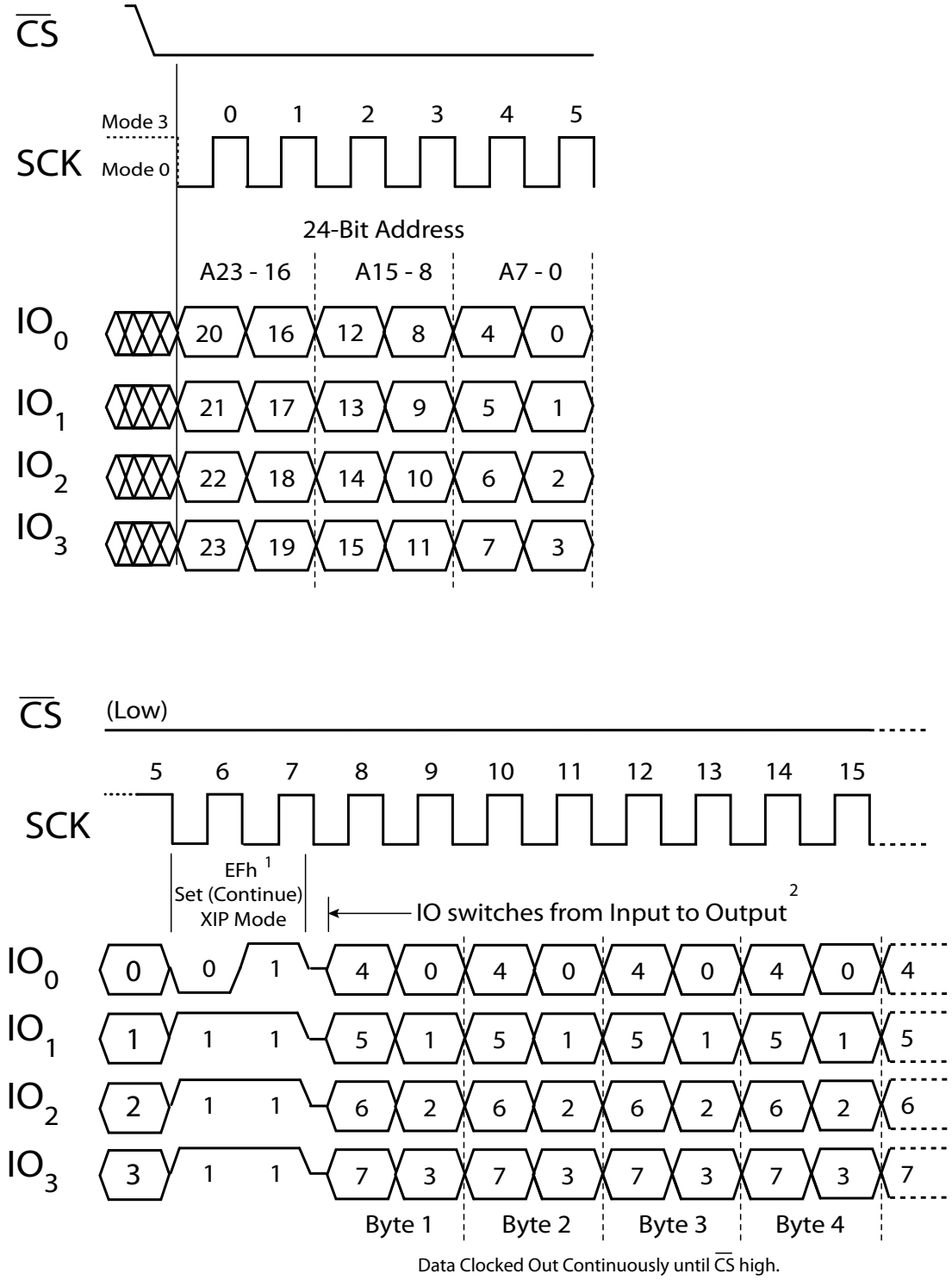
Figure 29 – FRQAD Command - Set XIP Mode - Initial Access



Notes:

1. Initial access, XIP Mode Byte set for next access.
2. The I/O pins should be high impedance prior to the falling edge of the second mode clock.

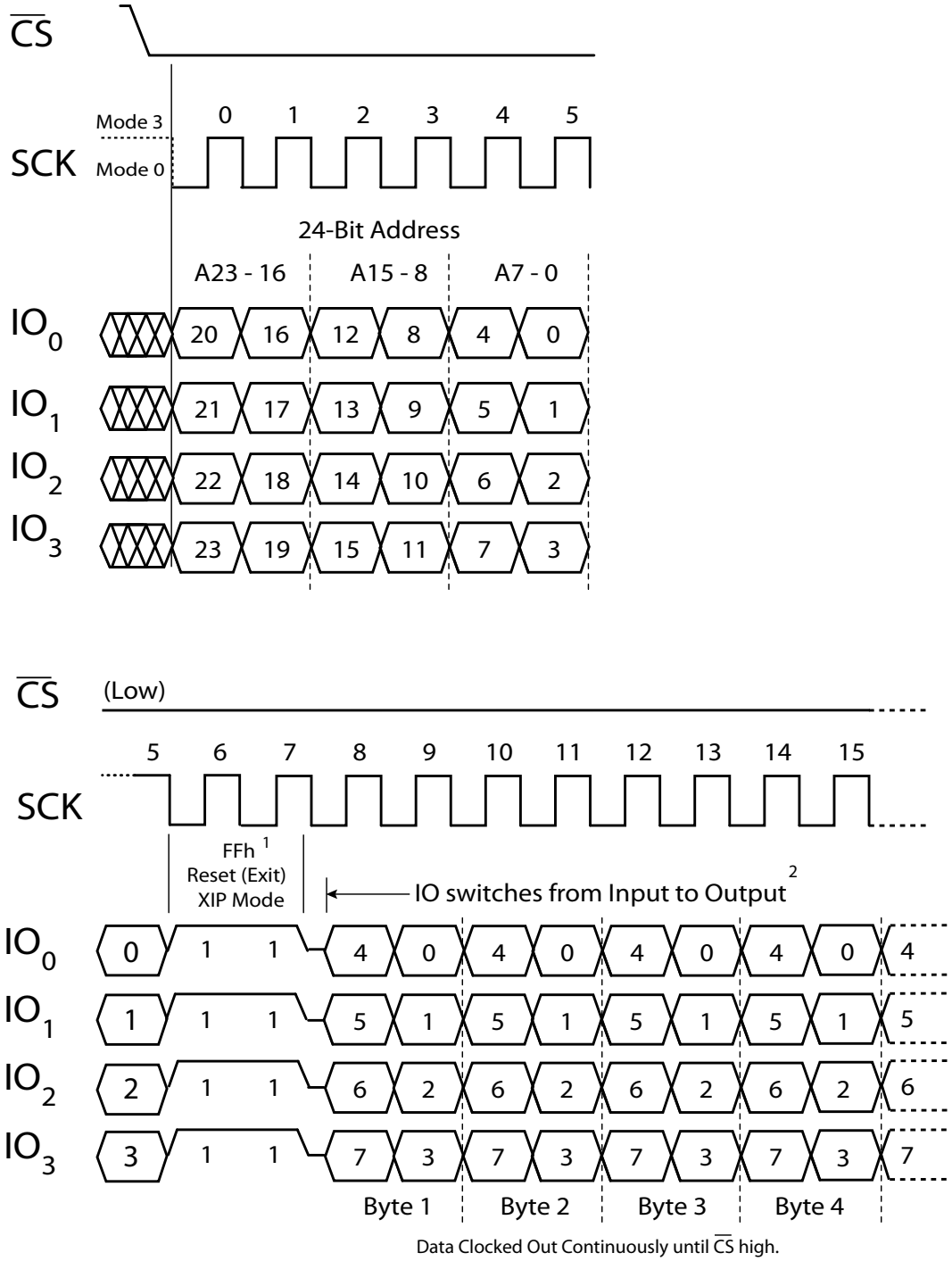
Figure 30 – FRQAD Command - XIP Mode Set - Next Access



Notes:

1. Next access, set to continue XIP Mode.
2. The I/O pins should be high impedance prior to the falling edge of the second mode clock.

Figure 31 – FRQAD Command - XIP Mode Exit



Notes:

1. XIP Mode Byte FFh. Exit XIP Mode.
2. The I/O pins should be high impedance prior to the falling edge of the second mode clock.
3. After this access a command must be entered on the next access. Any new command may be entered, including the original command.

ELECTRICAL SPECIFICATIONS

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 16 – Absolute Maximum Ratings

Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.

Symbol	Parameter	Conditions	Value	Unit
V_{DD}	Supply voltage [1]		-0.5 to 4.0	V
V_{DDQ}	I/O Bus Supply voltage [1]		-0.5 to 2.4	V
V_{IN}	Voltage on any pin [1]		-0.5 to V_{DDQ} + 0.5	V
I_{OUT}	Output current per pin		±20	mA
T_{BIAS}	Temperature under bias	Commercial Grade	-45 to 95	°C
T_{stg}	Storage Temperature		-55 to 150	°C
T_{Lead}	Lead temperature during solder (3 minute max)		260	°C
H_{max_write}	Maximum magnetic field during write	Write	12,000	A/m
H_{max_read}	Maximum magnetic field during read or standby	Read or Standby	12,000	A/m

Notes:

1. All voltages are referenced to V_{SS}. The DC value of V_{IN} must not exceed actual applied V_{DD} by more than 0.5V. The AC value of V_{IN} must not exceed applied V_{DD} by more than 2V for 10ns with I_{IN} limited to less than 20mA.

Table 17 – Operating Conditions

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
V_{DD}	Power supply voltage		3.0	3.3	3.6	V
V_{DDQ}	I/O Bus Power supply voltage		1.7	1.8	2.0	V
V_{IH}	Input high voltage		1.4		V_{DDQ} + 0.2	V
V_{IL}	Input low voltage		-0.2		0.4	V
T_A	Ambient temperature under bias	Commercial Grade	0		70	°C
		Industrial Grade	-40		85	°C
		Extended Grade	-40		105	°C

Table 18 – DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
I_{IL}	Input leakage current		-	±2	µA
I_{OL}	Output leakage current		-	±2	µA
V_{OL}	Output low voltage	I_{OL} = 4mA	-	0.4	V
V_{OH}	Output high voltage	I_{OH} = -100µA	1.4	-	V

Table 19 – Power Supply Characteristics

Symbol	Parameter	Conditions	Typical	Max	Unit
I_{DDR}	Active Read Current	SPI @ 1 MHz	5.0	11	mA
		SPI @ 40 MHz	12	17	mA
		Quad SPI @ 104MHz	-	60	mA
I_{DDW}	Active Write Current	@ 1 MHz	9.0	25	mA
		@ 40 MHz	28	42	mA
		Quad SPI @ 104MHz	-	100	mA
I_{DDQ}	Active V_{DDQ} Current	Note 1	-	3	mA
I_{SB1}	AC Standby Current ($\overline{CS}$ High = V_{IH}. No other restrictions on other inputs.)	f ≤104MHz	-	8	mA
I_{SB1Q}	AC Standby Current on V_{DDQ} supply ($\overline{CS}$ High = V_{IH}. No other restrictions on other inputs.)	f ≤104MHz	-	1	mA
I_{SB2}	CMOS Standby Current ($\overline{CS}$ High)	f = 0 MHz	-	3	mA
I_{SB2Q}	CMOS Standby Current on V_{DDQ} Supply ($\overline{CS}$ High)	f = 0 MHz	-	10	µA
I_{ZZ}	Standby Sleep Mode Current ($\overline{CS}$ High)	Sleep Mode	-	100	µA

Note

1. I_{DDQ} Conditions: Quad SPI at 104MHz, V_{DDQ} = 2.0v, V_{IH} = 1.8v, V_{IL} = 0v.

Table 20 – Capacitance

Symbol	Parameter	Typical	Max	Unit
C_{In}	Control input capacitance [1]	-	6	pF
$C_{I/O}$	Input/Output capacitance [1]	-	8	pF

Notes:

1. f = 1.0 MHz, dV = 3.0 V, T_A = 25 °C, periodically sampled rather than 100% tested.

TIMING SPECIFICATIONS

AC Measurement Conditions

Table 21 – AC Measurement Conditions

Parameter	Value	Unit
Logic input timing measurement reference level	0.9	V
Logic output timing measurement reference level	0.9	V
Logic input pulse levels	0 to 1.6	V
Input rise/fall time	2	ns
Output load for low and high impedance parameters	See Figure 32	
Output load for all other timing parameters	See Figure 33	

Figure 32 – Output Load for Impedance Parameter Measurements

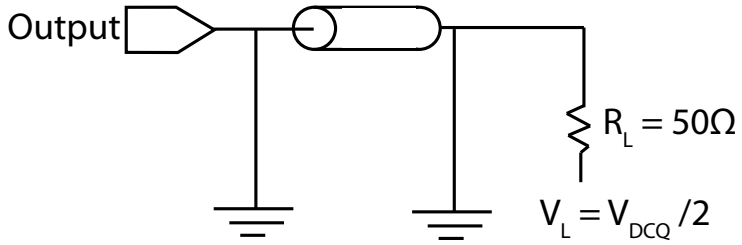
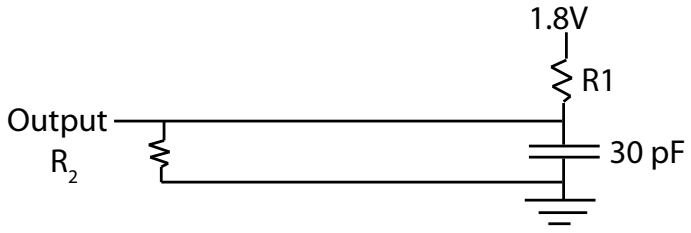


Figure 33 – Output Load for all Other Parameter Measurements



Power Up Timing

To provide protection for data during initial power up, power loss or brownout, whenever V_{DD} falls below V_{WIDD} or V_{DDQ} falls below V_{WIDDQ} the device cannot be selected ($\overline{CS}$ is restricted from going low) and the device is inhibited from Read or Write operations. See "Table 22 – Power-Up Delay Minimum Voltages and Timing" below.

Power Up Delay Time

During initial power up or when recovering from brownout or power loss, a power up delay time (^{t}PU) must be added to the time required for voltages to rise to their specified minimum voltages ($V_{DD(min)}$ and $V_{DDQ(min)}$) before normal operations may commence. This time is required to insure that the device internal voltages have stabilized. See "Table 22 – Power-Up Delay Minimum Voltages and Timing" below.

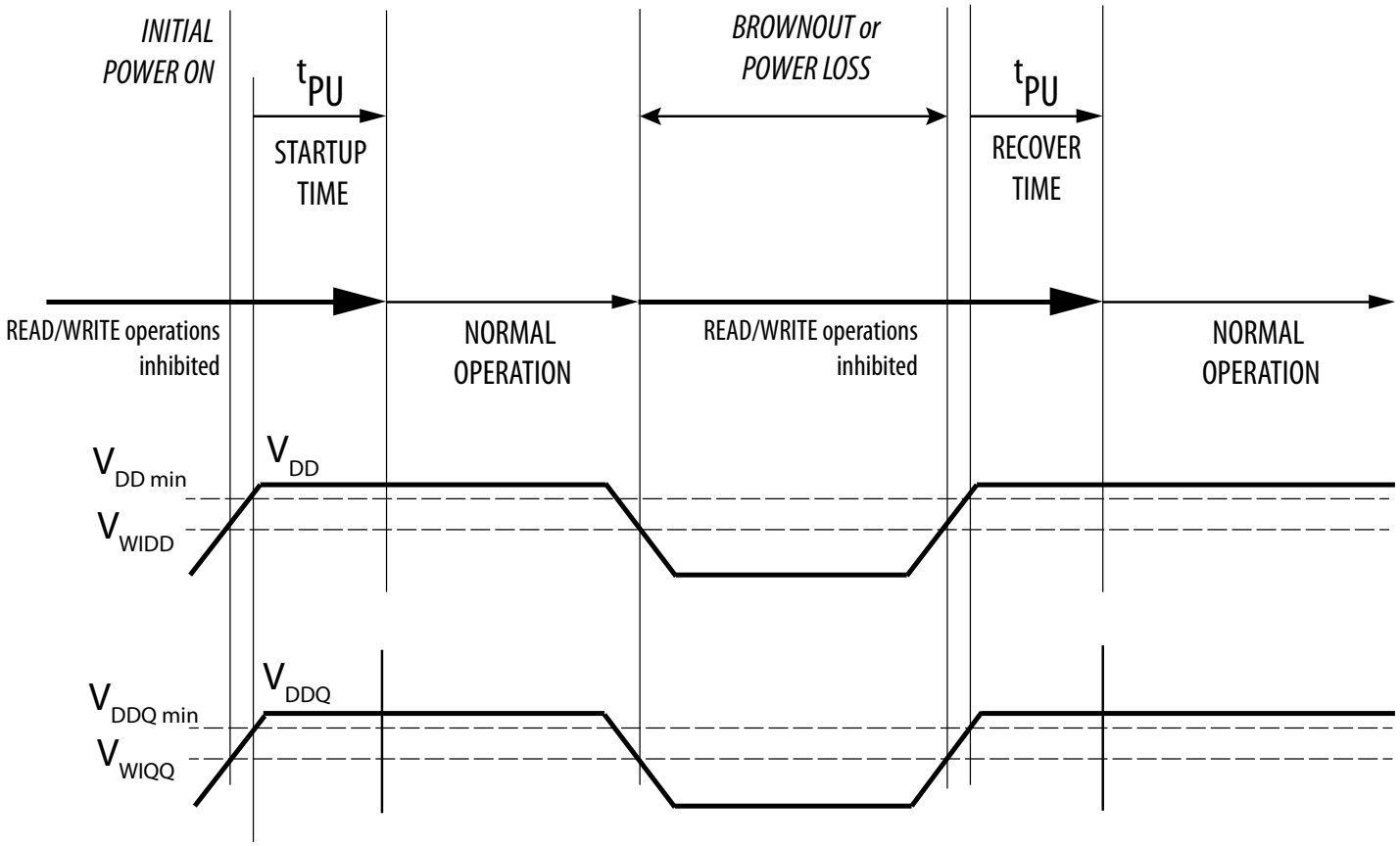
^{t}PU is measured from the time that both V_{DD} and V_{DDQ} have reached their specified minimum voltages. See "Figure 34 – Power-Up Timing" for an illustration of the timing.

During initial startup or power loss recovery the $\overline{CS}$ pin should always track V_{DDQ} (up to V_{DDQ} + 0.2 V) or V_{IH}, whichever is lower, and remain high for the total startup time, ^{t}PU. In most systems, this means that $\overline{CS}$ should be pulled up to V_{DDQ} with a resistor. Any logic that drives other inputs or IOs should hold the signals at V_{DDQ} until normal operation can commence.

Table 22 – Power-Up Delay Minimum Voltages and Timing

Symbol	Parameter	Min	Unit
V_{WIDD}	Write Inhibit Voltage	2.2	V
V_{WIDDQ}	I/O Write Inhibit Voltage	1.2	V
^{t}PU	Power Up Delay Time	400	µs

Figure 34 – Power-Up Timing



Note: $\overline{CS}$ may not be enabled until ^{t}PU startup or recovery time is met.

AC Timing Parameters

Table 23 – AC Timing Parameters

Symbol	Parameter	Min	Typical	Max	Unit
^{f}SCK	SCK Clock Frequency for all instructions except READ	-	-	104	MHz
	SCK Clock freq for READ	-	-	40	MHz
^{t}RI	Input Rise Time	-	-	50	ns
^{t}RF	Input Fall Time	-	-	50	ns
^{t}WH	SCK High Time except READ	4	-	-	ns
^{t}WHR	SCK High Time READ	11	-	-	ns
^{t}WL	SCK Low Time except READ	4	-	-	ns
^{t}WLR	SCK Low Time READ	12	-	-	ns
Synchronous Data Timing see Figures 35, 36, 37, 38					
^{t}CSS	$\overline{CS}$ Setup Time	5	-	-	ns
^{t}CSH	$\overline{CS}$ Hold Time	5	-	-	ns
^{t}SU	Data In Setup Time	2	-	-	ns
^{t}H	Data In Hold Time	5	-	-	ns
^{t}V	Output Valid	-	-	7	ns
^{t}HO	Output Hold Time	1.5	-	-	ns
^{t}CS	$\overline{CS}$ High Time at end of all Cycles except Writes	10	-	-	ns
^{t}CSW	$\overline{CS}$ High Time at end of Write Cycles	50	-	-	ns

AC Timing Parameters - Continued

Symbol	Parameter	Min	Typical	Max	Unit
$\overline{\text{HOLD}}$ **Timing see Figure 39**					
^{t}HD	$\overline{\text{HOLD}}$ Setup Time	2	-	-	ns
^{t}CD	$\overline{\text{HOLD}}$ Hold Time	2	-	-	ns
^{t}LZ	$\overline{\text{HOLD}}$ to Output Low Impedance	-	-	12	ns
^{t}HZ	$\overline{\text{HOLD}}$ to Output High Impedance	-	-	7	ns
Other Timing Specifications					
^{t}WPS	WP Setup To CS Low	5	-	-	ns
^{t}WPH	WP Hold From CS High	5	-	-	ns
^{t}DP	Sleep Mode Entry Time	-	-	3	µs
^{t}RDP	Sleep Mode Exit Time	-	-	400	µs
^{t}DIS	Output Disable Time	-	-	7	ns

Figure 35 – Synchronous Data Timing (READ)

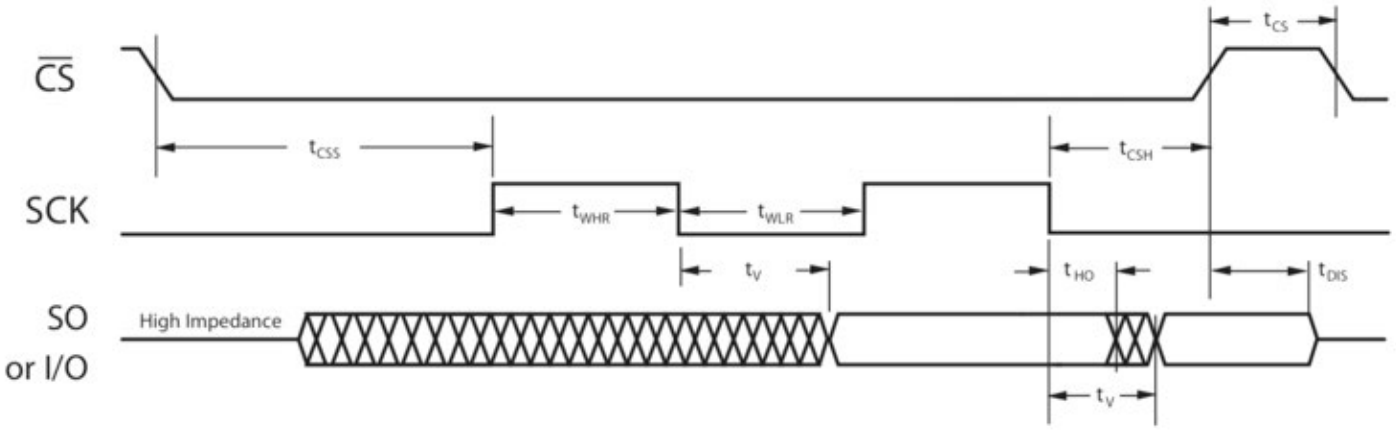


Figure 36 – Synchronous Data Timing Fast Read (FREAD)

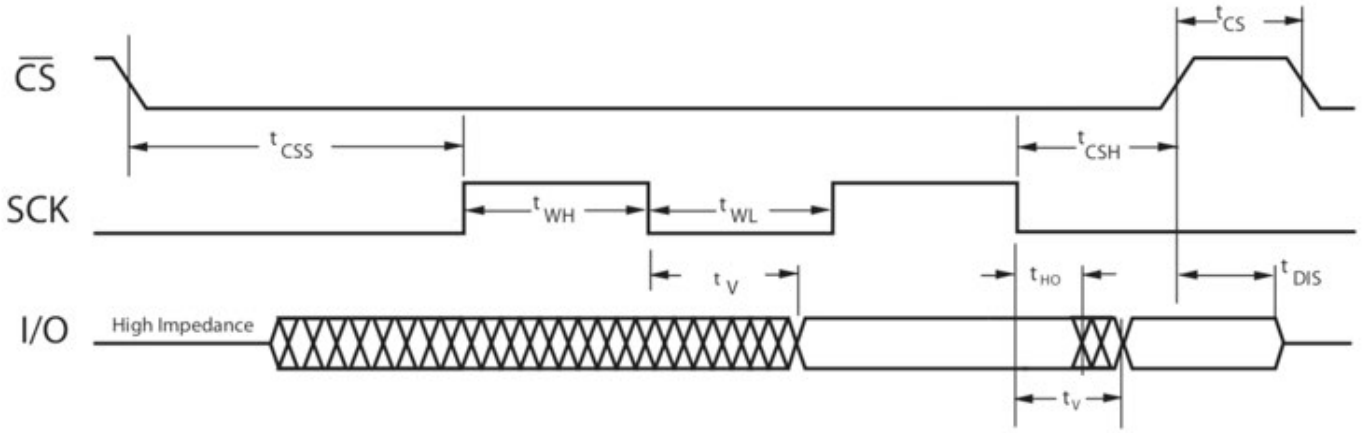


Figure 37 – Synchronous Data Timing (WRITE)

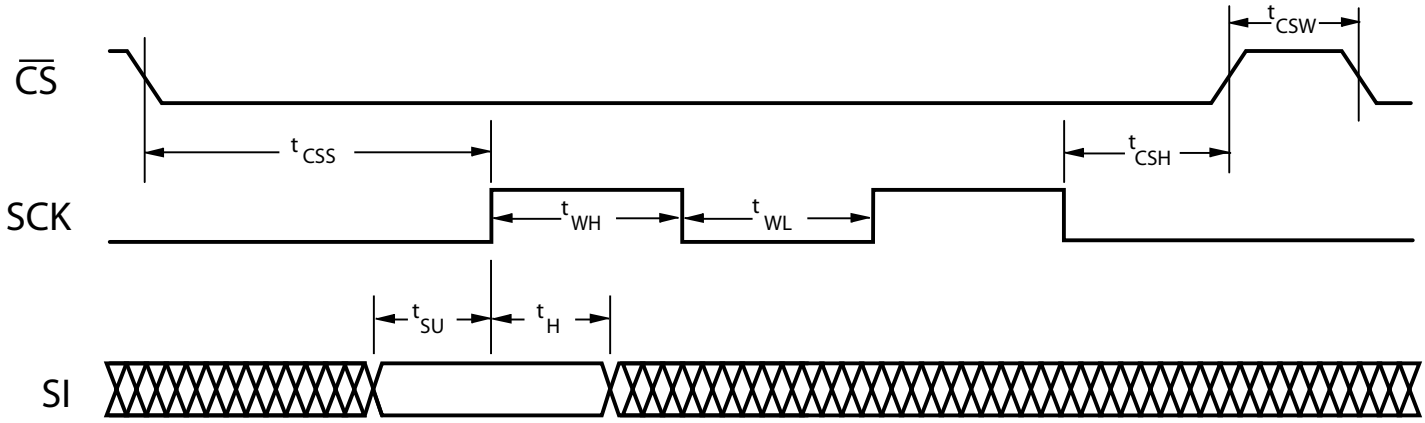


Figure 38 – Synchronous Data Timing Fast Write Quad Data and Fast Write Quad Address and Data (FWQD and FWQAD)

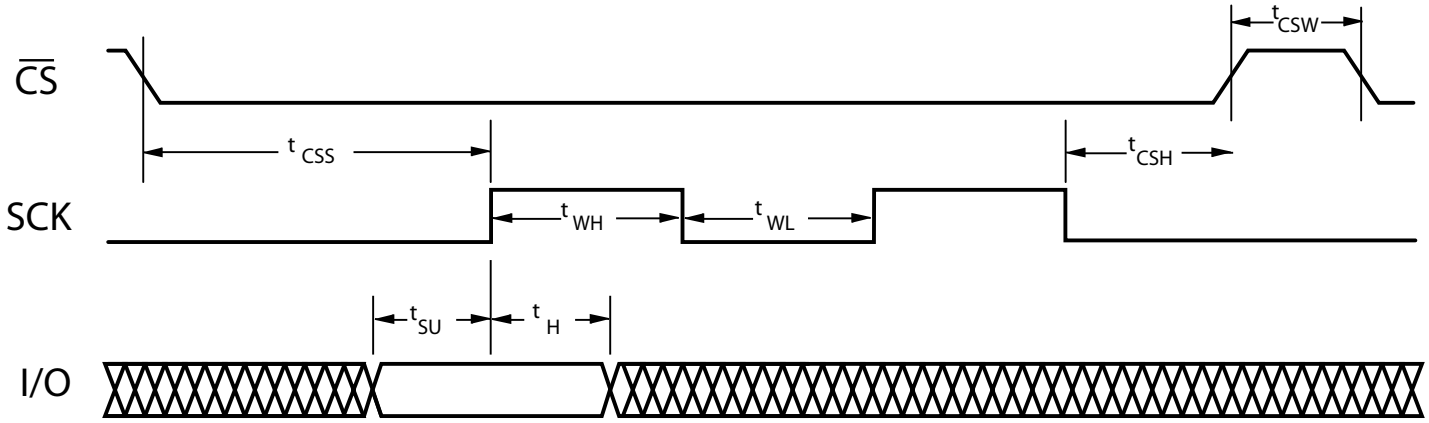
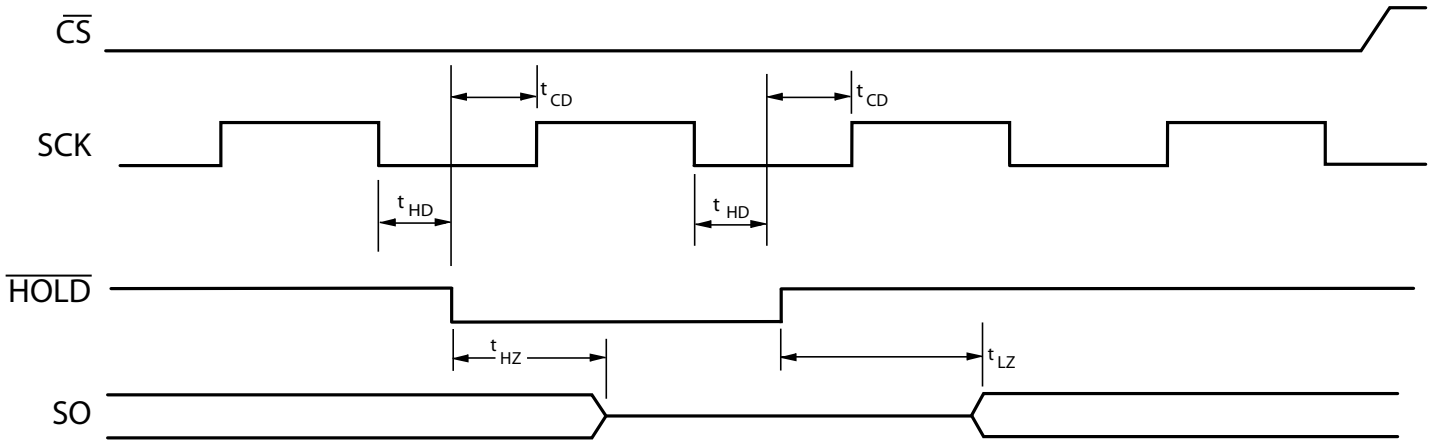


Figure 39 – $\overline{\text{HOLD}}$ Timing



PART NUMBERS AND ORDERING

Table 24 – Part Numbering System

			Memory	Interface	Density	Revision	Temp	Package	Ship	Grade
Example Ordering Part Number			MR	10Q	010		C	SC	R	
MRAM (Toggle)		MR								
104MHz Quad SPI Family		10Q								
1 Mb		010								
4 Mb		040								
16Mb		160								
No Revision		Blank								
Revision A		A								
Revision B		B								
Commercial	0 to 70°C	Blank								
Industrial	-40 to 85°C	C								
Extended	-40 to 105°C	V								
16-pin SOIC		SC								
24-ball BGA		MB								
Tray		Blank								
Tape and Reel		R								
Customer Samples		CS								
Mass Production		Blank								

Table 25 – Ordering Part Numbers

Temp Grade	Temperature	Package	Shipping Container	Order Part Number
Commercial	0 to 70°C	16-SOIC	Trays	MR10Q010SC
			Tape and Reel	MR10Q010SCR
		24-BGA	Trays	MR10Q010MB
			Tape and Reel	MR10Q010MBR
Industrial	-40 to 85°C	16-SOIC	Trays	MR10Q010CSC
			Tape and Reel	MR10Q010CSCR
		24-BGA	Trays	MR10Q010CMB
			Tape and Reel	MR10Q010CMBR
Extended	-40 to 105°C	16-SOIC	Trays	MR10Q010VSC
			Tape and Reel	MR10Q010VSCR
		24-BGA	Trays	MR10Q010VMB
			Tape and Reel	MR10Q010VMBR

PACKAGE CHARACTERISTICS

Table 26 – Thermal Resistance 16-pin SOIC

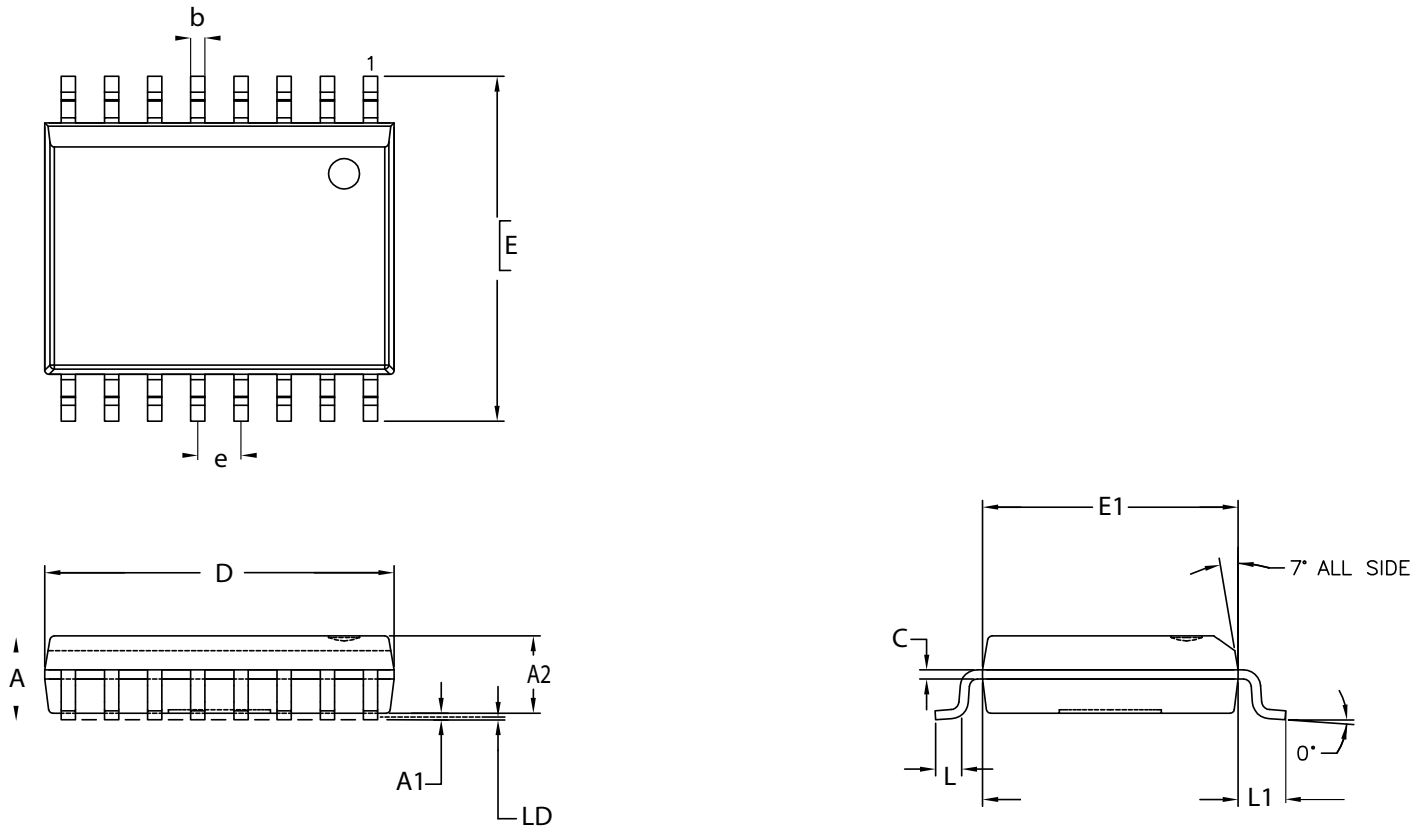
All thermal resistance values are estimated by simulation.

Velocity	T_A [1]	P_D [2]	T_J Max [3]	Θ_{JA} [4]	Θ_{JB} [5]	Θ_{JC} [6]
m/s	°C	W	°C	°C/W		
0	25	0.792	71.0	58.1	30.6	31.6
1			64.5	49.9		
2			62.8	47.7		
3			61.8	46.4		

Notes:

1. T_A - Ambient temperature.
2. P_D - Power dissipation at maximum V_{DD} and I_{DDW}.
3. T_J Max - Maximum junction temperature reached at maximum power dissipation.
4. Θ_{JA} - Junction to ambient.
5. Θ_{JB} - Junction to board.
6. Θ_{JC} - Junction to package case.

Figure 40 – 16-SOIC Package Outline

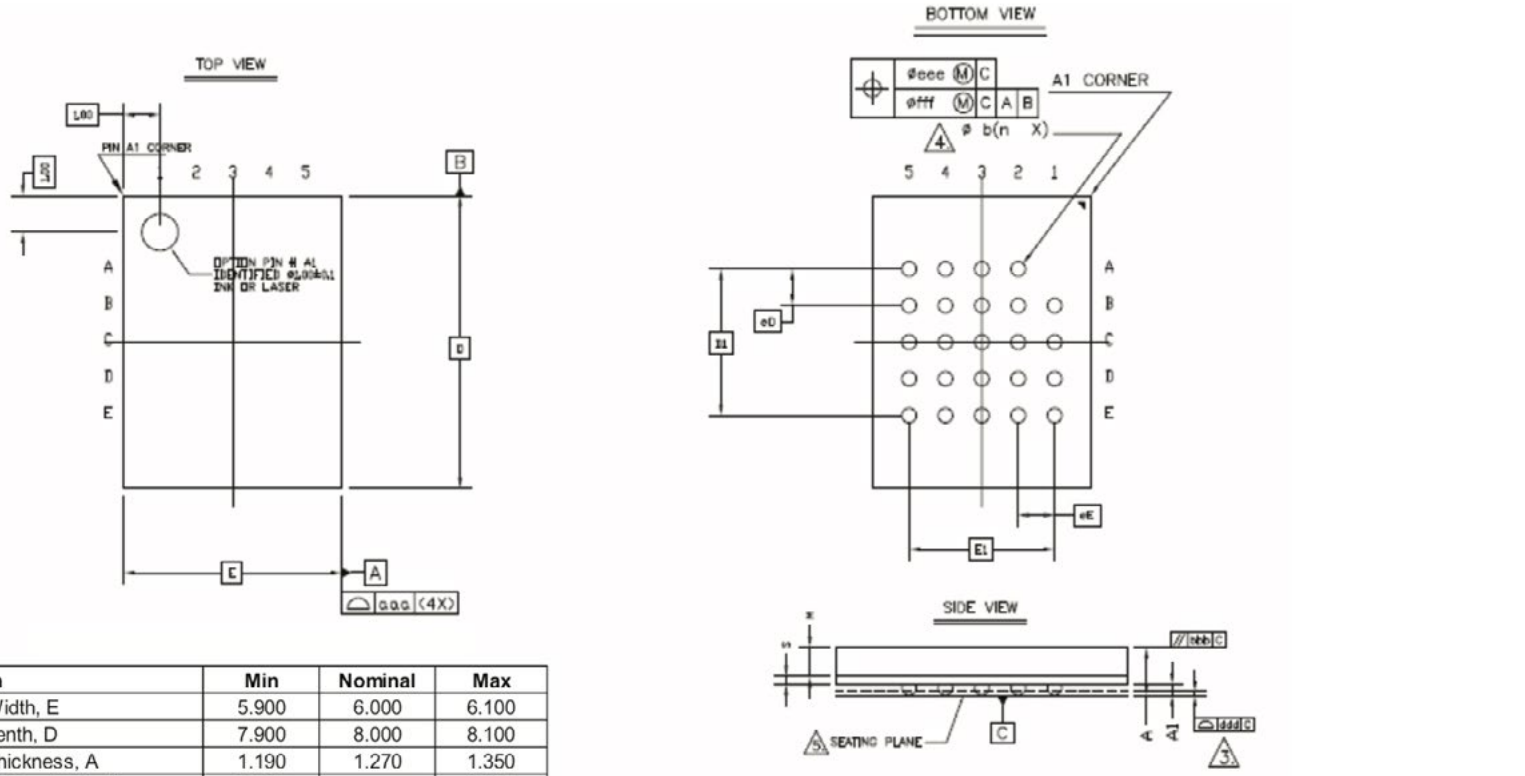


Dimensions next page.

16-SOIC Package Outline - Dimensions

Symbol	JEDEC MS - 013 (AA) issue (mm)			Everspin POD 16L SOIC PKG OUTLINE DWG. 300 MIL (mm)		
Ref	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	-	-	2.65	2.46	2.56	2.64
A1	0.10	-	0.30	0.127	0.22	0.29
A2	2.05	-	-	2.29	2.34	2.39
b	0.31	-	0.51	0.35	0.41	0.51
c	0.20	-	0.33	0.23	0.25	0.32
D	10.30 BSC			10.21	10.34	10.46
E	10.30 BSC			10.16	10.31	10.63
E1	7.50 BSC			7.44	7.52	7.59
L	0.40	-	1.27	0.61	0.81	1.02
L1	1.40 REF			N/A		
e	1.27 BSC			1.27 BSC		
Θ	0°	-	8°	0°	5°	8°

Figure 41 – 24 Ball BGA Package Outline



Dimension	Min	Nominal	Max
Package Width, E	5.900	6.000	6.100
Package Lenth, D	7.900	8.000	8.100
Package Thickness, A	1.190	1.270	1.350
Solder Ball Stand-Off, A1	0.220		0.320
Solder Ball Width, b	0.320		0.420
Solder Ball Diameter		0.350	
Solder Ball Pitch, eE		1.000	
Solder ball Pitch, eD		1.000	
package Edge Tolerance, aaa		0.100	
Mold Flatness, bbb		0.200	
Solder Ball Coplanarity, ddd		0.080	
Solder Offset (Package)		0.150	
Solder Offset (Ball)		0.080	
Edge Ball Center to Center, E1		4.000	
Edge Ball Center to Center, D1		4.000	
Ball Count, n		24	

Notes:	
1	Dimensions and tolerances per ASME Y14.5M - 1994.
2	Solder ball position designation per JESD 95-1, SPP-010.
3	This dimension includes stand-off height, packge body thickness and lid height, but does not include attached features, e.g. external heatsink or chip capacitors. An intergral heatslug is not considered an attached feature.
4	Dimension is measured at the maximum solder ball diameter, parallel to primary Datum C.
5	Primary Datum C and the seating plane are defined by the spherical crowns of the solder balls.
6	All dimensions are in millimeters.

REVISION HISTORY

Revision	Date	Description of Change
1.7	February 26, 2013	Initial Release Preliminary.
1.8	March 7, 2013	Revision to Table 5. Revision to $\overline{HOLD}$ timing Table 15. Corrected package illustration.
1.9	May 14, 2013	Added QPI Commands.
2.0	October 24, 2013	Removed QPI Commands, TDET and reference to XIP. These features will be released in a future product revision.
3.0	April 17, 2014	Major revision. Complete restructure of command section. Added QPI Mode, TDET, TDETX commands and XIP operating mode commands, instructions and timing diagrams. Removed Preliminary watermark from all pages. Removed Max and Typical values for V_{WIDD} and V_{WIDDQ}.
4.0	December 17, 2014	Added I_{SB1Q}, I_{SB2}, I_{SB2Q}, I_{DDQ} values. Revisions to Command Descriptions for FRQO and FRQAD. Revisions to Note 3 for Command Timing Diagrams for FRQO and FRQAD. Added package thermal resistance table. I_{DD} values in Table 8 have been updated.
4.1	March 20, 2015	Revised Table 23: ^{t}CS updated. ^{t}V (min) now unspecified. ^{t}HO (min) revised to 1.5ns.
4.2	May 19, 2015	Revised Everspin contact information.
4.3	June 11, 2015	Corrected Japan Sales Office telephone number.
5.0	August 12, 2015	Added 6x8mm 24-ball BGA package outline and dimensions.
5.1	January 26, 2017	Table 23: Revised ^{t}WHR = 11ns; ^{t}WLR = 12ns. 16-SOIC package options released to MP. 24-BGA now qualified.
5.2	February 1, 2017	Figures 35 and 36 - Synchronous Data Timing. Added timing detail for ^{t}V and ^{t}HO.
5.3	December 4, 2017	Figure 40 updated with new dimensions
5.4	January 26, 2018	Added extended temperature range to the data sheet.
5.5	March 15, 2018	Added extended range to Table 17
5.6	June 1, 2018	Updated table 24

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