QPV750
QPV750L
QPV750B
QPV750BL

December 17, 2010

QPV750, QPV750L, QPV750B & QPV750BL
High Density UV Erasable Programmable Logic Devices

General Description

The QPV750(L) and QPV750B(L) are High Density UV Erasable Programmable Logic Devices (PLDs). e2v aerospace and defense designed the QPV750(L) and QPV750B(L) to be direct replacements for the ATV750/L and ATV750B/L. They are designed to be used for a wide variety of programmable logic designs and as a high-density replacement for discrete logic.

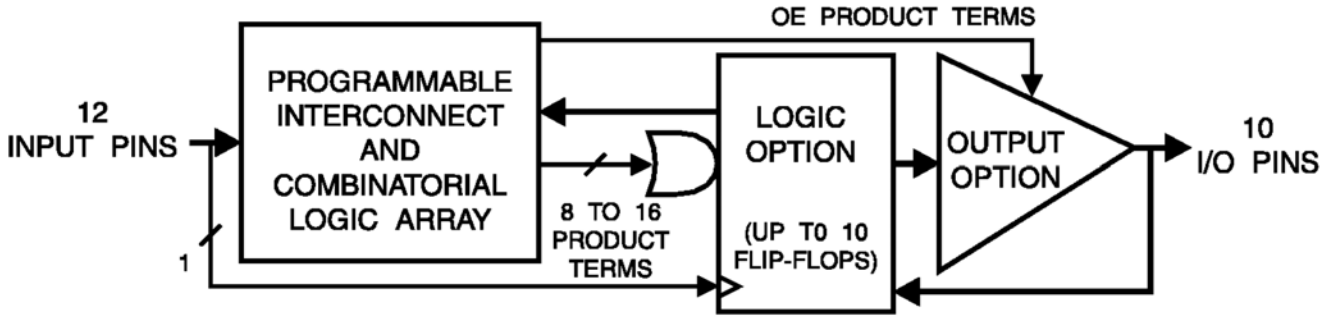
The QPV750(L) and QPV750B(L) support increased logic flexibility, with up to 42 array inputs, 20 sum terms, and 20 flip-flops. In addition, the QPV750(L) and QPV750B(L) offer enhanced output logic flexibility with all 20 flip-flops able to feed back internally and 10 of the flip-flops available as direct outputs.

The QPV750(L) and QPV750B(L) are available in hermetic 24-pin ceramic DIP and 28-pin ceramic LCC packages. Military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

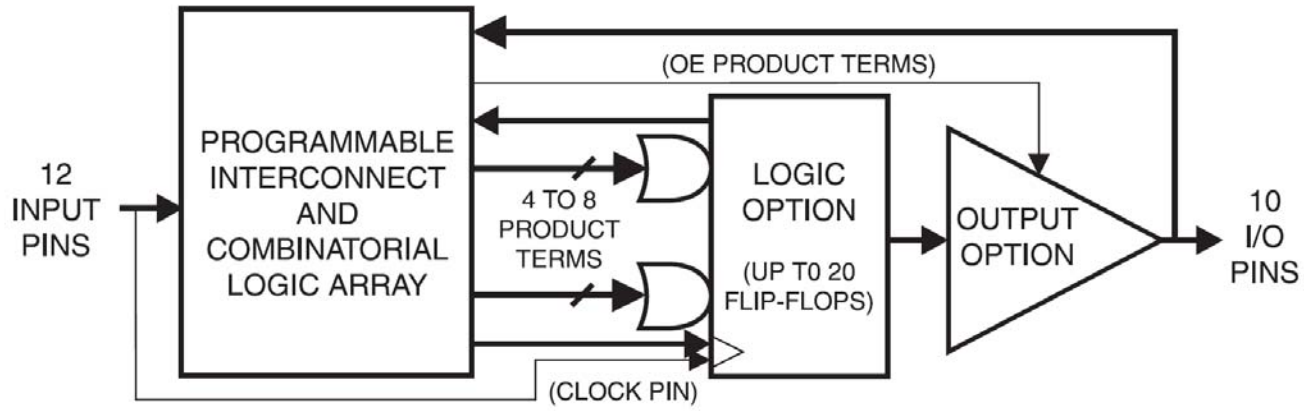
Features

- Advanced, high-speed programmable logic structure – superset of the 22V10
  - Pin-to-pin delay as low as 10ns
- Increased logic flexibility
  - Up to 42 inputs, 20 sum terms, and 20 flip-flops
- Enhanced output logic flexibility
  - All 20 flip-flops feed back internally
  - Up to 10 flip-flops available as outputs
- New flip-flop features (QPV750B only)
  - D- or T-type
  - Product term or direct input pin clocking
- Low-Power versions for critical applications (QPV750L and QPV750BL)
  - Standby current as low as 5mA typical
- Multiple feedback paths provide for buried state machines and I/O bus capability
- Fully reprogrammable
  - Fully tested and guaranteed for 100% programmability
- Multiple package options
  - 24-pin ceramic DIP
  - 28-pin ceramic LCC
- Available as SMD# 5962-88726

Logic Diagram – QPV750(L)



Logic Diagram – QPV750B(L)



Functional Description

The QPV750(L) and QPV750B(L) High Density UV Erasable PLDs offer flexible functionality with many advanced options. Ten of the QPV750(L) and QPV750B(L) pins are flexible and can be used as inputs, outputs or bi-directional I/O pins. The other 12 pins are usable as dedicated input pins.

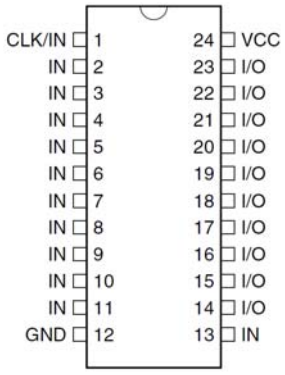
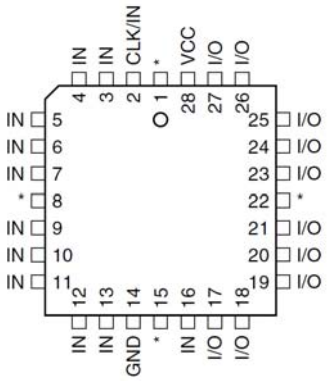
In the QPV750B(L) only, the flip-flops can be configured as either D-type or T-type. Each flip-flop output is fed back into the array independently, allowing the burying of all the sum terms and flip-flops.

There are 171 total product terms available. A variable format is used to assign between four to eight product terms per sum term. There are two sum terms per output, providing added flexibility. With 20 sum terms and flip-flops, complex state machines can be implemented while providing room for additional logic functionality.

Product terms provide individual clocks and asynchronous resets for each flip-flop. Each flip-flop may also be individually configured to have direct input pin controlled clocking. Each output has its own enable product term. One product term provides a common synchronous preset for all flip-flops. Register preload functions are provided to simplify testing. All registers automatically reset upon power-up.

The QPV750 devices have a maximum operating supply current of 140mA and input-to-output (t_{PD}) performance ranging from 40 ns to as low as 20ns. The QPV750B devices offer faster performance with t_{PD} as 10ns with a maximum operating and standby supply current of 100mA. For low power applications, the QPV750L and QPV750BL offer a maximum operating supply current of 50mA and a maximum standby supply current of only 15 mA.

Connection Diagrams

Pin Configurations		CERDIP	LCC
Pin Name	Function		
CLK	Clock		
GND	Ground		
IN	Logic Inputs		
I/O	Bidirectional Buffers		
*	No Internal Connection		
V_{CC}	+5V Supply		

Absolute Maximum Ratings

Stresses above the AMR may cause permanent damage; extended operation at AMR may degrade performance and affect reliability

Condition		Units	Notes
Power Supply and Output Voltage	-0.5 to +7.0	Volts DC	/1
Input Voltage	- 2.0 to +7.0	Volts DC	/1
Output Voltage	-0.5 to +7.0	Volts DC	
Programming Voltage and Voltage on Input Pins during Programming	- 2.0 to +14.0	Volts DC	/1
Output Sink Current	16	mA	
Maximum Power Dissipation	1.2	W	/2
Storage Temperature Range	-65 to +150	ºC	
Temperature under Bias	-55 to +125	ºC	
Junction Temperature (T_J)	+175	ºC	
Lead Temperature (soldering, 10 sec., max)	+300	ºC	
Integrated UV Erase Dose	7258	W-sec / cm^2	

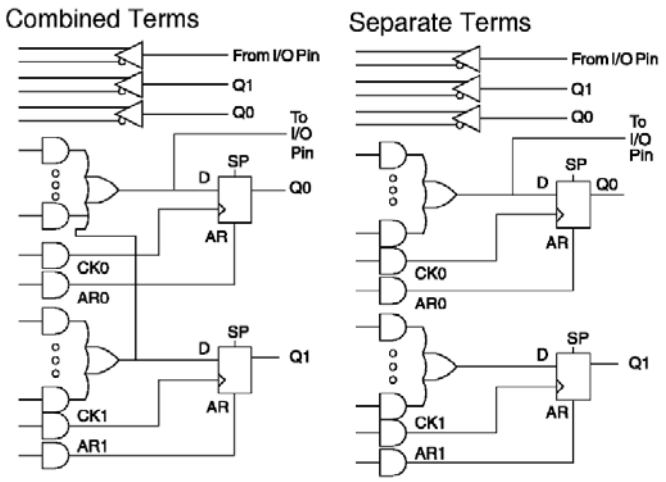
/1 Minimum voltage is -0.6V DC, which may undershoot to -2.0V DC for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to +7.0V DC for pulses of less than 20 ns.
/2 – Must withstand the added P_D due to short circuit test, e.g. loss.

Recommended Operating Conditions

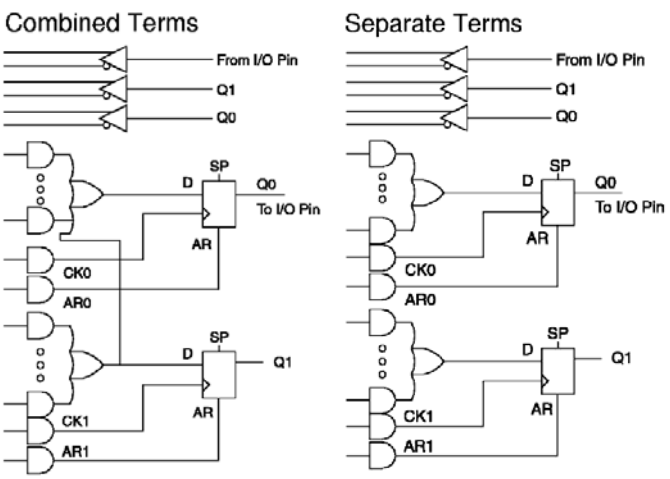
Condition		Units	Notes
Operating Temperature	-55 to +125	ºC	
Supply Voltage Range (V_{CC})	4.5 to 5.5	Volts DC	
Minimum High-Level Input Voltage (V_{IH})	2.0	Volts DC	
Maximum Low-Level Input Voltage (V_{IL})	0.8	Volts DC	

Logic Options – QPV750(L)

Combinatorial Output

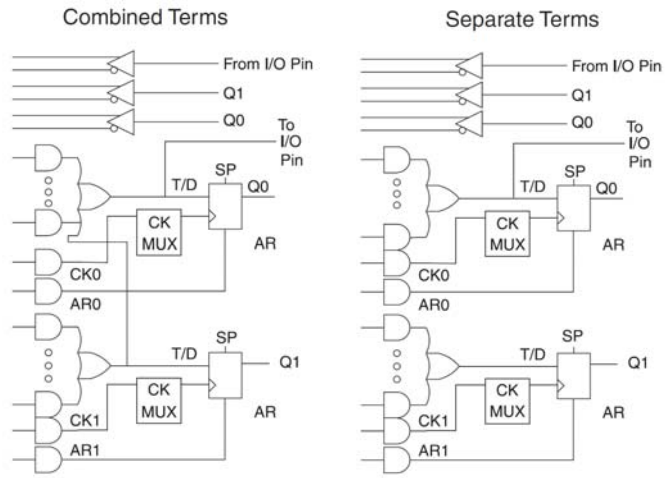


Registered Output

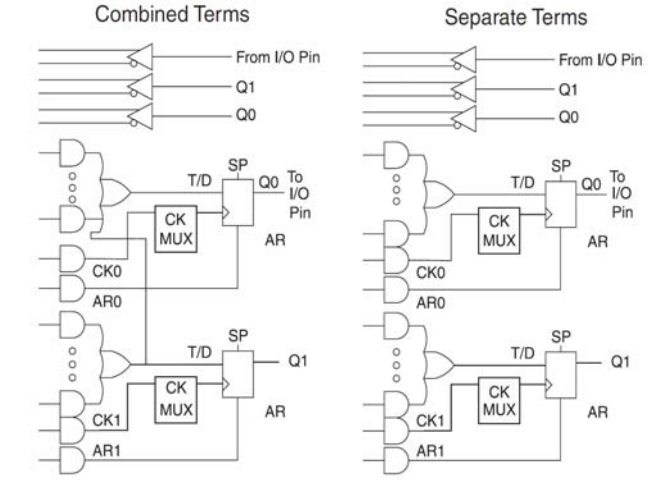


Logic Options – QPV750B(L)

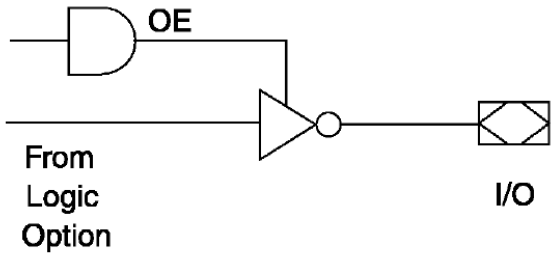
Combinatorial Output

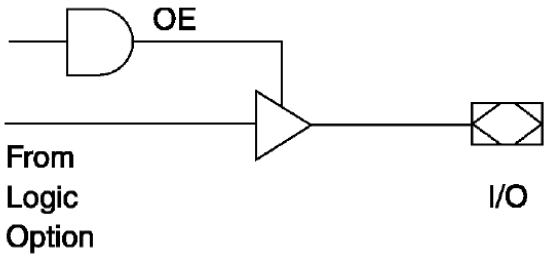


Registered Output

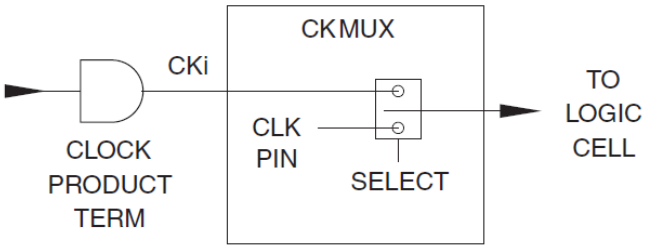


Output Options – QPV750(L) and QPV750B(L)





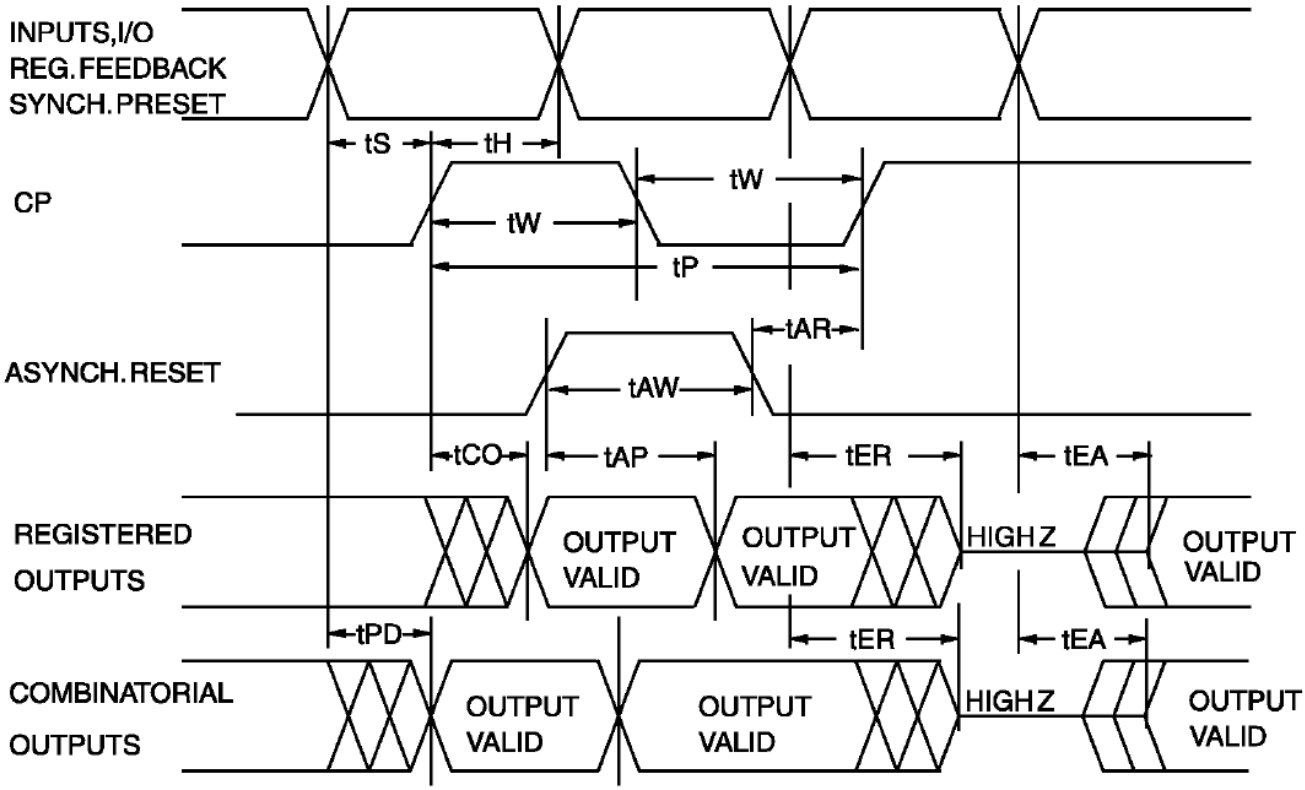
Clock Mux – QPV750B(L) Only



Unprogrammed Truth Table

Pins	Number	State	Description
Input-Only Pins	10	X	Don't care
Bidirectional I/O Pins	12	High Z	Three-state

AC Waveforms – Product Term Clock, QPV750(L) and QPV750B(L) (Refer to Table I)



Note: Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions[1] 4.5V ≤ V_{CC} ≤ 5.5V -55ºC ≤ T_A ≤+125ºC Unless Otherwise Specified	Device Types	Min	Max	Unit
Output High Voltage	V_{OH}	I_{OH}= -4.0mA	All	2.4		V
Output Low Voltage	V_{OL}	I_{OH}= 8.0mA	QPV750(L)		0.5	V
		I_{OH}= 12.0mA	QPV750B(L)			
Output Leakage Current[2] (High Impedance)	I_{OZ}	V_{CC} = 5.5V, V_O = 5.5V Vo = GND	All	-10	10	µA
Input High Current	I_{IH}	V_{IH} = 5.5V	All		10	µA
		V_{IH} = 2.4V	All		10	
Input Low Current	I_{IL}	V_{IL} = 0.4V	All		-10	µA
		V_{IL} = GND	All		-10	
Operating Supply Current	I_{CC1}	V_{CC} = 5.5V, f = 1MHz Outputs open V_{IN} = V_{CC} or GND	QPV750		100	mA
			QPV750L		50	
			QPV750B		100	
			QPV750BL		50	
Standby Supply Current	I_{CC2}	V_{CC} = 5.5V V_{IN} = GND Outputs open	QPV750		100	mA
			QPV750L		15	
			QPV750B		100	
			QPV750BL		15	
Output Short Circuit Current[4]	I_{OS}	V_{CC} = 5.5V	All	-30	120	mA
Input Capacitance[5]	C_I	V_I = 0V, V_{CC} = 5.0V, T_A = 25°C, f = 1MHz	All		20	pF
Output Capacitance[5]	C_O	V_I = 0V, V_{CC} = 5.0V, T_A = 25°C, f = 1MHz	All		15	pF

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS (cont.)

Test	Symbol	Conditions[1] 4.5V ≤ V_{CC} ≤ 5.5V -55ºC ≤ T_A ≤+125ºC Unless Otherwise Specified	Device Types	Min	Max	Unit
Input or Feedback to Non-registered Output	t_{PD}	V_{CC} = 4.5V C_L = 50pF	QPV750-40		40	ns
			QPV750-35		35	
			QPV750L-30		30	
			QPV750-25 QPV750L-25 QPV750B-25 QPV750BL-25		25	
			QPV750-20		20	
			QPV750B-15 QPV750BL-15		15	
			QPV750B-10		10	
Clock to Output	t_{CO}	V_{CC} = 4.5V C_L = 50pF	QPV750-40		35	ns
			QPV750-35 QPV750L-30		30	
			QPV750-25 QPV750L-25 QPV750B-25 QPV750BL-25		22	
			QPV750-20		20	
			QPV750B-15 QPV750BL-15		14	
			QPV750B-10		10	
Input to Output Enable and Input to Output Disable	t_{EA} & t_{ER}	V_{CC} = 4.5V C_L = 5pF	QPV750-40		40	ns
			QPV750-35 QPV750L-30		35	
			QPV750-25 QPV750L-25 QPV750B-25 QPV750BL-25		25	
			QPV750-20		20	
			QPV750B-15 QPV750BL-15		15	
			QPV750B-10		10	

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS (cont.)

Test	Symbol	Conditions[1] 4.5V ≤ V_{CC} ≤ 5.5V -55ºC ≤ T_A ≤+125ºC Unless Otherwise Specified	Device Types	Min	Max	Unit
Clock Period	t_P	V_{CC} = 4.5V C_L = 5pF	QPV750-40	35		ns
			QPV750-35 QPV750L-30	30		
			QPV750-25 QPV750L-25	22		
			QPV750-20	18		
			QPV750B-25 QPV750BL-25	17		
			QPV750B-15 QPV750BL-15	14		
			QPV750B-10	11		
Clock Pulse Width[5]	t_{CL}	V_{CC} = 4.5V C_L = 50pF	QPV750-40	17		ns
			QPV750-35 QPV750L-30	15		
			QPV750-25 QPV750L-25	10		
			QPV750B-25 QPV750BL-25	8.5		
			QPV750-20	8		
			QPV750B-15 QPV750BL-15	7		
			QPV750B-10	5.5		
Clock to Feedback[6]	t_{CF}	V_{CC} = 4.5V C_L = 50pF	QPV750-40	15		ns
			QPV750-35 QPV750L-30	12		
			QPV750-25 QPV750-20 QPV750L-25 QPV750B-25 QPV750BL-25	10		
			QPV750B-15 QPV750BL-15	9		
			QPV750B-10	7.5		

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS (cont.)

Test	Symbol	Conditions[1] 4.5V ≤ V_{CC} ≤ 5.5V -55ºC ≤ T_A ≤+125ºC Unless Otherwise Specified	Device Types	Min	Max	Unit
Input Setup Time[5]	t_s	V_{CC} = 4.5V C_L = 50pF	QPV750-40	20		ns
			QPV750-35 QPV750L-30	18		
			QPV750-25 QPV750L-25 QPV750B-25 QPV750BL-25	12		
			QPV750-20 QPV750BL-15	10		
			QPV750B-15	8		
			QPV750B-10	4		
Hold Time[5]	t_H	V_{CC} = 4.5V C_L = 50pF	QPV750-40	15		ns
			QPV750-35 QPV750L-30	10		
			QPV750BL-25 QPV750BL-15	7		
			QPV750-25 QPV750-20 QPV750L-25 QPV750B-25 QPV750B-15	5		
			QPV750B-10	2		
Maximum Clock Frequency[5]	f_{MAX}	V_{CC} = 4.5V C_L = 50pF	QPV750-40	28		MHz
			QPV750B-25 QPV750BL-25	29		
			QPV750-35 QPV750L-30	33		
			QPV750BL-15	41		
			QPV750-25 QPV750L-25 QPV750B-15	45		
			QPV750-20	55		
			QPV750B-10	71		

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS (cont.)

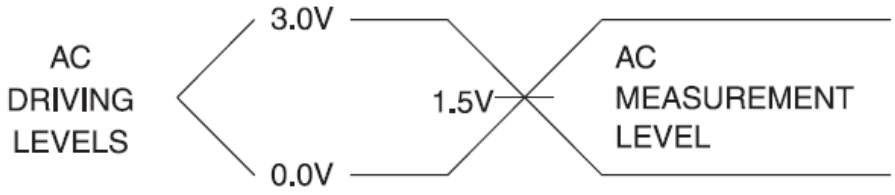
Test	Symbol	Conditions[1] $4.5V \le V_{CC} \le 5.5V$ $-55ºC \le T_A \le +125ºC$ Unless Otherwise Specified	Device Types	Min	Max	Unit
Asynchronous Reset Pulse Width and Asynchronous Reset Recovery Time	t_{AW} & t_{AR}	$V_{CC} = 4.5V$ $C_L = 50pF$	QPV750-40	40		ns
			QPV750-35 QPV750L-30	35		
			QPV750-25 QPV750L-25 QPV750B-25 QPV750BL-25	20		
			QPV750-20 QPV750B-15 QPV750BL-15	15		
			QPV750B-10	10		
Feedback Setup Time	t_{SF}	$V_{CC} = 4.5V$ $C_L = 50pF$	QPV750-40, QPV750-35	18		ns
			QPV750L-30	15		
			QPV750-25 QPV750L-25 QPV750B-25 QP750BL-25 QPV750B-15 QPV750BL-15	7		
			QPV750-20	5		
			QPV750B-10	4		
Asynchronous Reset to Registered Output Reset	t_{AP}	$V_{CC} = 4.5V$ $C_L = 50pF$	QPV750-40		40	ns
			QPV750-35 QPV750L-30		35	
			QPV750-25 QPV750L-25 QPV750B-25 QPV750BL-25		25	
			QPV750-20		20	
			QPV750B-15 QPV750BL-15		15	
			QPV750B-10		12	

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS (cont.)

Test	Symbol	Conditions[1] $4.5V \le V_{CC} \le 5.5V$ $-55ºC \le T_A \le +125ºC$ Unless Otherwise Specified	Device Types	Min	Max	Unit
Setup Time, Synchronous Preset Product Term Clock	t_{SP}	$V_{CC} = 4.5V$ $C_L = 50pF$	QPV750-40, QPV750-35	18		ns
			QPV750-25 QPV750L-30 QPV750L-25 QPV750B-25 QPV750BL-25	15		
			QPV750-20	12		
			QPV750B-15 QPV750BL-15	8		
			QPV750B-10	7		

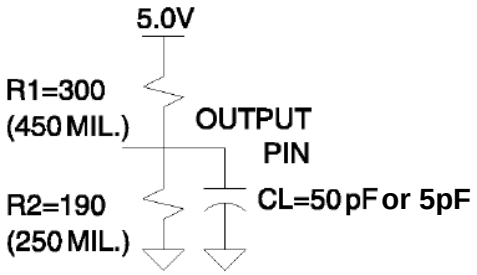
Notes:
1. All voltages are referenced to ground.
2. I/O terminal leakage is the worst case of I_{IX} or I_{OZ}.
3. I_{CC} for typical functional pattern 5mA/MHz for devices 10-12, worst case based on initial characterization.
4. Only one output shorted at a time.
5. Tested only initially and after any design changes. Test applies only to register outputs.
6. Values guaranteed by design and are not tested.

Input Test Waveforms and Measurement Levels

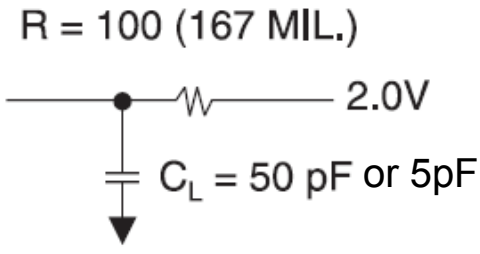


Note: t_R, t_F < 5ns (10% to 90%) for the QPV750. t_R, t_F < 3ns (10% to 90%) for the QPV750B.

Output Test Loads



QPV750(L)



QPV750B(L)

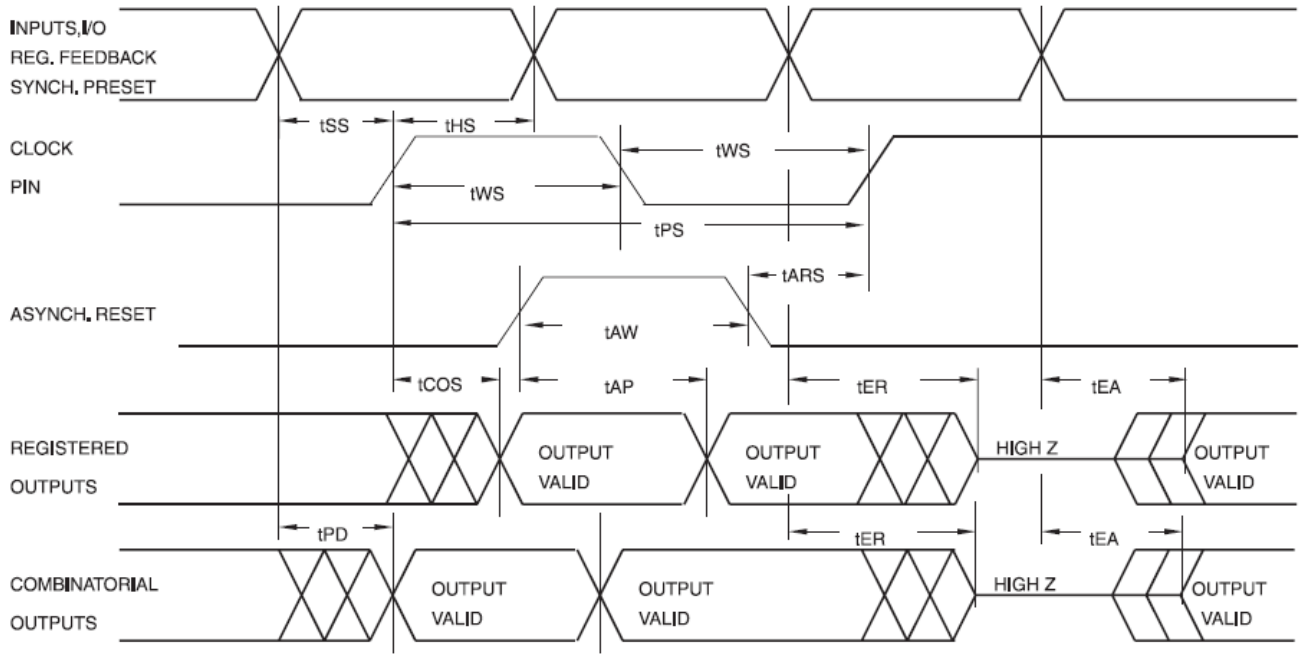
TABLE II – INPUT PIN CLOCK PERFORMANCE CHARACTERISTICS – QPV750B(L) ONLY

Test	Symbol	Conditions 4.5V ≤ V_{CC} ≤ 5.5V -55ºC ≤ T_A ≤+125ºC Unless Otherwise Specified	Device Types	Min	Max	Unit
Clock Period, Input Pin Clock	t_{PS}	V_{CC} = 4.5V C_L = 50pF	QPV750B-25 QPV750BL-25	16		ns
			QPV750B-15 QPV750BL-15	12		
			QPV750B-10	10		
Clock Pulse Width, Input Pin Clock	t_{WS}	V_{CC} = 4.5V C_L = 50pF	QPV750B-25 QPV750BL-25	8		ns
			QPV750B-15 QPV750BL-15	6		
			QPV750B-10	5		
Clock to Feedback, Input Pin Clock	t_{CFS}	V_{CC} = 4.5V C_L = 50pF	QPV750B-25 QPV750BL-25		7	ns
			QPV750B-15 QPV750BL-15		5.5	
			QPV750B-10		5	
Input Setup Time, Input Pin Clock	t_{SS}	V_{CC} = 4.5V C_L = 50pF	QPV750BL-25	12		ns
			QPV750BL-15	10		
			QPV750B-25	9		
			QPV750B-15	8		
			QPV750B-10	6.5		
Hold Time, Input Pin Clock	t_{HS}	V_{CC} = 4.5V C_L = 50pF	QPV750B-All QPV750BL-All	0		ns
Maximum Clock Frequency, Input Pin Clock	f_{MAXS}	V_{CC} = 4.5V C_L = 50pF	QPV750BL-25		37	MHz
			QPV750B-25		41	
			QPV750BL-15		52	
			QPV750B-15		58	
			QPV750B-10		74	
Asynchronous Reset Recovery Time, Input Pin Clock	t_{ARS}	V_{CC} = 4.5V C_L = 50pF	QPV750B-25 QPV750BL-25	25		ns
			QPV750B-15 QPV750BL-15	15		
			QPV750B-10	10		

TABLE II – INPUT PIN CLOCK PERFORMANCE CHARACTERISTICS – QPV750B ONLY (cont.)

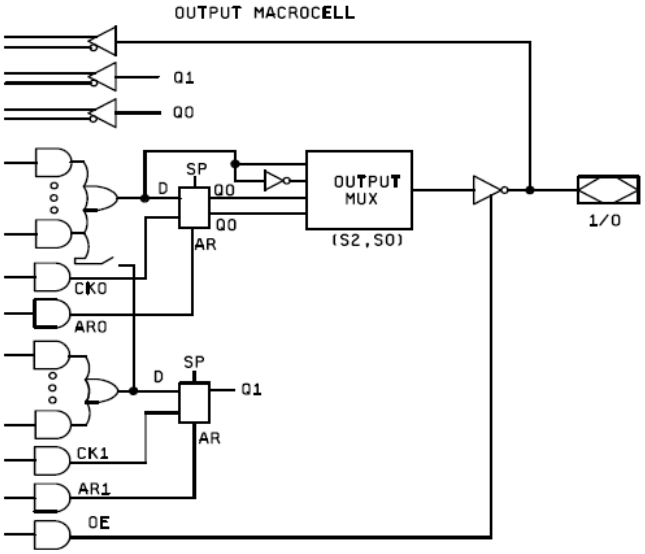
Test	Symbol	Conditions 4.5V ≤ V_{CC} ≤ 5.5V -55ºC ≤ T_A ≤+125ºC Unless Otherwise Specified	Device Types	Min	Max	Unit
Clock to Output, Input Pin Clock	t_{COS}	V_{CC} = 4.5V C_L = 50pF	QPV750B-25 QPV750BL-25	0	15	ns
			QPV750B-15 QPV750BL-15	0	9	
			QPV750B-10	0	7	
Feedback Setup Time, Input Pin Clock	t_{SFS}	V_{CC} = 4.5V C_L = 50pF	QPV750B-25 QPV750BL-25	9		ns
			QPV750B-15 QPV750BL-15	7		
			QPV750B-10	6.5		
Setup Time, Synchronous Preset, Input Pin Clock	t_{SPS}	V_{CC} = 4.5V C_L = 50pF	QPV750B-25 QPV750BL-25	15		ns
			QPV750B-15 QPV750BL-15	11		
			QPV750B-10	5		

AC Waveforms – Input Pin Clock – QPV750B(L) Only (Refer to Table II)

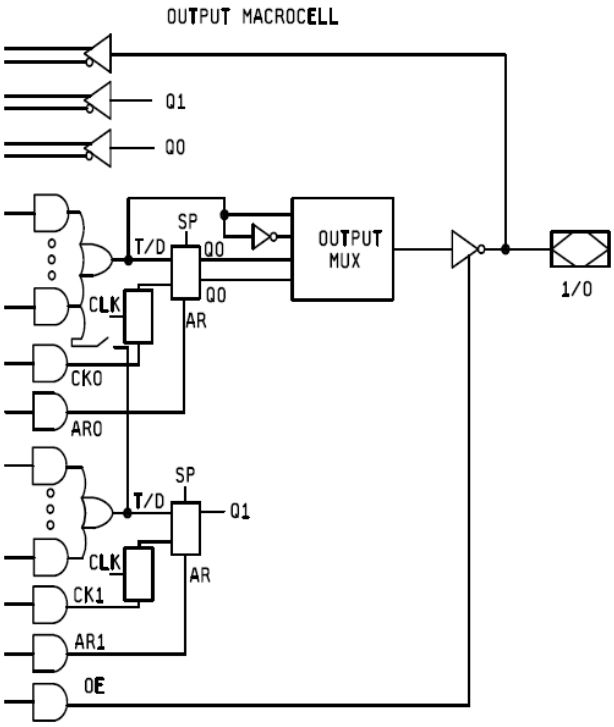


Note: Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

Output Macrocells



QPV750(L)

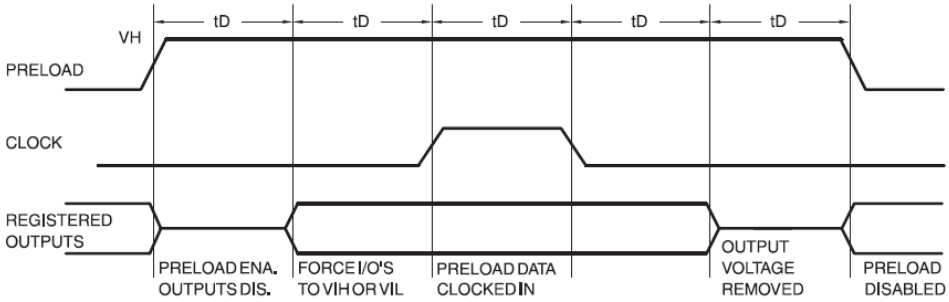


QPV750B(L)

QP750(L) Output Configurations			
S2	**S1**	**S0**	**Output Configuration**
0	0	0	Active low, combined terms, registered
0	0	1	Active low, combined terms, combinatorial
0	1	0	Active low, separate terms, registered
0	1	1	Active low, separate terms, combinatorial
1	0	0	Active high, combined terms, registered
1	0	1	Active high, combined terms, combinatorial
1	1	0	Active high, separate terms, registered
1	1	1	Active high, separate terms, combinatorial

Preload of Registered Outputs

The registers in the QPV750(L) and QPV750B(L) are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low; independent of the output polarity. The preload state is entered by placing a 10.25V to 10.75V signal on pin 8 on the DIP, and pin 10 on the LCC. When the clock term is pulsed high, the data on the I/O pin is placed into the register chosen by the Select Pin.

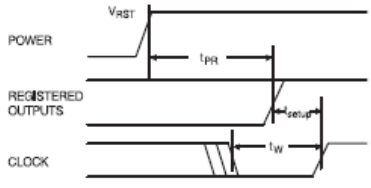


Level Forced on Registered Output Pin during PRELOAD Cycle	Select Pin State	Register State after Cycle Register #0	Register State after Cycle Register #1
V_{IH}	Low	High	X
V_{IL}	Low	Low	X
V_{IH}	High	X	High
V_{IL}	High	X	Low

Power-Up Reset

The registers in the QPV750(L) and QPV750B(L) are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer. This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required.

1. The V_{CC} rise must be monotonic
2. After reset occurs, all input and feedback setup times must be met before driving the clock term high
3. The signals from which the clock is derived must remain stable during t_{PR}



Parameter	Description	Typ	Max	Units
t_{PR}	Power-up Reset Time	600	1,000	ns
V_{RST}	Power-up Reset Voltage	3.8	4.5	V

Advanced Features

The QPV750(L) and QPV750B(L) offer advanced features beyond the standard 22V10 architecture.

Advanced Features – QPV750(L) and QPV750B(L)

Asynchronous Clocks

Each of the flip-flops in the QPV750(L) and QPV750B(L) has a dedicated product term driving the clock. The user is no longer constrained to using one clock for all the registers. Buried state machines, counters, and registers can all coexist in one device, while running on separate clocks. The QPV750(L) and QPV750B(L) clock period matches that of similar synchronous devices.

A Full Bank of 10 More Registers

The QPV750(L) and QPV750B(L) provide two flip-flops per output logic cell for a total of 20. Each register has its own sum term, its own reset term and its own clock term.

Independent I/O Pin and Feedback Paths

Each I/O pin on the QPV750(L) and QPV750B(L) has a dedicated input path. Each of the 20 registers has its own feedback terms into the array as well. This feature combined with individual product terms for each I/O's output enable, facilitates true bi-directional I/O design.

Combinable Sum Terms

Each output macrocell's two sum terms can be combined in an OR gate before the output or the register. This provides up to 16 product terms per output or flip-flop, increasing the number of usable gates available.

Advanced Features – QPV750B(L) only

Selectable D- and T-type Registers

Each QPV750B(L) flip-flop can be individually configured as either D- or T-type. Using the T-type configuration, JK and SR flip-flops are also easily created. These options allow more efficient product term usage.

Selectable Asynchronous Clocks

Each of the QPV750B(L) flip-flops may be clocked by its own clock product term or directly from Pin 1 (SMD Lead 2). This removes the constraint that all registers must use the same clock. Buried state machines, counters and registers can all coexist in one device while running on separate clocks. Individual flip-flop clock source selection further allows mixing higher performance pin clocking and flexible product term clocking within one design.

Programming Software Support

Software capable of transforming Boolean equations, state machine descriptions and truth tables into JEDEC files for the QPV750(L) and QPV750B(L) is available from several PLD software vendors. The QPV750(L) programming algorithm is different from the QPV750B(L) algorithm. Choose the appropriate device in your programmer menu to ensure proper programming.

If needed, the QPV750B(L) may be programmed to perform the QPV750(L) functional subset (no T-type flip-flops or pin clocking) using the QPV750(L) JEDEC file. In this case, the QPV750B(L) becomes a direct replacement or speed upgrade for the QPV750(L).

Synchronous Preset and Asynchronous Reset

One synchronous preset line is provided for all 20 registers in the QPV750(L) and QPV750B(L). The appropriate input signals to cause the internal clocks to go to a high state must be received during a synchronous preset. Appropriate setup and hold times must be met, as shown in the switching waveform diagram. An individual asynchronous reset line is provided for each of the 20 flip-flops. Both master and slave halves of the flip-flops are reset when the input signals received force the internal resets high.

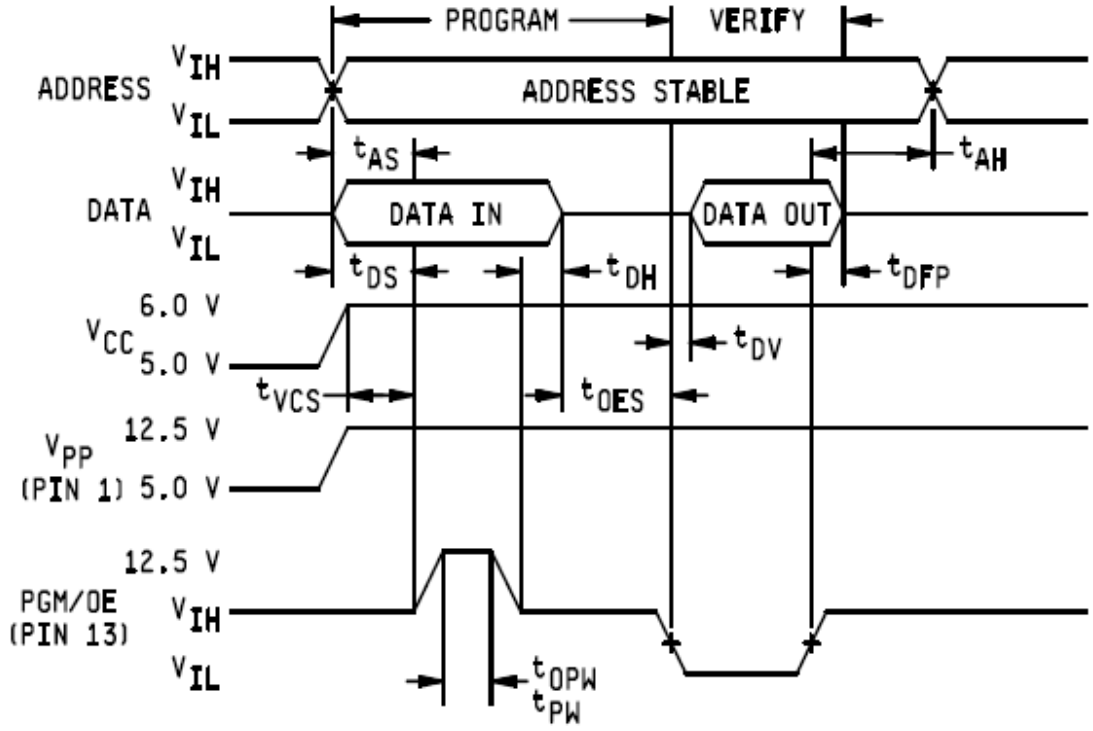
Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the QPV750(L) and QPV750B(L) fuse patterns. Once the security fuse is programmed, all fuses will appear programmed during verify. The security fuse should be programmed last, as its effect is immediate.

Erasure Characteristics

The entire memory array of a QPV750(L) and QPV750B(L) is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 μW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W-sec/ cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any QPV750(L) or QPV750B(L) which will be subjected to continuous fluorescent indoor lighting or sunlight.

Programming Waveform (Refer to Table III)



Programming Characteristics

TABLE III – PROGRAMMING CHARACTERIISTICS

Test	Symbol	Conditions[1] Ta = +25°C ± 5°C V_{CC} = 6.0V ± 0.25V V_{PP} = 12.5V ± 0.5V	Device Types	Min	Max	Unit
Input Current (all Inputs)	I_{LI}	$V_{IN} = V_{IL}$ or V_{IH}	All		10	µA
Input Low Level (All Inputs)	V_{IL}		All	-0.6	0.8	V
Input High Level	V_{IH}		All	2.0	V_{CC}+0.75	V
Output Low Voltage during Verify	V_{OL}	I_{OL} = 16 mA	All		0.5	V
Output High Voltage during Verify	V_{OH}	I_{OL} = -4.0 mA	All	2.4		V
V_{CC} Supply Current	I_{CC2}		QPV750(L)		140	mA
			QPV750B(L)		190	mA
V_{PP} Supply Current (Programming)	I_{PP2}	V_{PP} pin = V_{PP}	All		30	mA
Address Setup Time	t_{AS}		All	2		µs
Output Enable Setup Time	t_{OES}		All	2		µs
Data Setup Time	t_{DS}		All	2		µs
Address Hold Time	t_{AH}		All	0		µs
Data Hold Time	t_{DH}		All	2		µs
Output Enable to Output Float Delay[2]	t_{DFP}		All	0	130	ns
V_{CC} = Setup Time	t_{VCS}		All	2		µs
PGM Initial Program Pulse Width[3]	t_{PW}		All	0.02		ms
PGM Overprogram Pulse Width[4]	t_{OPW}		All	0.02		ms
Data Valid from Output Enable	t_{DV}		All		70	ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output float is defined as the point where data is no longer driven.
3. Initial program pulse width tolerance is 1 ms ±5 percent.
4. The length of the overprogram pulse may vary from 18 ms to 225 ms as a function of the iteration counter value X.

Ordering Information

GDIP3-T24 (Ceramic Dip)			
Device Type	DSCC SMD#	Part Number	Propagation Delay
QPV750	5962-8872601LA	QPV750-40DM/883	40 ns
	5962-8872602LA	QPV750-35DM/883	35 ns
	5962-8872603LA	QPV750-25DM/883	25 ns
	5962-8872604LA	QPV750-20DM/883	20 ns
QPV750L	5962-8872606LA	QPV750L-30DM/883	30 ns
	5962-8872607LA	QPV750L-25DM/883	25 ns
QPV750B	5962-8872610LA	QPV750B-25DM/883	25 ns
	5962-8872609LA	QPV750B-15DM/883	15 ns
	5962-8872608LA	QPV750B-10DM/883	10 ns
QPV750BL	5962-8872612LA	QPV750BL-25DM/883	25 ns
	5962-8872611LA	QPV750BL-15DM/883	15 ns

CQCC13-N28 (Ceramic LCC)			
Device Type	DSCC SMD#	Part Number	Propagation Delay
QPV750	5962-88726013A	QPV750-40LM/883	40 ns
	5962-88726023A	QPV750-35LM/883	35 ns
	5962-88726033A	QPV750-25LM/883	25 ns
	5962-88726043A	QPV750-20LM/883	20 ns
QPV750L	5962-88726063A	QPV750L-30LM/883	30 ns
	5962-88726073A	QPV750L-25LM/883	25 ns
QPV750B	5962-88726103A	QPV750B-25LM/883	25 ns
	5962-88726093A	QPV750B-15LM/883	15 ns
	5962-88726083A	QPV750B-10LM/883	10 ns
QPV750BL	5962-88726123A	QPV750BL-25LM/883	25 ns
	5962-88726113A	QPV750BL-15LM/883	15 ns

e2v aerospace and defense supports Source Control Drawing (SCD) and custom package development for this product family.

Notes:

Package outline information and specifications are defined by Mil-Std-1835 package dimension requirements.

“M/883” products manufactured by e2v aerospace and defense are compliant to the assembly, burn-in, test and quality conformance requirements of Test Methods 5004 & 5005 of Mil-Std-883 for Class B devices. This datasheet defines the electrical test requirements for the device(s).

The listed drawings, Mil-PRF-38535, Mil-Std-883 and Mil-Std-1835 are available online at http://www.dscc.dla.mil/

Additional information is available at our website http://www.e2v.com/qp