EV12AS200GS
12-bit 1.5 Gsps ADC

Datasheet - *Preliminary*

Main Features

- Single Core ADC Architecture with 12-bit Resolution Integrating a Selectable 1:1 and 1:2 DEMUX
- 1.5 GSps Guaranteed Conversion Rate
- Differential Input Clock (AC Coupled)
- 500 mVpp Analogue Input Voltage (Differential Full Scale and AC Coupled)
- Analogue and Clock Input Impedance: 100Ω Differential
- LVDS Differential Output Data
- 3 Wires Serial Interface (3WSI) Digital Interface (Write Only) with Reset Signal
- ADC Gain, Offset, Sampling Delay for Interleaving Control
- No Missing Codes at 1.5 GSps 1st and 2nd Nyquist
- Low Latency (< 5 Clock Cycles)
- Test Modes
- Data Ready Common to the 2 Output Ports
- Power Supply : 5.2V, 3.3V and 2.5V (Output Buffers)
- Power Dissipation : 3.2W
- CI CGA 255 Package

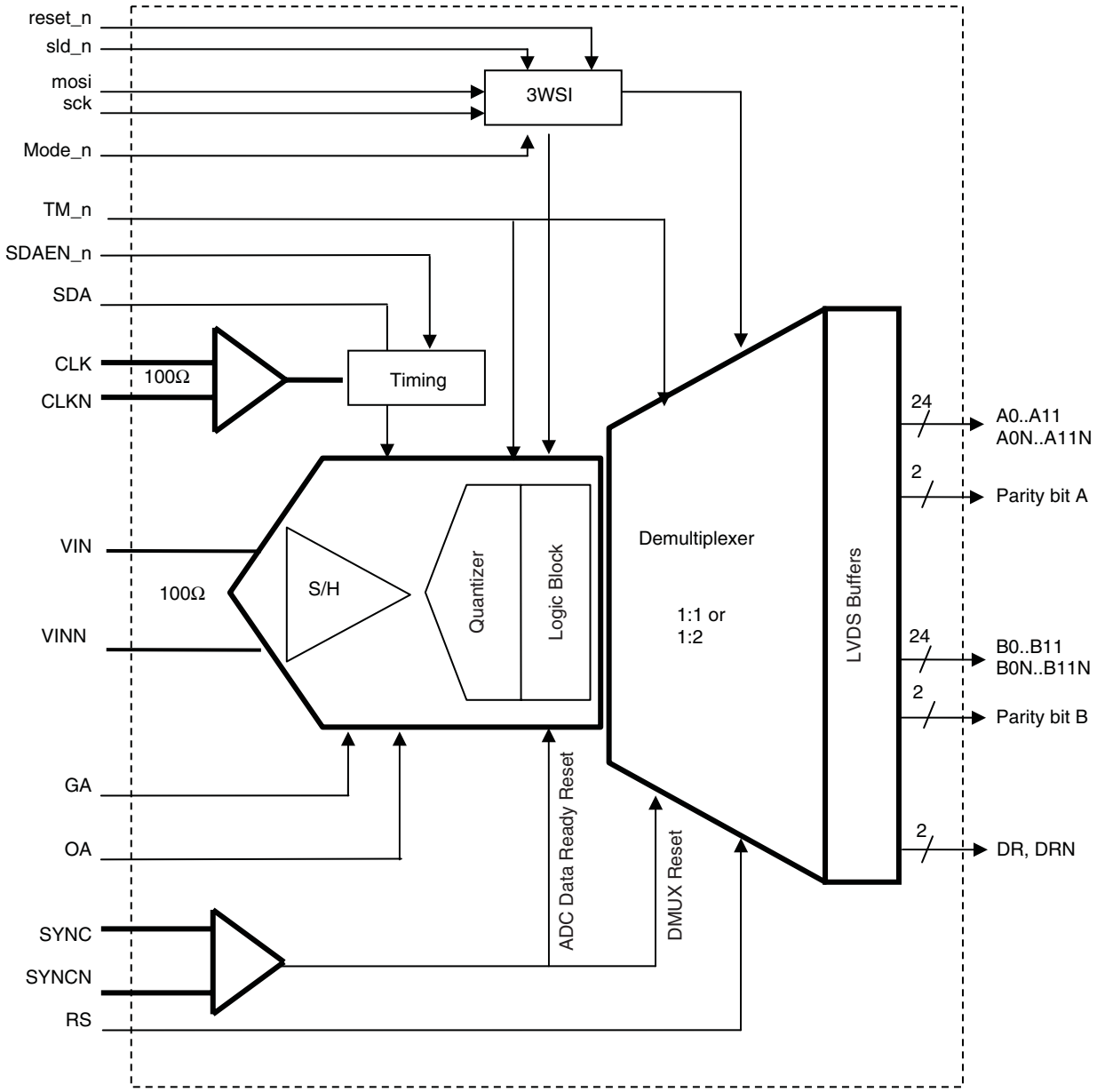
Applications

- Telecom Test Instrumentation
- Wireless Communications Systems
- Direct RF Down-conversion
- Automatic Test Equipment
- Direct L-Band RF Down Conversion
- Radar Systems
- Satellite Communications Systems

1. General Description

1.1 Block Diagram

Figure 1-1. ADC with Integrated DEMUX Block Diagram



1.2 Description

The EV12AS200 is a 12-bit 1.5 GSps ADC. The device includes a front-end Track and Hold stage (T/H), followed by an analog encoding stage (Analog Quantizer) which outputs analog residues resulting from analog quantization. Successive banks of latches regenerate the analog residues into logical levels before entering an error correction circuitry and a resynchronization stage followed by a DEMUX with 100Ω differential output buffers. It integrates a Wires Serial Interface (3WSI) circuit (write only), which can be activated or deactivated (via Mode signal). Main functions accessed via the 3WSI can also be accessed by hardware (OA, GA, SDA, SDAEN_n, TM_n, RS pin).

The EV12AS200 works in fully differential mode from analog inputs through digital outputs.
It operates in the first Nyquist zone up to L-Band.

DEMUX Ratio (1:1 or 1:2) can be selected with the pin RS or via the 3WSI when activated.
DEMUX outputs are synchronous on each port.

A differential Data Ready output is available to indicate when the outputs are valid. The Data Ready (differential DR, DRN) is common to the 2 ports.

A sampling rate mode (HSR) is embedded in order to output data faster up to 1 GHz in mode DMUX1:1.

In order to ease the synchronization of multiple ADC, the TRIGGER function could be activated.

A power up reset ensures that the first digitized data corresponds to the first acquisition. An external differential LVDS Reset (SYNC, SYNCN) can also be used. RES function allows changing the active edge of the RESET signal.

The gain control pin GA and offset control OA are provided to adjust the ADC gain and offset transfer function. These functions can also be accessed via the 3WSI.

A Sampling Delay Adjust function (SDA) is provided to fine tune the ADC aperture delay, for applications requesting the interleaving of multiple ADCs for example. It is enabled thanks to SDAEN_n pin. This function is also available with the 3WSI. In this case the tunable range is extended thanks to 2 bits for coarse adjustment.

For debug and testability, the following functions are provided:

- A static test mode, used to test either VOL or VOH at the ADC outputs (all bits at “0” level or “1” level respectively) – these modes are accessed only via the 3WSI when activated;
- A dynamic built-In Test (alignment pattern with period of 16), accessed by hardware (TM_n signal) or via 3WSI when activated.

A diode is provided to monitor the junction temperature, with both anode and cathode accessible.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1. Absolute Maximum Ratings

Parameter	Symbol	Comments	Value	Unit
V_{CC5} supply voltage	V_{CC5}		GND to 6	V
V_{CC3} supply voltage	V_{CC3}		GND to 3.6	V
V_{CCO} supply voltage	V_{CCO}		GND to TBC	V
Analog input voltages	V_{IN} or V_{INN}	DC coupled	TBD	V
Maximum difference between V_{IN} and V_{INN}	$V_{IN} – V_{INN}$		–2 to +2 (TBC)	V
Clock input voltage	V_{CLK} or V_{CLKN}	DC coupled	TBD	V
Maximum difference between V_{CLK} and V_{CLKN}	$V_{CLK} – V_{CLKN}$		–1.5 to +1.5 (TBC)	Vpp
Reset input voltage	V_{RST} or V_{RSTN}		–0.3 to V_{CC3} + 0.3	V
Analog input settings	VA	OA, GA, SDA	TBD to TBD	V
Control inputs	V_D	SDAEN, TM0, TM1, RS0, RS1, RSTN	–0.3 to V_{CC3} + 0.3	V
Junction Temperature	T_J		140	°C
Storage Temperature	Tstg		–65 to 150	°C

Notes: 1. Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability. All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

2. Maximum ratings enable active inputs with ADC powered off.

3. Maximum ratings enable floating inputs with ADC powered on.

2.2 Recommended Conditions of Use

Table 2-2. Recommended Conditions of Use

Parameter	Symbol	Comments	Typ	Unit
Power supplies	V_{CC5}		5.2	V
	V_{CC3}		3.3	V
	V_{CC0}		2.5	V
Differential analog input voltage (Full Scale)	$V_{IN} – V_{INN}$	100Ω differential	500	mVpp
Clock input power level	P_{CLK} P_{CLKN}	With 100Ω differential input With 1.3 Ghz sinewave input	+4	dBm
Operating Temperature Range	T_c T_j	Commercial “C” grade Industrial “V” grade	T_c >0°C < T_j < 90°C T_c > –40°C < T_j < 110°C	°C

2.3 Electrical Characteristics

Unless otherwise stated, requirements apply over the full operating temperature range (for performance) and at all power supply conditions.

Table 2-3. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
RESOLUTION			12		bit
POWER REQUIREMENTS					
Power Supply voltage - Analogue - Analogue Core and Digital - Output buffers[4]	 VCC5 VCC3 VCCO	 5 3.15 2.4	 5.2 3.3 2.5	 5.5 3.45 2.6	 V V V
Power Supply current in 1:1 DEMUX Ratio - Analogue - Analogue Core and Digital - Output buffers	 I_VCC5 I_VCC3 I_VCCO		 200 570 70		 mA mA mA
Power Supply current in 1:2 DEMUX Ratio - Analogue - Analogue Core and Digital - Output buffers	 I_VCC5 I_VCC3 I_VCCO		 200 570 110		 mA mA mA
Power dissipation - 1:1 Ratio with standard LVDS output swing, 665 Msps output rate HRS = 1 1 GSps output rate HRS = 0 - 1:2 Ratio with standard LVDS output swing 665 Msps output rate 1.33 GSps output rate	 P_D P_D P_D P_D		 3.1 3.15 3.22 3.22	 3.2 3.25 3.3 3.3	 W
LVDS Data and Data Ready Outputs					
Logic compatibility			LVDS differential		
Output Common Mode[1]	VOCM	1.125	1.25	1.375	V
Differential output ([1][2]	VODIFF	250	350	450	mV
Output level “High”[2]	VOH	1.25	–	–	V
Output level “Low” [2]	VOL	–	–	1.25	V
Output data format			Binary		
ANALOG INPUT					
Input type			AC coupled		
Analogue input Common mode (for DC coupled input)			3.12		
Full scale input voltage range (differential mode)	VIN VINN	–125 –125		+125 +125	mV mV
Full scale analog input power level	PIN		–5		dBm
Analog input capacitance (die only)	CIN		0.3 (TBC)		pF
Input leakage current (VIN = VINN = 0V)	IIN		50		µA
Analog Input resistance (Differential)	RIN	96	100	104	Ω

Table 2-3. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
CLOCK INPUT (CLK, CLKN)					
Input type		DC or AC coupled			
Clock Input Common Mode (for DC coupled clock)	VICM		2.72		V
Clock Input power level (low phase noise sinewave input) 100Ω differential	PCLK	0	4	+10	dBm
Clock input swing (differential voltage) on each clock input	VCLK VCLKN	±447	±708	±1410	mV
Clock input capacitance (die only)	CCLK		0.3		pF
Clock Input resistance (Differential)	RCLK	95	100	105	Ω
SYNC, SYNCN (active low)					
Logic compatibility		LVDS			
Input Common Mode	VICM	1.125	1.25	1.375	V
Differential input	VIDIFF	250	350	450	mV
Input level “High”	VIH				V
Input level “Low”	VIL				V
DIGITAL INPUTS (RS, SDAEN_n, TM_n)					
Logic low - Resistor to ground - Voltage level - Input current	 R_{IL} V_{IL} I_{IL}	 0		 10 0.5 450	 Ω V µA
Logic high - Resistor to ground - Voltage level - Input current	 R_{IH} V_{IH} I_{IH}	 10k 2.0		 infinite 150	 Ω V µA
OFFSET, GAIN & SAMPLING DELAY ADJUST SETTINGS (OA, GA, SDA)					
Min voltage for minimum Gain, Offset or SDA	Analog_min	$2*V_{cc3}/3 - 0.5$			V
Max voltage for maximum Gain, Offset or SDA	Analog_max			$2*V_{cc3}/3 + 0.5$	V
Input current for min setting	I_{min}			200 (TBC)	µA
Input current for nominal setting	I_{nom}			50 (TBC)	µA
Input current for max setting	I_{max}			200 (TBC)	µA
3WSI (sck, sld_n, mosi, reset_n, mode_n)					
Logic compatibility		3.3V CMOS			
Low Level input voltage	V_{IL}	0		1	V
High Level input voltage	V_{IH}	2.3		V_{cc3}	V
Low Level input current			TBD		µA
High Level input current			TBD		µA
DC ACCURACY					
Missing codes	M_{CODES}	None allowed			
Differential Non Linearity (for information only)	DNL+		TBD		LSB
Differential Non Linearity (for information only)	DNL-		TBD		LSB

Table 2-3. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Integral Non Linearity (for information only)	INL+		TBD		LSB
Integral Non Linearity (for information only)	INL-		TBD		LSB
Gain central value(3)	ADC_{GAIN}	0.9	1.0	1.1	
Gain error drift versus temperature (over 15°C)				0.15 (TBC)	dB
ADC offset(4)	ADC_{OFFSET}		TBD		LSB

Notes: 1. Assuming 100Ω termination ASIC load.
2. VOH min and VOL max can never be 1.25V at the same time when VODIFFmin.
3. The ADC Gain center value can be tuned to 1.0 thanks to Gain adjust function.
4. The ADC offset can be tuned to mid code 2048 thanks to Offset adjust function.

2.4 Dynamic Performance

Unless otherwise stated, requirements apply over the full operating temperature range (for performance) and at all power supply conditions assuming an external clock jitter of 75 fs rms. ADC internal clock jitter is 75 fs rms.

Table 2-4. Dynamic Performance

Parameter		Symbol	Min	Typ	Max	Unit	Note
AC Analog Inputs							
Full power Input Bandwidth		FPBW		2.3		GHz	
Input voltage standing Wave Ratio up to 1.8 GHz (unpowered device)		VSWR		1.2:1			
–1 dBFS differential input mode, 50% clock duty cycle, +4dBm differential clock, internal jitter = 75 fs rms							
Signal to Noise And Distortion Ratio		SINAD				dBFS	(1)
FS = 1 GSps	Fin = 665 MHz			56.6			
FS = 1 GSps	Fin = 1 GHz			55.9			
FS = 1.33 GSps	Fin = 1.3 GHz			55.2			
Effective Number of Bits		ENOB				Bit FS	(1)
FS = 1 GSps	Fin = 665 MHz			9.1			
FS = 1 GSps	Fin = 1 GHz			9.0			
FS = 1.33 GSps	Fin = 1.3 GHz			8.9			
Signal to Noise Ratio		SNR				dBFS	
FS = 1 GSps	Fin = 665 MHz			58.1			
FS = 1 GSps	Fin = 1 GHz			57.5			
FS = 1.33 GSps	Fin = 1.3 GHz			56.6			
Total Harmonic Distortion (25 harmonics)		|THD|				dBFS	(1)
FS = 1 GSps	Fin = 665 MHz			62			
FS = 1 GSps	Fin = 1 GHz			61.5			
FS = 1.33 GSps	Fin = 1.3 GHz			61			

Table 2-4. Dynamic Performance (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Spurious Free Dynamic Range FS = 1 GSps Fin = 665 MHz FS = 1 GSps Fin = 1 GHz FS = 1.33 GSps Fin = 1.3 GHz	|SFDR|		66 65.5 65		dBFS	(1)
–12 dBFS differential input mode, 50% clock duty cycle, +4dBm differential clock, internal jitter = 75 fs rms						
Signal to Noise And Distortion Ratio FS = 1.33 GSps Fin = 1.3 GHz	SINAD		58.3		dBFS	
Effective Number of Bits FS = 1.33 GSps Fin = 1.3 GHz	ENOB		9.4		Bit FS	
Signal to Noise Ratio FS = 1.33 GSps Fin = 1.3 GHz	SNR		58.8		dBFS	
Total Harmonic Distortion (25 harmonics) FS = 1.33 GSps Fin = 1.3 GHz	|THD|		68		dBFS	
Spurious Free Dynamic Range FS = 1.33 GSps Fin = 1.3 GHz	|SFDR|		70		dBFS	
Broad band Performances						
Noise Power Ratio Notch centered on 800 MHz, notch width 10 MHz on 770 MHz –1450 MHz band (~700 MHz pattern) 1.5 GSps at optimum loading factor of –14 dBFS	NPR		48		dB	
Noise Power Ratio Notch centered on 1100 MHz, notch width 10 MHz on 770 MHz –1450 MHz band 1.5 GSps at optimum loading factor of –14 dBFS	NPR		48		dB	

Note: 1. Value without taken into account 3rd order harmonic (H3).

2.5 Timing Characteristics and Switching Performances

Unless otherwise stated, requirements apply over the full operating temperature range (for performance) and at all power supply conditions

Table 2-5. Timing characteristics and Switching Performances

Parameter	Symbol	Min	Typ	Max	Unit	Note
SWITCHING PERFORMANCE AND CHARACTERISTICS						
Maximum clock frequency[1] 1:1 DEMUX Ratio 1:2 DEMUX Ratio				 1000 1500	MHz	
Minimum clock frequency[1]		300			MHz	
Maximum Output Rate per port (Data and Data Ready) 1:1 DEMUX Ratio HRS = 1 HRS = 0 1:2 DEMUX Ratio				 750 1000 750	Msps	
Analogue input frequency		10		1500	MHz	
BER			10^{-12}		Error/sample	
TIMING						
ADC settling time (V_{IN}-V_{INN} = 400 mV pp)	TS		TBD		ps	
Overvoltage recovery time	ORT			TBD	ps	
ADC step response (10% to 90%)			170		ps	
Overshoot			0.2		%	
Ringback			0.2		%	
Sampling Clock duty cycle			50		%	
Minimum clock pulse width (high)	TC1	0.3		1.5	ns	
Minimum clock pulse width (low)	TC2	0.3		1.5	ns	
Aperture delay[1]	TA		TBD		ns	
Internal clock Jitter				100	fsrms	
Output rise/fall time for DATA (20% to 80%)[3]	TR/TF		420		ps	[3]
Output rise/fall time for DATA READY (20% to 80%)[2]	TR/TF		350		ps	[3]
Data output delay[4]	TOD		TBD		ps	[3]
Data Ready output delay[4]	TDR		TBD		ps	[3]
	|TOD –TDR|		0		ps	[3]
Output Data to Data Ready propagation delay[5]	TD1		TBD		ps	[3]
Data Ready to Output Data propagation delay[5]	TD2		TBD		ps	[3]

Table 2-5. Timing characteristics and Switching Performances (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output Data Pipeline delay 1:1 DEMUX Ratio 1:2 DEMUX Ratio Port A Port B	TPD		 4 (TBC) 4 (TBC) 3 (TBC)		Clock cycle	
Data Ready Pipeline delay 1:1 DEMUX Ratio 1:2 DEMUX Ratio Port A Port B			 4.5 (TBC) 5 (TBC) 5 (TBC)		Clock cycle	
SYNC to DR, DRN 1:1 DEMUX Ratio 1:2 DEMUX Ratio	TRDR		 2.5 2.6		ps	
SYNC min pulse duration		See application note			ps	

Notes:
1. See Definition Of Terms.
2. Data Ready outputs are active on both rising and falling edges (DR/2 mode)
3. 100Ω// C_{LOAD} = 2pF // 2nH termination (for each single-ended output). Termination load parasitic capacitance derating value: 50 ps/pF (LVDS).
4. TOD and TDR propagation times are defined at package input/outputs. They are given for reference only.
5. Values for TD1 and TD2 are given for a 1.33 GSps external clock frequency (50% duty cycle). For different sampling rates, apply the following formula: TD1 = T/2 + (TOD-TDR) and TD2 = T/2 - (TOD-TDR), where T=clock period. This places the rising edge (True-False) od the differential Data ready signal in the middle of the Output Data Valid window. This gives maximum setup and hold times for external acquisition. The difference (TD1-TD2) gives information if Data Ready is centered on the output data. If Data Ready is in middle TD1 = TD2 = Tdata/2. This places the rising edge (True-False) of the differential Data Ready signal in the middle of the Output Data valid window. This gives maximum setup and hold times for external data acquisition.

2.6 Timing Diagrams

Figure 2-1. Principle of Operation, DMUX 1:1

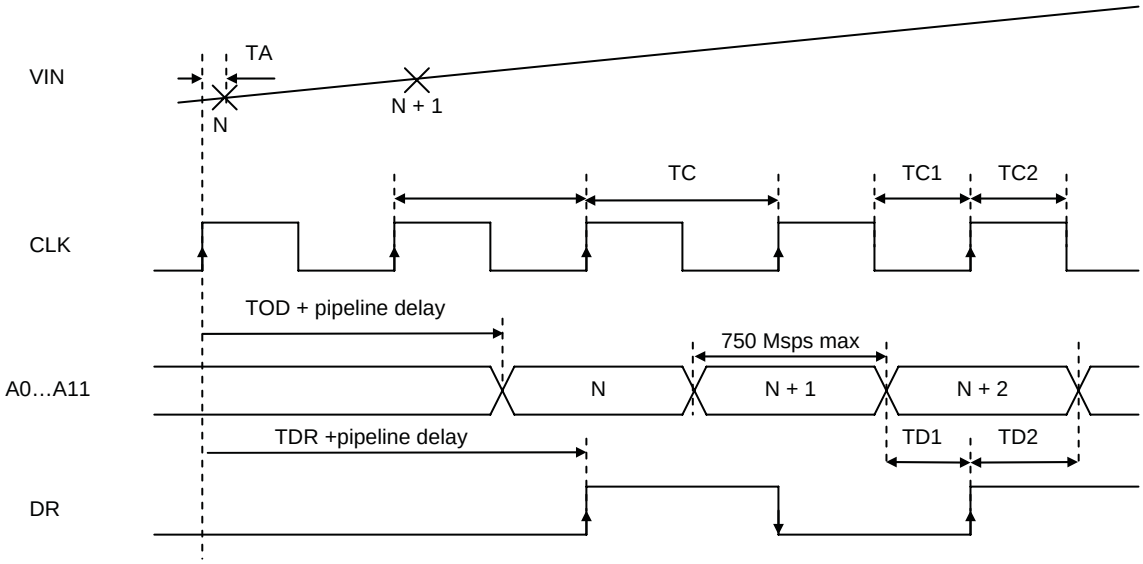


Figure 2-2. Principle of Operation, DMUX 1:2

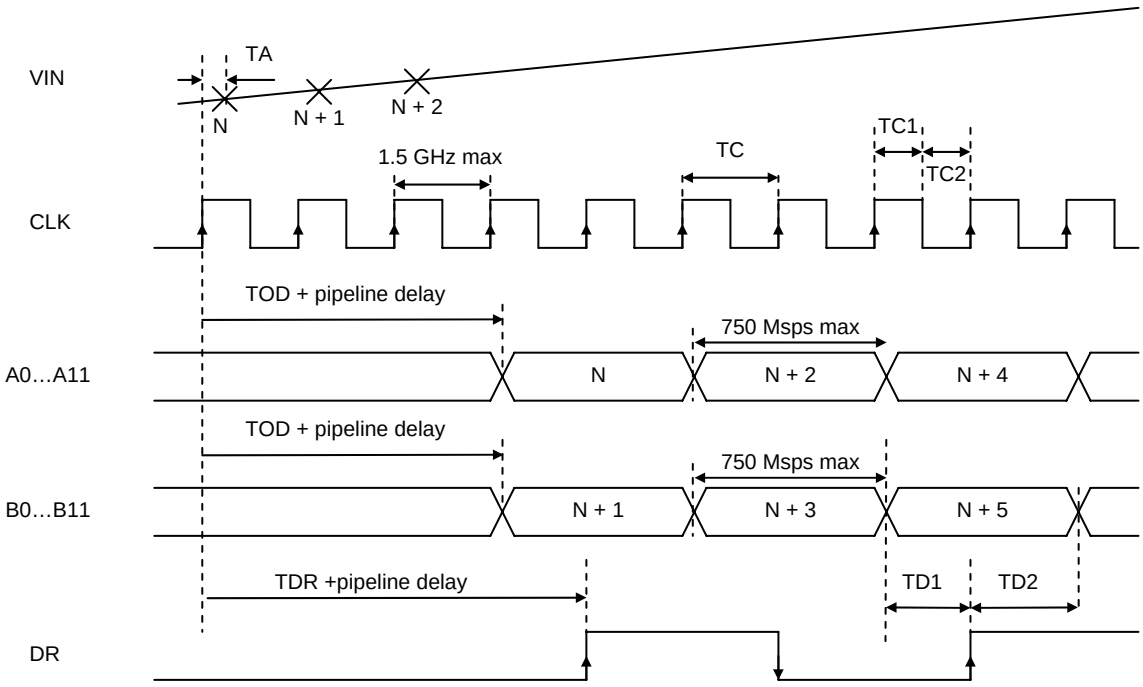


Figure 2-3. Power up Reset Timing Diagram (1:1 DMUX)

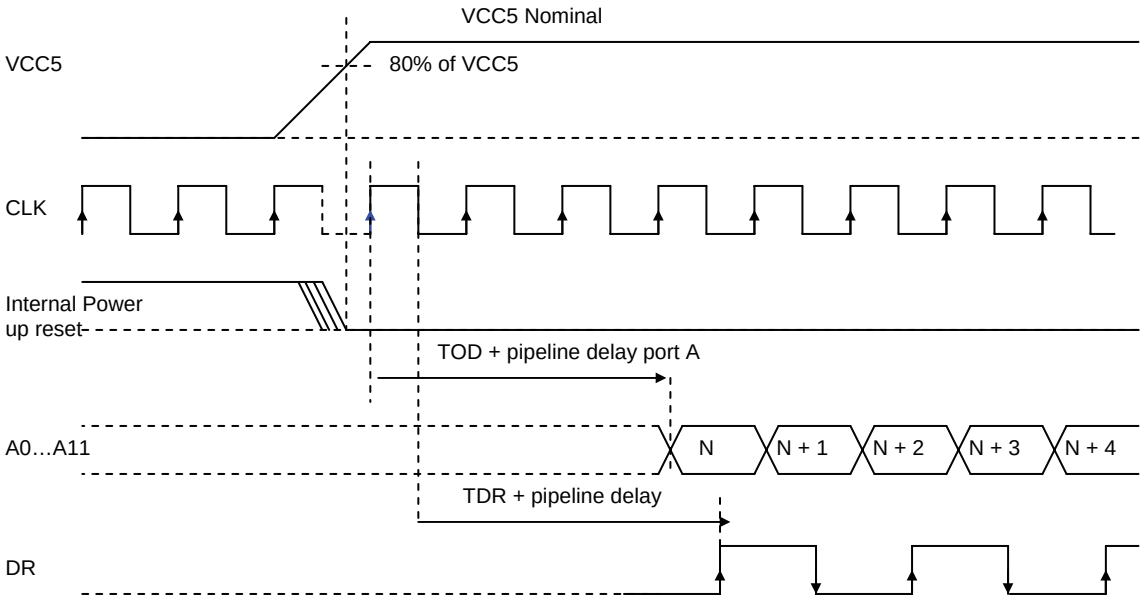
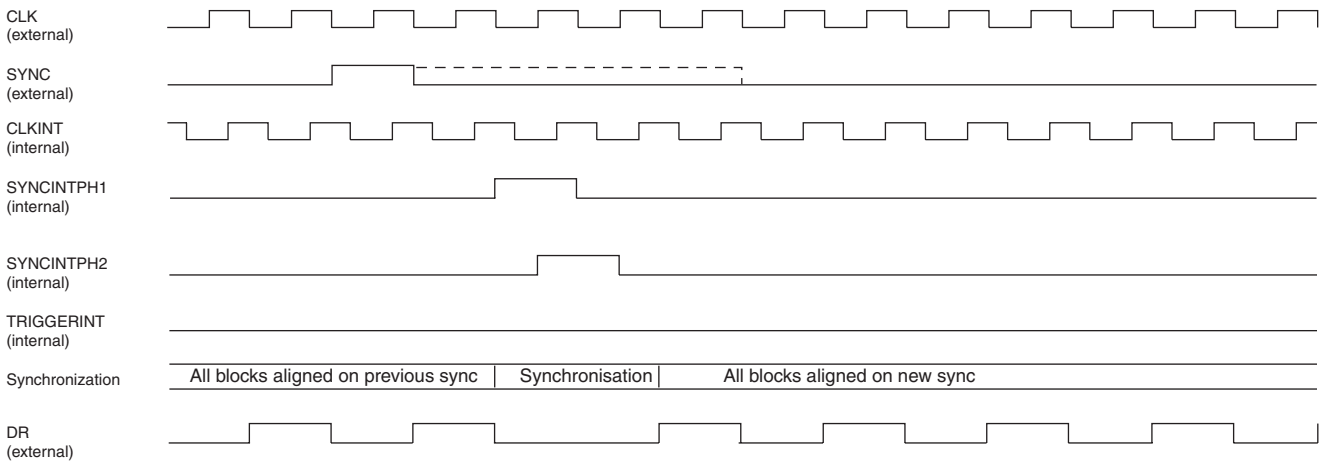


Figure 2-4. External Reset Timing Diagram (1:1 DMUX)



2.7 Definition of Terms

Table 2-6. Definition of Terms

Abbreviation	Term	Definition	
(Fs max)	*Maximum Sampling Frequency*	Sampling frequency for which ENOB < 6 bits	
(Fs min)	*Minimum Sampling frequency*	Sampling frequency for which the ADC Gain has fallen by 0.5dB with respect to the gain reference value. Performances are not guaranteed below this frequency.	
(BER)	*Bit Error Rate*	Probability to exceed a specified error threshold for a sample at maximum specified sampling rate. An error code is a code that differs by more than ±16 LSB from the correct code.	
(FPBW)	*Full power input bandwidth*	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at Full Scale –1 dB (–1 dBFS).	
(SSBW)	*Small Signal Input bandwidth*	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at Full Scale –10 dB (–10 dBFS).	
(SINAD)	*Signal to noise and distortion ratio*	Ratio expressed in dB of the RMS signal amplitude, set to 1 dB below Full Scale (–1 dBFS), to the RMS sum of all other spectral components, including the harmonics except DC.	
(SNR)	*Signal to noise ratio*	Ratio expressed in dB of the RMS signal amplitude, set to 1dB below Full Scale, to the RMS sum of all other spectral components excluding the twenty five first harmonics.	
(THD)	*Total harmonic distortion*	Ratio expressed in dB of the RMS sum of the first twenty five harmonic components, to the RMS input signal amplitude, set at 1 dB below full scale. It may be reported in dB (i.e, related to converter –1 dB Full Scale), or in dBc (i.e, related to input signal level).	
(SFDR)	*Spurious free dynamic range*	Ratio expressed in dB of the RMS signal amplitude, set at 1 dB below Full Scale, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It may be reported in dB (i.e., related to converter –1 dB Full Scale), or in dBc (i.e, related to input signal level).	
(ENOB)	*Effective Number Of Bits*	$ENOB = \frac{SINAD - 1.76 + 20 \log (A / FS/2)}{6.02}$	Where A is the actual input amplitude and FS is the full scale range of the ADC under test
(DNL)	*Differential non linearity*	The Differential Non Linearity for an output code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic.	
(INL)	*Integral non linearity*	The Integral Non Linearity for an output code i is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.	
(TA)	*Aperture delay*	Delay between the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point), and the time at which (V_{IN},V_{INN}) is sampled.	
(JITTER)	*Aperture uncertainty*	Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.	
(TS)	*Settling time*	Time delay to achieve 0.2 % accuracy at the converter output when a 80% Full Scale step function is applied to the differential analog input.	
(ORT)	*Overvoltage recovery time*	Time to recover 0.2 % accuracy at the output, after a 150 % full scale step applied on the input is reduced to midscale.	
(TOD)	*Digital data Output delay*	Delay from the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.	
(TDR)	*Data ready output delay*	Delay from the falling edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.	

Table 2-6. Definition of Terms (Continued)

Abbreviation	Term	Definition
(TD1)	*Time delay from Data transition to Data Ready*	This gives maximum setup and hold times for external acquisition. The difference (TD1-TD2) gives information if Data Ready is centered on the output data. If Data Ready is in middle TD1 = TD2 = Tdata/2. This places the rising edge (True-False) of the differential Data Ready signal in the middle of the Output Data valid window. This gives maximum setup and hold times for external data acquisition
(TD2)	*Time delay from Data Ready to Data*	
(TC)	*Encoding clock period*	TC1 = Minimum clock pulse width (high) TC = TC1 + TC2 TC2 = Minimum clock pulse width (low)
(TPD)	*Pipeline Delay*	Number of clock cycles between the sampling edge of an input data and the associated output data being made available, (not taking in account the TOD).
(TRDR)	*Data Ready reset delay*	Delay between the falling edge of the Data Ready output asynchronous Reset signal (RSTN) and the reset to digital zero transition of the Data Ready output signal (DR).
(TR)	*Rise time*	Time delay for the output DATA signals to rise from 20% to 80% of delta between low level and high level.
(TF)	*Fall time*	Time delay for the output DATA signals to fall from 20% to 80% of delta between low level and high level.
(PSRR)	*Power supply rejection ratio*	Ratio of input offset variation to a change in power supply voltage.
(NRZ)	*Non return to zero*	When the input signal is larger than the upper bound of the ADC input range, the output code is identical to the maximum code and the Out of Range bit is set to logic one. When the input signal is smaller than the lower bound of the ADC input range, the output code is identical to the minimum code, and the Out of range bit is set to logic one. (It is assumed that the input signal amplitude remains within the absolute maximum ratings).
(IMD)	*InterModulation Distortion*	The two tones intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products.
(NPR)	*Noise Power Ratio*	The NPR is measured to characterize the ADC performance in response to broad bandwidth signals. When applying a notch-filtered broadband white-noise signal as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test.
(VSWR)	*Voltage Standing Wave Ratio*	The VSWR corresponds to the ADC input insertion loss due to input power reflection. For example a VSWR of 1.2 corresponds to a 20dB return loss (ie. 99% power transmitted and 1% reflected).

3. Pin Description

Figure 3-1. Pin Mapping Ci CGA (Top View)

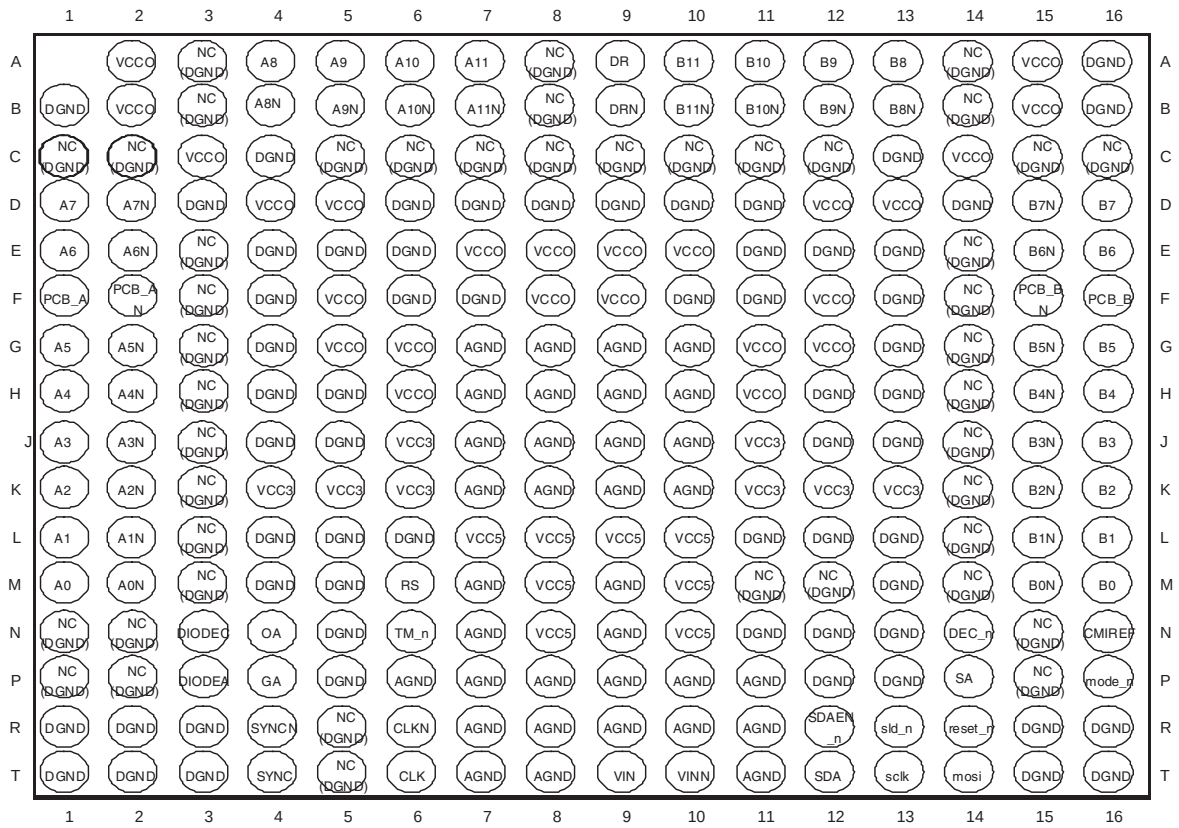


Table 3-1. Pin Description

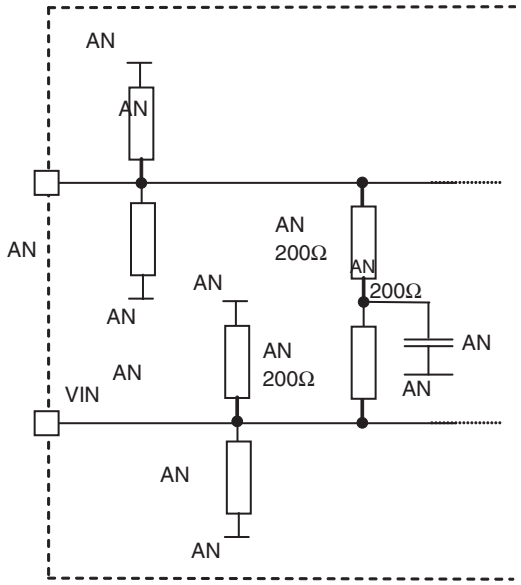
Signal Name	Pin Number	Function	Dir.	Equivalent Simplified Schematics
POWER SUPPLIES				
V_{CC5}	L7, L8, L9, L10, M8, M10, N8, N10	5.2V analog supply (Front-end Track & Hold circuitry) Referenced to AGND	N/A	
V_{CC3}	J6, J11, K4, K5, K6, K11, K12, K13	3.3V power supply (ADC Core, Regeneration and Logic, DEMUX circuitry and Timing circuitry) Referenced to AGND	N/A	
V_{CCO}	A2, A15, B2, B15, C3, C14, D4, D5, D12, D13, E7, E8, E9, E10, F5, F8, F9, F12, G5, G6, G11, G12, H6, H11	2.5V digital power supply (output buffers) Referenced to DGND	N/A	
DGND	A16, B1, B16, C4, C13, D3, D6, D7, D8, D9, D10, D11, D14, E4, E5, E6, E11, E12, E13, F4, F6, F7, F10, F11, F13, G4, G13, H4, H5, H12, H13, J4, J5, J12, J13, L4, L5, L6, L11, L12, L13, M4, M5, M13, N5, N11, N12, N13, P5, P12, P13, R1, R2, R3, R15, R16, T1, T2, T3, T15, T16	Digital Ground DGND should be separated from AGND on board (the two planes can be reunited via 0 ohm resistors)	N/A	
AGND	G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M7, M9, N7, N9, P6, P7, P8, P9, P10, P11, R7, R8, R9, R10, R11, T7, T8, T11	Analogue Ground AGND should be separated from DGND on board (the two planes can be reunited via 0 ohm resistors)	N/A	
ANALOG INPUTS				
VIN VINN	T9 T10	Analogue input (differential) with internal common mode It should be driven in AC coupling. Analogue input is sampled and converted on each positive transition of the CLK input. Equivalent internal differential 100 ? input resistor.	I	
CMIRef	N16	Input common mode signal	O	

Table 3-1. Pin Description (Continued)

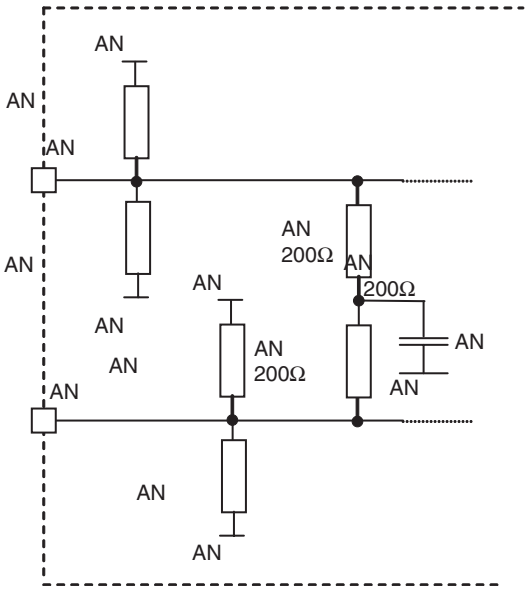
Signal Name	Pin Number	Function	Dir.	Equivalent Simplified Schematics
CLOCK INPUTS				
CLK CLKN	T6 R6	Master sampling clock input (differential) with internal common mode at 2.65V It should be driven in AC coupling. Equivalent internal differential 100Ω input resistor.	I	
RESET INPUT				
SYNC SYNCN	T4 R4	Reset input (active low). It is available in case it is necessary to reset the ADC during operation (it is not mandatory to perform an external reset on the ADC for proper operation of the ADC as a power up reset is already implemented). This reset is Synchronous, it is LVDS compatible.	I	

Table 3-1. Pin Description (Continued)

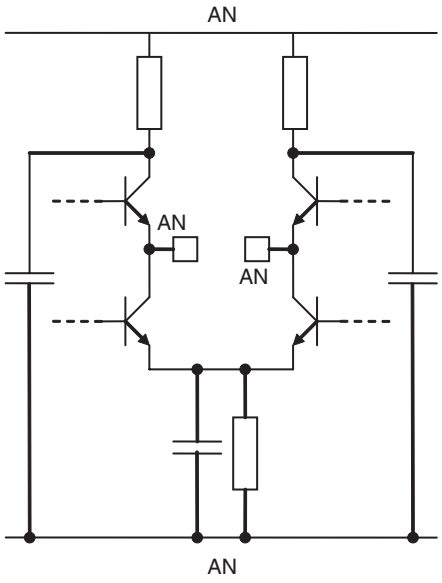
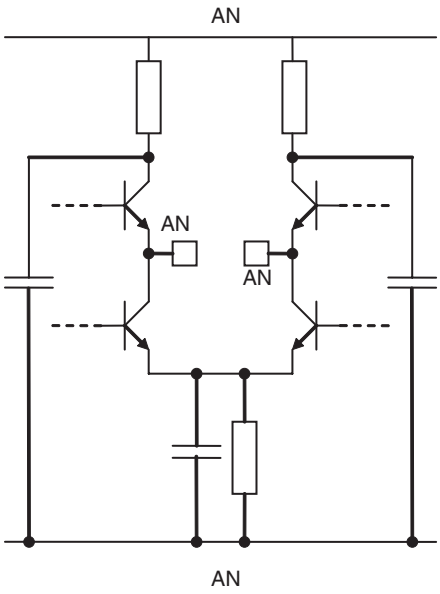
Signal Name	Pin Number	Function	Dir.	Equivalent Simplified Schematics
DIGITAL OUTPUTS				
A0, A0N A1, A1N A2, A2N A3, A3N A4, A4N A5, A5N A6, A6N A7, A7N A8, A8N A9, A9N A10, A10N A11, A11N	M1, M2 L1, L2 K1, K2 J1, J2 H1, H2 G1, G2 E1, E2 D1, D2 A4, B4 A5, B5 A6, B6 A7, B7	In-phase (Ai) and inverted phase (AiN) digital outputs on DEMUX Port A (with i = 0…11) Differential LVDS signal A0 is the LSB, A11 is the MSB The differential digital output data is transmitted at clock rate divide by DMUX ratio (refer to RS0 and RS1 settings). Each of these outputs should be terminated by 100 ? differential resistor placed as close as possible to the differential receiver.	O	
B0, B0N B1, B1N B2, B2N B3, B3N B4, B4N B5, B5N B6, B6N B7, B7N B8, B8N B9, B9N B10, B10N B11, B11N	M16, M15 L16, L15 K16, K15 J16, J15 H16, H15 G16, G15 E16, E15 D16, D15 A13, B13 A12, B12 A11, B11 A10, B10	In-phase (Bi) and inverted phase (BiN) digital outputs on DEMUX Port B (with i = 0…11) Differential LVDS signal B0 is the LSB, B11 is the MSB The differential digital output data is transmitted at clock rate divide by DMUX ratio (refer to RS0 and RS1 settings). Each of these outputs should be terminated by 100Ω differential resistor placed as close as possible to the differential receiver.	O	

Table 3-1. Pin Description (Continued)

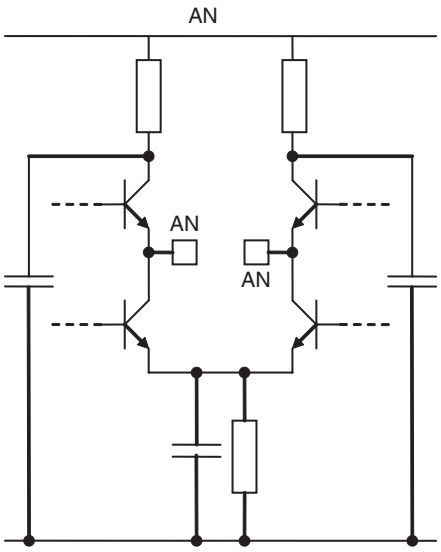
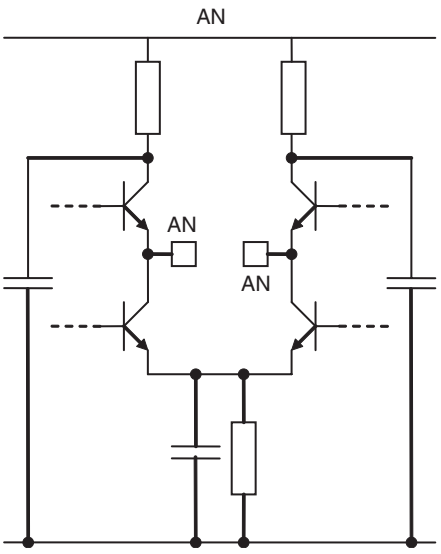
Signal Name	Pin Number	Function	Dir.	Equivalent Simplified Schematics
PCB_A PCB_AN	F1 F2	Parity Check Bit port A	O	
PCB_B PCB_BN	F16 F15	Parity Check Bit port B	O	
DR DRN	A9 B9	In-phase (DR) and inverted phase (DRN) global data ready digital output clock Differential LVDS signal The differential digital output clock is used to latch the output data on rising and falling edge. The differential digital output clock rate is (CLK/2) divided by the DMUX ratio (provided by RS0 and RS1 pins). This differential digital output clock should be terminated by 100Ω differential resistor placed as close as possible to the differential receiver.	O	
ADDITIONAL FUNCTIONS				
Reserved	N14	Reserved pin/ To keep NC	I	
TM_n	N6	Test Mode	I	Driving by resistor: 10 ohm or 10 kohm Driving by voltage: 0.5 V or 2 V
RS	M6	DEMUX Ratio Selection 7	I	
SDAEN_n	R12	Sampling delay adjust enable	I	
SDA	T12	Sampling delay adjust	I	
GA	P4	Gain Adjust	I	
OA	N4	Offset Adjust	I	

Table 3-1. Pin Description (Continued)

Signal Name	Pin Number	Function	Dir.	Equivalent Simplified Schematics
SA	P14	Reserved	I	To leave unconnected or must be connected to 2.2V through a potential divider
mode_n	P16	SPI Enable (active Low) a. “1” ◊SPI not active b. “0” --< SPI active	I	
sclk	T13	SPI write only clock. Serial data on mosi signal is shifted into SPI synchronously to this signal on positive transition of sck.	I	
mosi	T14	SPI write only serial data input. Shifted into SPI while sld_n is active (low).	I	
Sld_n	R13	SPI write only Serial load enable input. When this signal is active (low), sck is used to clock data present on mosi signal.	I	
Reset_n	R14	SPI write only asynchronous reset input signal. This signal allows to reset internal values of the SPI to their default value.	I	
DIODEA	P3	Die Junction temperature monitoring (anode)		
DIODEC	N3	Die Junction temperature monitoring (cathode)		
NC(DGND)	A3, A8, A14, B3, B8, B14, C1, C2, C5, C6, C7, C8, C9, C10, C11, C12, C15, C16, E3, E14, F3, F14, G3, G14, H3, H14, J3, J14, K3, K14, L3, L14, M3, M11, M12, M14, N1, N2, N15, P1, P2, P15, R5, T5	Non connected pins, to be connected on board to DGND		

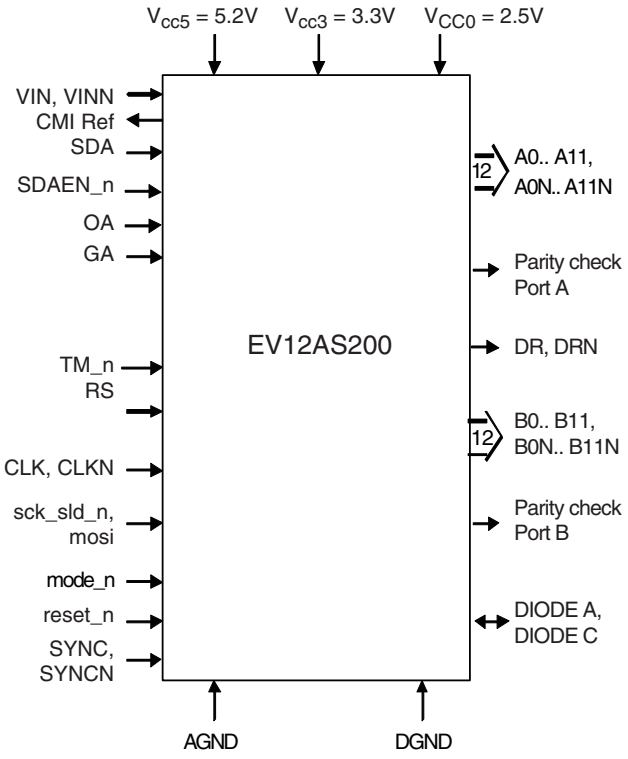
4. Functional Description

4.1 List of Functions

- External synchronous LVDS reset (SYNC, SYNCN)
- Write only 3WSI-like digital interface (gain, offset, sampling delay adjust, DMUX ratio selection, test modes)
- ADC Gain adjust
- ADC Offset adjust
- Sampling delay adjust
- Dynamic Test Mode (alignment sequence)
- Data Ready common to the 2 output ports
- HSR function
- RES function
- TRIGGER function

Table 4-1. Function Descriptions

Name	Function
V_{CC5}	5.2V Power supply
V_{CC3}	3.3V Power supply
V_{CC0}	2.5V Power supply
GND	Ground
GNDO	Digital Ground for outputs
VIN,VINN	Differential Analog Input
CLK,CLKN	Differential Clock Input
[A0:A11] [A0N:A11N]	Differential Output Data on port A
PCB_A, PCB_AN	Parity check bit port A
[B0:B11] [B0N:B11N]	Differential Output Data on port B
PCB_B, PCB_BN	Parity check bit port B
DR,DRN	Global Differential Data Ready
RS	DEMUX Ratio select
SYNC, SYNCN	External reset
TM_n	Test Mode Enable
SDA	Sampling Delay Adjust input
SDAEN_n	Sampling Delay Adjust Enable
GA	Gain Adjust input.
OA	Offset adjust input
DIODEA, DIODEC	Diode for die junction temperature monitoring
Sck, sld_n, reset_n, mosi, mode_n	3WSI write only pins
CMIRef	Input common mode



The different functions could be enabled by external dedicated command pin and/or 3WSI interface according the table below.

Table 4-2. ADC Mode Settings – Summary by external or by the 3WSI

Function	3WSI	External command pin	Description
TM_n	yes	yes	Test mode ON/OFF (Active LOW)
TESTTYPE	yes (2 bits)	no	Test Type : dynamic or static pattern (static pattern : 3WSI only)
SDAEN_n	yes	yes (fine only)	Sampling Delay Adjust ON/OFF (Active LOW)
SDA_fine	yes (8 bits)	yes (2,2V ±0,5V)	SDA Fine tuning (0 -> 255 for 3wsi or 1,7V -> 2,7V external)
SDA_coarse	yes (2 bits)	no	SDA Coarse tuning (3WSI Only) : "00" -> 0ps, "01" -> 30ps, "10" -> 60ps, "11" -> 90ps
RS	yes	yes	Demux Ratio Select : "1" : 1:2 mode, "0" : 1:1 mode
GAIN ADJUST	yes (10 bits)	yes (2,2V ±0,5V)	Gain Adjust (0 -> 1023 for 3wsi or 1,7V -> 2,7V external)
OFFSET ADJUST	yes (10 bits)	yes (2,2V ±0,5V)	Offset Adjust (0 -> 1023 for 3wsi or 1,7V -> 2,7V external)
mode_n	no	yes	3wsi ON/OFF (Active LOW, all other settings are external if OFF)
trig_sel_n	yes	no	SYNC Behavior : "1" : Trigger Mode, "0" : Syncronization Mode
res	yes	no	SYNC Active Edge ("1" : falling, "0" : rising)
hsr	yes	no	Sampling Rate Mode (1:1 demux ratio) : "1" : Half speed, "0" : Full Speed

4.2 External Reset (SYNC, SYNCN)

An external LVDS reset (SYNC, SYNCN) is available in case it is necessary to reset the ADC during operation (it is not mandatory to perform an external reset on the ADC for proper operation of the ADC as a power up reset is already implemented). This reset is LVDS compatible. It is active low. It is asynchronous but is relatched internally to the sampling clock.

4.3 Mode (mode_n) function

It is possible to activate the digital interface via the mode_n signal, external command.

The coding table for the mode is given in Table 4-3.

Table 4-3. Mode Coding

Function	Logic Level	Electrical Level	Description
Mode_n	0	10Ω to ground	Digital interface active
	1	10 KΩ to ground	Digital interface inactive (default mode)
		N/C	

Description of the 3WSI interface are described in Section 4.12 on page 29.

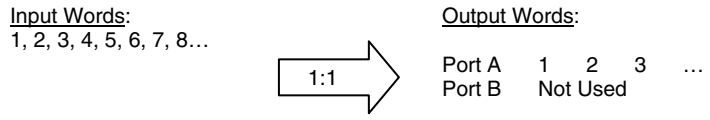
When the 3WSI functions are activated (mode_n active), the hardware commands are disabled.

When the hardware commands are activated (mode_n disabled), the values of the register can not be modified and are set to default.

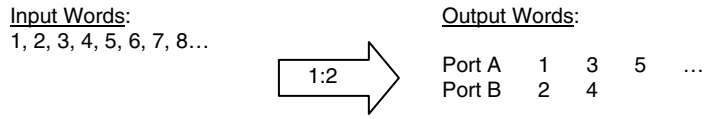
4.4 DEMUX Ratio Select (RS) Function

Two DEMUX Ratios can be selected via the RS pin or via the 3WSI.

ADC in 1:1 Ratio



ADC in 1:2 Ratio



Note that Data of the different ports are synchronous: they appear at the same instant on each port.

4.4.1 DEMUX ratio selection with the external command (RS pin)

Two DEMUX Ratios can be selected thanks to pin RS according to the table below.

Table 4-4. Ratio Select Coding

Function	Logic Level	Electrical Level	Description
RS	0	10Ω to ground	1:1 DEMUX Ratio (Port A)
	1	10 KΩ to ground	1:2 DEMUX Ratio (Ports A and B)
		N/C	

4.4.2 DEMUX Ratio Selection with 3WSI

This mode is selectable when WSI interface (Mode_n = 0) is activated and when the bit D0 of the state register is set to 0.

Please refer to State register coding for more details in Section 4.12 ”ADC 3WSI Description (ADC Controls)” on page 29.

Table 4-5. State Register Coding

Label		Coding	Description	Default Value
RS	D0	0	1:1 DMUX mode	1
		1	1:2 DMUX mode	

4.5 Test Mode (TM_n) Function

This mode can be selected thanks to pin TM_n according to the table below or 3WSI interface.

4.5.1 Test Mode with the external command (TM_n pin)

One dynamic test mode is made available in order to test the outputs of the ADC; this test mode corresponds to a pseudo random sequence with a period of 16.

The coding table for the Test mode is given in Table 4-6 on page 24.

Table 4-6. Test Mode Coding

Function	Logic Level	Electrical Level	Description
TM_n	0	10Ω to ground	Alignment pattern ON (period of 16) see Figure 4-1
	1	10 KΩ to ground	Normal conversion mode (default mode)
		N/C	

4.5.2 Test Mode with 3WSI

This mode is selectable when 3WSI interface (Mode_n = 0) is activated and when the bit D2 of the stare register is set to 0.

Please refer to State register coding for more details in Section 4.12 ”ADC 3WSI Description (ADC Controls)” on page 29.

Description

Table 4-7. Test Register Coding (Address 0101)

Label	Coding	Description	Default Value
TEST TYPE <1:0>	00	VOL Test mode ON	11
	01	VOH Test mode ON	
	10	Unused	
	11	Alignment Pattern ON (period 16)	

Test Mode functionalities

Notes: Alignment pattern is described in Figure 6.

Goals:

Validation at full speed of interface between ADC and FPGA in both DMUX 1:1 or DMUX 1:2 modes. Verification of synchronization of output data between different ADC (Output data shift after external synchronization pulse).

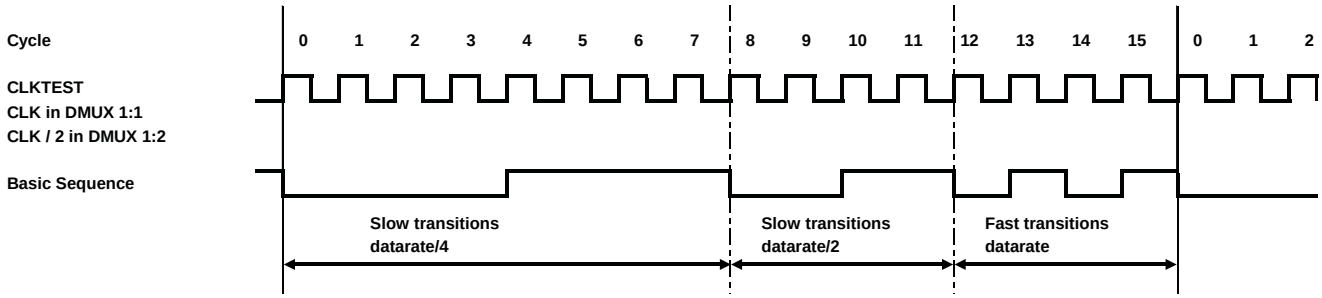
Basic Sequence

Period of 16 cycles of output datarate.
Slow transitions at datarate/4 or datarate/2 (full swing).
Fast transitions at datarate (reduced swing).
Easy to use for synchronization (start with four consecutive “0”).

Output Data

Adapted to DMUX mode to have validation at full datarate in each mode.
Same data between port A and Port B in DMUX 1:2 mode
Parity Bit (PC) handled like other bits (no parity calculation) during Test mode.

Figure 4-1. Alignment Pattern Timing Diagram



4.6 Sampling Delay adjust (SDA)

Sampling delay adjust (SDA pin) allows to tune the sampling ADC aperture delay (TA) around its nominal value.

This feature is particularly interesting for interleaving ADCs to increase sampling rate.

This function can be activated either by external command or the 3WSI.

4.6.1 Sampling Delay adjust (SDA) function with the external command (SDA pin)

This functionality is enabled thanks to the SDAEN_n signal, which is active at low level (when tied to ground) and inactive at high level (10 KΩ to Ground, or tied to V_{CC3} = 3.3V, or left floating).

The coding table for the SDAEN_n is given in Table 4-8.

Table 4-8. SDAEN_n Coding

Function	Logic Level	Electrical Level	Description
SDAEN_n	0	10 Ω to ground	Sampling delay adjust enabled
	1	10 KΩ to ground	Sampling delay adjust disabled
		N/C	

Description :

With the external command (SDA pin), it is possible to tune the sampling ADC aperture delay by applying a control voltage on SDA pin.

Typical tuning range is from 0 to 30 ps for applied control voltage varying between ± 0.5V around 2*Vcc3/3.on SDA pin.

This tunable delay is in addition to the default value for coarse SDA fixed in the 3WSI register (~60 ps).

If not used, this function should be disabled via SDAEN_n set to high level.

4.6.2 Sampling Delay adjust (SDA) function with 3WSI interface

This mode is selectable when 3WSI interface (Mode_n = 0) is activated and when the bit D1 (SDAEN_n) of the stare register is set to 0.

Please refer to State register coding for more details in Section 4.12 ”ADC 3WSI Description (ADC Controls)” on page 29.

Description

Table 4-9. SDA Register Mapping (Address 0011)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NC	NC	SDA coarse<1:0>		SDA fine <7:0>							

Table 4-10. SDA Register Description

Description	Default register Value	Default parameter value	Register value for Max Value	Parameter Max Value	Register value for Min Value	Parameter Min Value	Step
Sampling Delay Adjust coarse	0x02	60 ps	0x03	90 ps	0x00	0 ps	30 ps
Sampling Delay Adjust fine	0x00	0 ps	0xFF	30 ps	0x00	0 ps	120 fs

Total SDA delay is given by SDA coarse value in addition to SDA fine value.
SDA coarse register [1:0] allows a variation step of 0, 30 ps, 60 ps or 90 ps.
SDA fine register [7:0] allows a fine step of 120fs between a range of 0 to 30 ps

So the Sampling Delay adjusts with the 3WSI interface could vary from 0 ps up to 120 ps with a step of 120 fs.

4.7 Gain Adjust (GA) Function

This function allows adjusting ADC Gain so that it can always be tuned to 1.0
This function could be activated either by external command or the 3WSI.

4.7.1 Gain Adjust Function with the External Command (GA Pin)

The ADC Gain can be tuned by ±10% by tuning the voltage applied on GA by ± 0.5V around $2*V_{CC}/3$.

4.7.2 Gain Adjust Function with the 3WSI

This mode is selectable when 3WSI interface (Mode_n = 0) is activated.

Please refer to State register coding for more details in Section 4.12 ”ADC 3WSI Description (ADC Controls)” on page 29.

Description

Table 4-11. GA Register Mapping (Address 0001)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		GA<9:0>									

The ADC Gain can be tuned by ±10% by step of 0.8LSB.

Table 4-12. GA Register Description

Description	Default register Value	Default parameter value	Register value for Max Value	Parameter Max Value	Register value for Min Value	Parameter Min Value	Step
GA register <9:0>	0x200	1 (500mVpp 4096 LSB)	0x3FF	1.10 (550 mVpp 4506 LSB)	0x000	0.90 (450mVpp 3686 LSB)	0.0002 (0.097mV 0.8LSB)

4.8 Offset Adjust (OA) Function

This function allows to adjust ADC Offset so that it can always be tuned to mid-code 2048.
This function could be activated either by external command or the 3WSI.

4.8.1 Offset Adjust Function with the External Command (OA Pin)

The ADC Offset can be tuned by ±195 LSB (± 23.8 mV) by tuning the voltage applied on OA by ± 0.5V around $2*V_{cc3}/3$.

$2*V_{cc3}/3+0.5V$ gives the most negative offset variation and $2*V_{cc3}/3-0.5V$ gives the most positive offset variation.

4.8.2 Offset Adjust Function with the 3WSI

This mode is selectable when 3WSI interface (Mode_n = 0) is activated.
Please refer to State register coding for more details in Section 4.12 ”ADC 3WSI Description (ADC Controls)” on page 29.

Description

Table 4-13. OA Register Mapping (Address 0010)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		OA<9:0>									

The ADC offset can be tuned by ±195LSB by step of 0.38LSB.

Table 4-14. OA Register Description

Description	Default register Value	Default parameter value	Register value for Max Value	Parameter Max Value	Register value for Min Value	Parameter Min Value	Step
Offset Adjust	0x200	0 LSB	0x000	+195 LSB (+23.8 mV)	0x3FF	–195 LSB (–23.8 mV)	0.38 LSB (0.046 mV)

4.9 HSR (High Sampling Rate) Function

This function is only selectable via the 3WSI.

Please refer to State register coding for more details in Section 4.12 ”ADC 3WSI Description (ADC Controls)” on page 29.

In DMUX1:1 it allows to output data faster up to 1 GHz instead of half speed (by default) by increasing current of output stages.

Note: There is a small consumption increase.

4.10 RES Function

This function is only selectable via the 3WSI.

Please refer to State register coding for more details in Section 4.12 ”ADC 3WSI Description (ADC Controls)” on page 29.

This function allows changing the active edge of the SYNC signal

4.11 TRIGGER Function

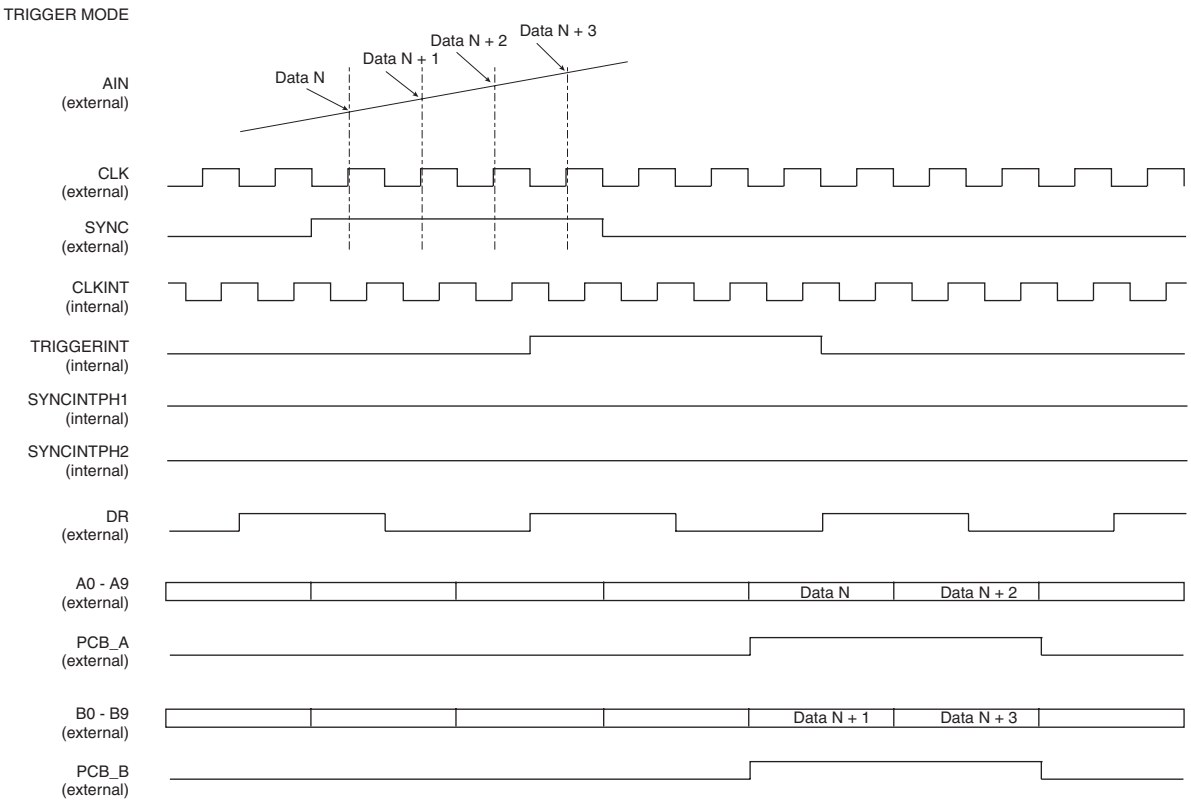
This function is only selectable via the 3WSI.

Please refer to State register coding for more details in Section 4.12 on page 29.

This function allows to help to synchronise multiple ADCs.

The pulse applied on SYNC is outputted after pipeline on the Parity Check pins (PCB_A) & (PCB_B) in DMUX 1:2.

Figure 4-2. Trigger Mode Diagram



4.12 ADC 3WSI Description (ADC Controls)

The digital interface of the ADC is activated via the mode_n signal (active low).

4.12.1 3WSI Timing Description

The 3WSI is a synchronous write only serial interface made of 4 wires:

- “reset_n” : asynchronous 3WSI reset, active low
- “sck” : serial clock input
- “sld_n ” : serial load enable input
- “mosi” : serial data input.

The 3WSI gives a “write-only” access to up to 16 different internal registers of up to 12 bits each. The input format is fixed with always 4 bits of register address followed by always 12 bits of data. **Address and data are entered MSB first.**

The write procedure is fully synchronous with the clock rising edge of “sclk” and described in the write chronogram hereafter.

“sld_n” and “mosi” are sampled on each rising clock edge of “sclk” (clock cycle).
“sld_n” must be set at “1” when no write procedure is done.

A write starts on the first clock cycle with “sld_n” at “0”. “sldn” must stay at “0” during the complete write procedure.

In the first 4 clock cycles with “sld_n” at “0”, 4 bits of register address from MSB (a[3]) to LSB (a[0]) are entered.

In the next 12 clock cycles with “sld_n” at “0”, 12 bits of data from MSB (d[11]) to LSB (d[0]) are entered.

This gives 16 clock cycles with “sld_n” at “0” for a normal write procedure.

A minimum of one clock cycle with “sld_n” returned at “1” is requested to end the write procedure, before the interface is ready for a new write procedure.

Any clock cycle with “sld_n” at “1” before the write procedure is completed interrupts this procedure and no data transfer to internal registers is done.

Additional clock cycles with “sld_n” at “0” after the parallel data transfer to the register (done at 15tth consecutive clock cycle with “sld_n” at “0”) do not affect the write procedure and are ignored.

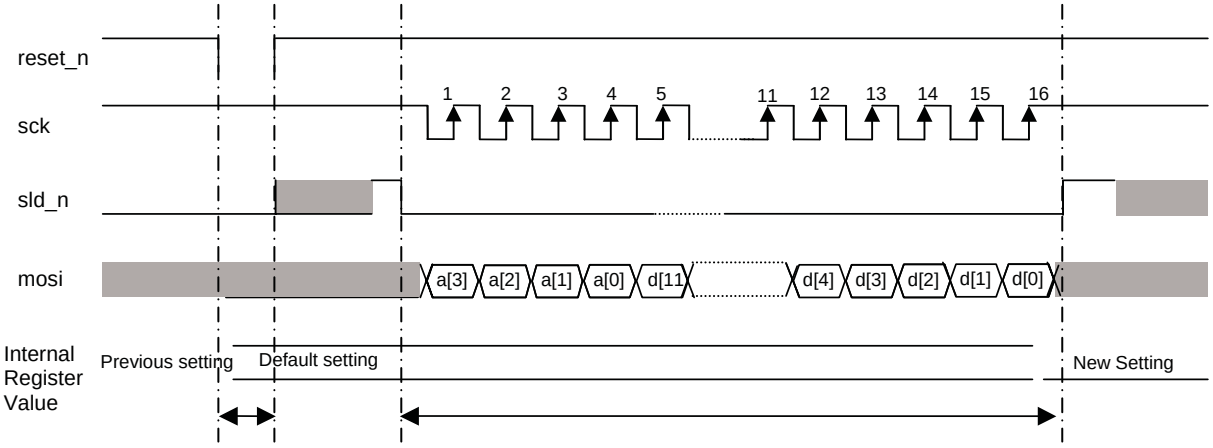
It is possible to have only one clock cycle with “sld_n” at “1” between two following write procedures.

12 bits of data must always be entered even if the internal addressed register has less than 12 bits. Unused bits (usually MSB’s) are ignored. Bit signification and bit position for the internal registers are detailed in the chapter “Registers”.

The “reset” pin combined with the “sld_n” pin can be used as a reset to program the chip to the “reset setting”.

- “reset_n” high: no effect
- “reset_n” low and “sld_n” low: programming of registers to default values

Figure 4-3. 3WSI Timing Diagram



Timings related to 3WSI are given in the table below

Table 4-15. 3WSI Timings

Name	Parameter	Min	Typ	Max	Unit	Note
Tsck	Period of sck	10			ns	
Twsck	High or low time of sck	5			ns	
Tssld_n	Setup time of sldn before rising edge of sck	4			ns	
Thsld_n	Hold time of sld_n after rising edge of sck	2			ns	
Tsmosi	Setup time of mosibefore rising edge of sck	4			ns	
Thmosi	Hold time of sdata after rising edge of sck	2			ns	
Twlreset_n	Minimum low pulse width of reset	5			ns	
Tdreset_n	Minimum delay between an edge of reset and the rising edge of sck	10			ns	

4.12.2 3WSI: Address and Data Description

This 3WSI is activated with the control bit sld_n going low (please refer to “write timing” in next section).
The length of the word is 16 bits: 12 for the data and 4 for the address.
The maximum serial logic clock frequency is 100 MHz.

Table 4-16. Registers Mapping

Address	Label	Description	Default Setting
0000	State Register	DMUX ratio Selection Sampling Delay Adjust Enable Test Mode Enable Output clock division ratio selection Trigger mode selection	0x7FF
0001	GA Register	Gain adjust register	0x200
0010	OA Register	Offset adjust register	0x200
0011	SDA Register	Sampling delay adjust register	0x002
0100	SA	reserved	0x1F
0101	Test Register	Test modes register	0x03
0110		reserved	
0111		reserved	
1000 to 1111		reserved	

4.12.3 State Register (Address 0000)

Table 4-17. State Register Mapping (Address 0000)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
reserved			TRIG_SEL_N	RES	HSR	reserved			TM_n	SDAEN_n	RS

Table 4-18. State Register Coding (Address 0000)

Label		Coding	Description	Default Value
RS	D0	0	1:1 DMUX mode	1
		1	1:2 DMUX mode	
SDAEN_n	D1	0	Sampling Delay Adjust function Enabled	1
		1	Sampling Delay Adjust function Disabled	
TM_n	D2	0	Test Mode ON (refer to register at address 0101)	1
		1	Test Mode OFF	
reserved	D3	1	Should be connected to 1	1
reserved	D4	1	Should be connected to 1	1
reserved	D5	1	Should be connected to 1	1
HSR	D6	0	Full Sampling rate mode in 1:1 DMUX Mode ON	1
		1	Half Sampling rate mode in 1:1 DMUX Mode ON	
RES	D7	0	RESET edge select: rising edge	1
		1	RESET edge select: falling edge	

Table 4-18. State Register Coding (Address 0000) (Continued)

Label		Coding	Description	Default Value
TRIG_SEL_N	D8	0	Trigger mode (Trigger pulse on PCB_X if positive pulse on SYNC. Internal synchronization inhibited, where X = A or B)	1
		1	Synchronization mode (Synchronization of internal functions on positive pulse on SYNC)	
reserved	D9			1
reserved	D10			1
reserved	D11			1

Notes: 1. HSR: when the digital interface is not active, default mode is DMUX 1:1 at half sampling speed. When HSR is set to 0, power consumption will slightly increase in order to allow for 1 GSps operation in DMUX 1:1.
2. Test pattern function “Always running” : Internal synchronization not affected by mode (TM_n) change.
3. Bit D3, D4, D5, D9, D10, D11 are reserved.
4. Synchronization and Trigger modes

4.12.4 GA Register (Address 0001)

Table 4-19. GA Register Mapping (Address 0001)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		GA<9:0>									

4.12.5 OA Register (Address 0010)

Table 4-20. OA Register Mapping (Address 0010)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		OA<9:0>									

4.12.6 SDA Register (Address 0011)

Table 4-21. SDA Register Mapping (Address 0011)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		SDA coarse<1:0>		SDA fine <7:0>							

4.12.7 SA Register (Address 0100)

Table 4-22. SA Register Mapping (Address 0100)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							SA<4:0>				

Note: Reserved register.

Table 4-23. Registers 0001 to 0100 Summary

Address	Description	Default register Value	Default parameter value	Register value for Max Value	Parameter Max Value	Register value for Min Value	Parameter Min Value	Step
0001	Gain Adjust	0x200	1 (500mVpp 4096 LSB)	0x3FF	1.10 (550 mVpp 4506 LSB)	0x000	0.90 (450mVpp 3686 LSB)	0.032 (0.195mV 1.6LSB)
0010	Offset Adjust	0x200	0 LSB	0x000	+128 LSB (+15.6 mV)	0x3FF	–128 LSB (–15.6 mV)	0.25 LSB (0.03 mV)
0011	Sampling Delay Adjust coarse	0x02	60 ps	0x03	90 ps	0x00	0 ps	30 ps
	Sampling Delay Adjust fine	0x00	0 ps	0xFF	30 ps	0x00	0 ps	120 fs
0100	SA(1)	0x1F	NA	NA	NA	NA	NA	NA

Note: 1. Reserved register.

4.12.8 Test Register (Address 0101)

Table 4-24. Test Register Mapping (Address 0101)

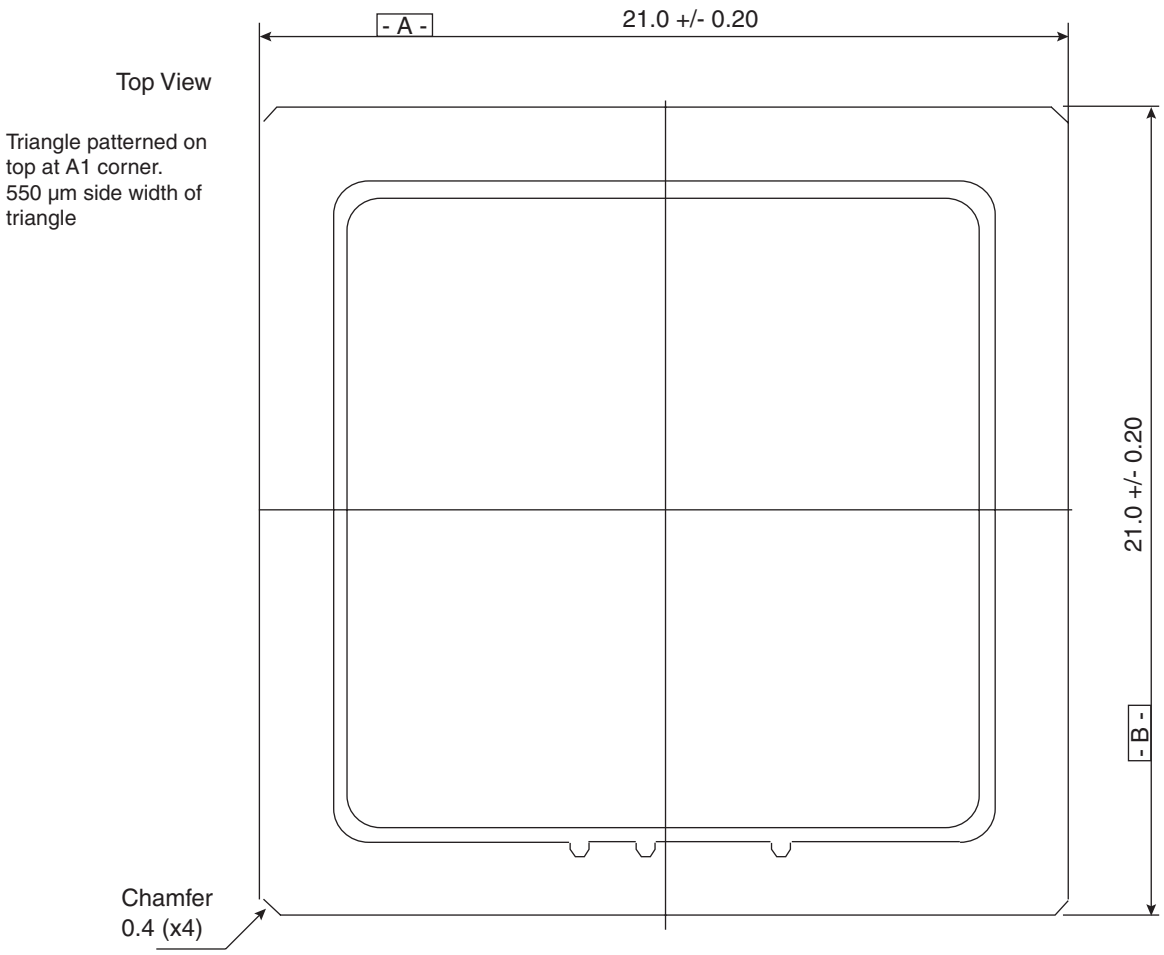
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
<Unused>										TEST TYPE	

5. Package Description

5.1 CLGA255 Outline

5.1.1 Top View

Figure 5-1. Ci-CGA255 Top View

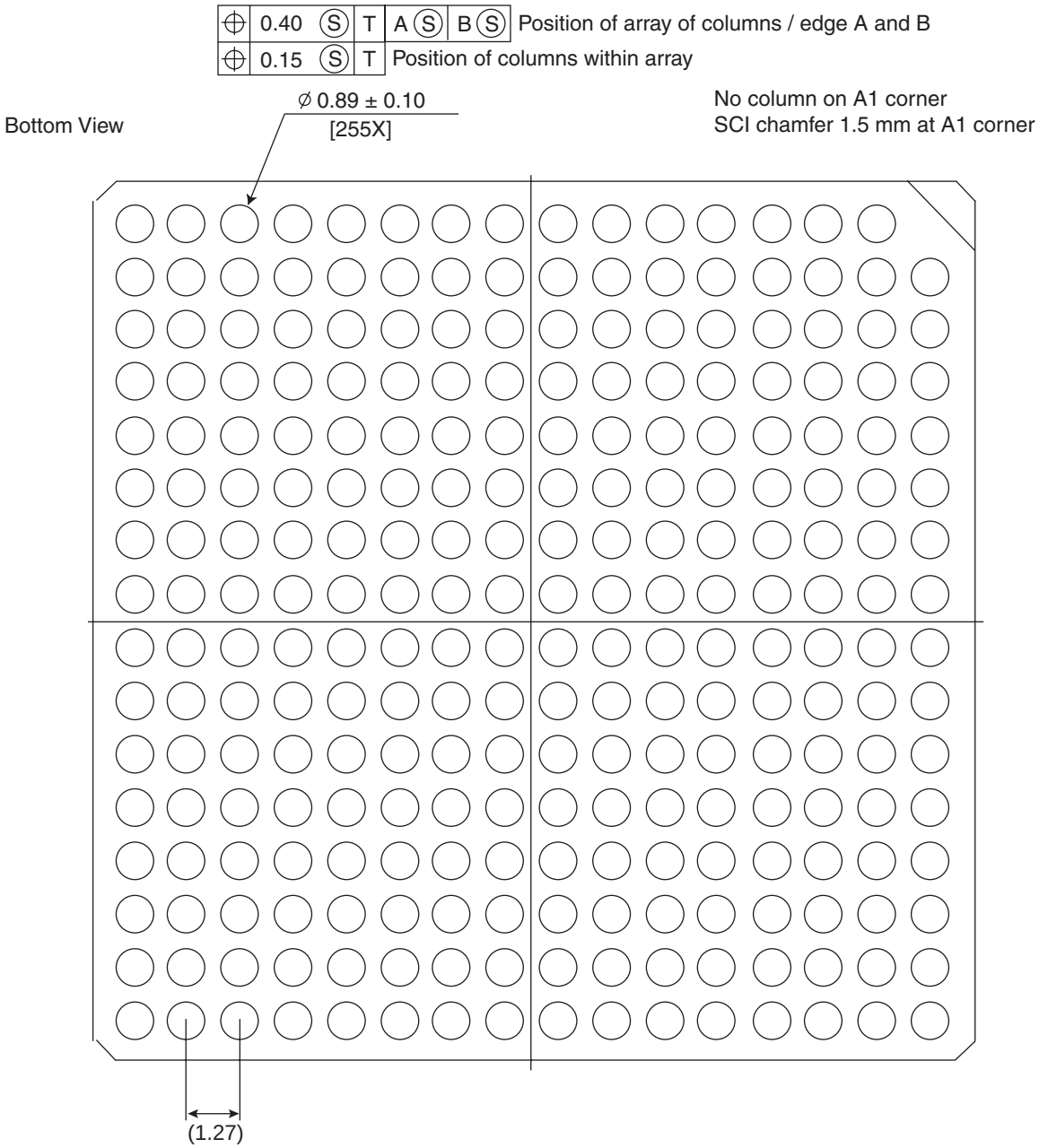


All units in mm

Sealring is connected to AGND

5.1.2 Bottom View

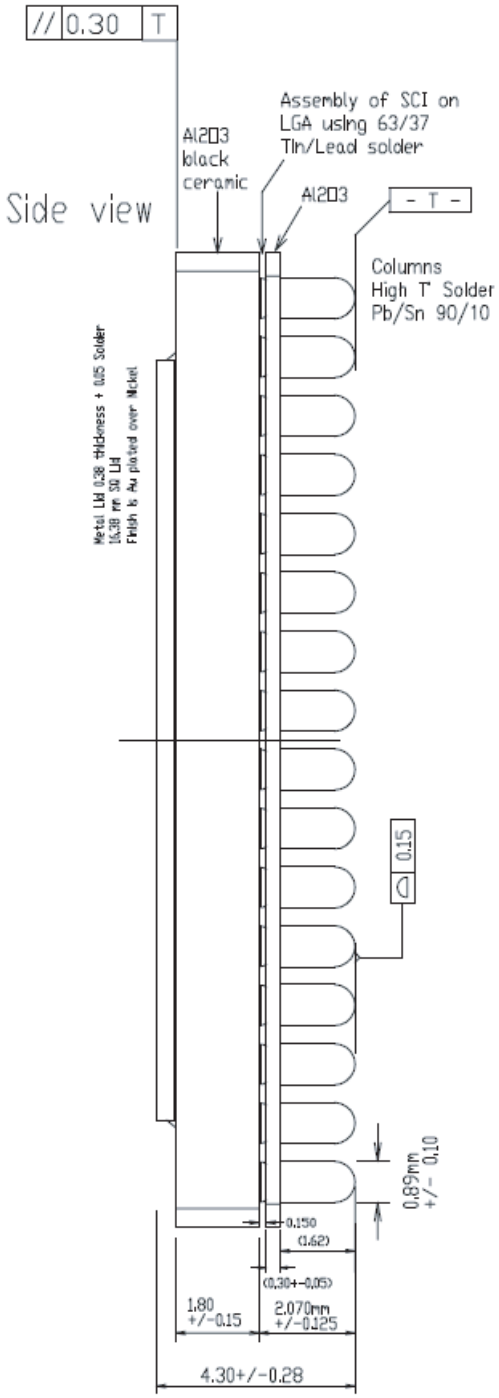
Figure 5-2. Ci-CGA255 Bottom View



All units in mm

5.1.3 Side View

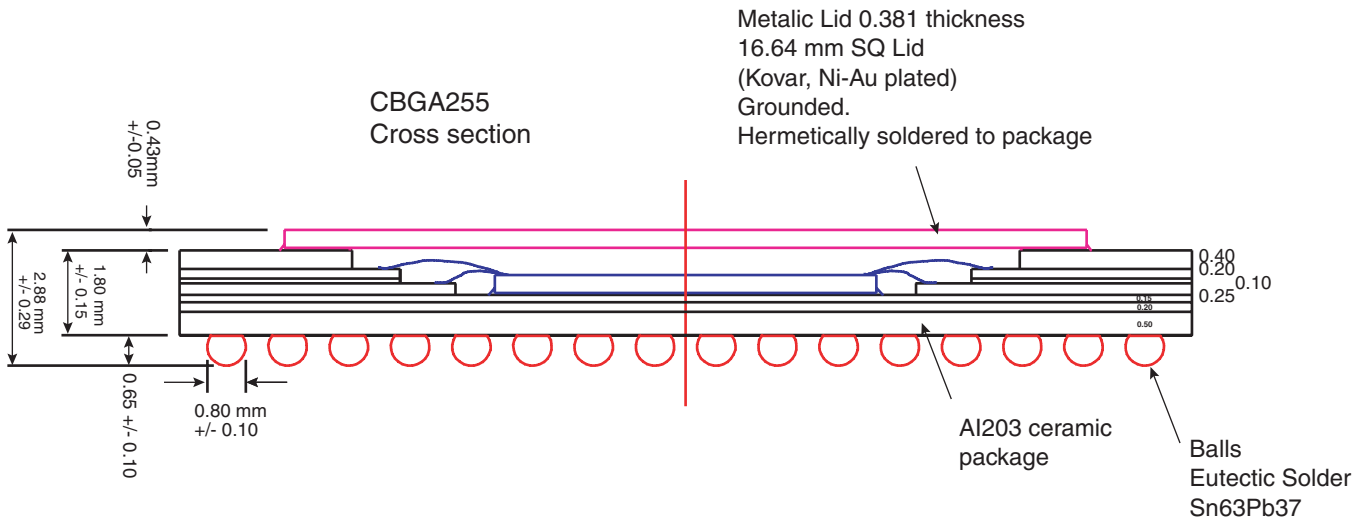
Figure 5-3. Ci-CGA255 Side View



All units in mm

5.1.4 Cross Section

Figure 5-4. Ci-CGA255 Cross Section



All units in mm.

Die backplane is connected to AGND

5.1.5 Thermal Characteristics of CI-CGA255

Assumptions:

- Die thickness = 300µm
- No convection
- Pure conduction
- No radiation
  - Rth Junction -bottom of columns (NTK SCI - 0.89 mm diameter) = 9.68°C/W
  - Rth Junction -bottom of columns (6Sigma Column array - 0.508 mm diameter) = 11.43°C/W
  - Rthj-top of lid = 15°C/W
  - Rthj-board (JEDEC JESD51-8) = 13°C/W (board size = 39 x 39 mm, 1.6 mm thickness)

Assumptions:

- Convection according to JEDEC
- Still air
- Horizontal 2s2p board
  - Rth-j-a (JEDEC) = 25.3°C/W (board size 114.3 x 76.2 mm, 1.6 mm thickness)

Assumptions:

- Convection according to JEDEC, except larger board dimensions and one additional copper plane
- Still air
- Horizontal 2s3p board
  - Rth-j-a (JEDEC) = 18.9°C/W (board size 260 x 220 mm, 1.6 mm thickness)

6. Ordering Information

Table 6-1. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
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EV12AS200GS-EB	CI CGA 255	Ambient	Prototype	Evaluation board

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