

## PE99153

### Hi-Rel 6A DC-DC Converter

### Radiation Tolerant UltraCMOS® Monolithic Point-of-Load Synchronous Buck Regulator with Integrated Switches

#### Features

- Up to 6A continuous
- Output voltage range from 1.0–3.6V by external select resistors
- Input voltage range 4.6–6.0V
- Current mode control, pulse-by-pulse current limit, current sharing enabled and (N+K) redundancy compatible shutdown mode
- SYNC function, 100 kHz–5 MHz lock range with selectable 500 kHz / 1 MHz free running frequency
- Shutdown pin, Power Good output pin for supply sequencing
- Better than 1% typical initial accuracy (+25 °C)
- Control inputs compatible with TTL, LVTTTL, LVCMOS (2.5V and 3.3V) and 5V CMOS
- Available in ceramic hermetic packaging and in bare die form

### Product Description

The PE99153 is a radiation tolerant point-of-load buck regulator delivering high efficiency at  $V_{IN} = 5V$  and output currents up to 6A continuous. This single-chip solution is perfect for Hi-Rel applications and delivers peak efficiency exceeding 93%. A minimal external component count and high switching frequency enables  $>10 W/in^2$  standard PCB designs while high efficiency minimizes thermal concerns. All power switching devices are integrated on-chip.

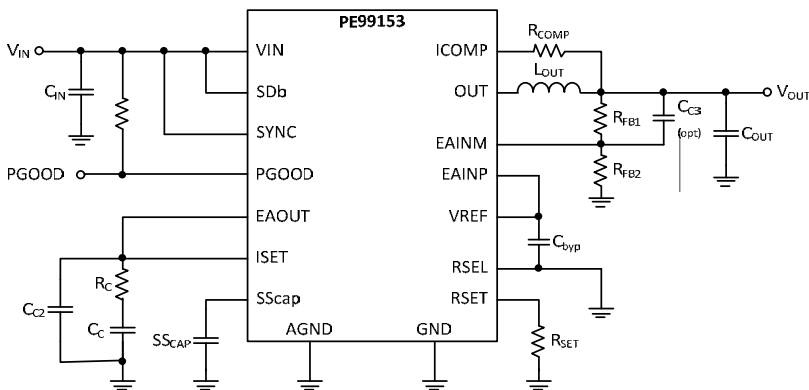
Fabricated in Peregrine’s patented UltraCMOS® technology, the PE99153 offers excellent power efficiency and intrinsic radiation tolerance.

**Table 1. Radiation Performance**

TID	100 kRad(Si)
SEL	$> 90 MeV \cdot cm^2/mg$
SEB	$> 90 MeV \cdot cm^2/mg$
SET	$> 90 MeV \cdot cm^2/mg$
SEFI	$> 90 MeV \cdot cm^2/mg$
SEGR	$> 90 MeV \cdot cm^2/mg$

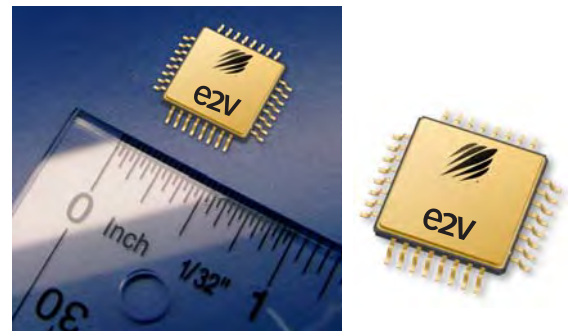
SEL, SEB, SEGR, SEU, SEFI: None observed, Au/60 degrees  
 SET: No events exceeding 30 mV transient observed @ Au,  
 LET=90, 60 degrees and normal incidence

**Figure 1. Typical Application Diagram**



**Figure 2. Package Type**

32-lead ceramic quad flat package



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**Table 2. Electrical Specifications**

Case Temp ( $T_c$ ) =  $-55\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ ,  $V_{IN} = 4.6\text{--}6.0\text{V}$ ,  $V_{OUT} = 1.0\text{--}3.6\text{V}$  (except as noted\*)

Parameter	Condition	Min	Typ	Max	Unit
Synchronous Frequency Range, <b>Fsw_range</b>		0.1		5	MHz
Maximum cycle-averaged RMS output current, <b>I<sub>max</sub></b>		6			A
Supply current (shutdown), <b>IDDS</b>	SDB = GND, $V_{IN} = 5.5\text{V}$		2	6	mA
	SDB = GND, $V_{IN} = 6.0\text{V}$		0	9.5	mA
Supply current (no-load, 1 MHz async), <b>IDDO</b>				55	mA
High side on resistance, <b>R<sub>on,hss</sub></b>	Test current = 100 mA		50	105	mΩ
Low side on resistance, <b>R<sub>on,lss</sub></b>	Test current = 100 mA		50	110	mΩ
<b>Output Voltage</b>					
Reference voltage accuracy, <b>V<sub>ref</sub></b> *	$V_{IN} = 5.0\text{V}$ , $I_{OUT} = I_{max}/2$ , $-55 \leq T_c \leq +125\text{ }^{\circ}\text{C}$ , Fsw = 100 kHz–1 MHz	-1.50	0	1.50	%
	$V_{IN} = 5.0\text{V}$ , $I_{OUT} = I_{max}/2$ , Fsw = 100 kHz–1 MHz (100 kRad post rad, $T_c = 25\text{ }^{\circ}\text{C}$ )	-1.50	0	1.50	%
Reference voltage line regulation, <b>K<sub>vi</sub> (steady state)</b>	$4.6\text{V} \leq V_{IN} \leq 6.0\text{V}$ , $I_{OUT} = 3\text{A}$ , $V_{OUT} = 2.5\text{V}$ , Fsw = 1 MHz	-0.20	0	0.20	%
Reference voltage load regulation, <b>K<sub>vo</sub> (steady state)</b>	$V_{IN} = 5.0\text{V}$ , $500\text{ mA} \leq I_{OUT} \leq 3\text{A}$ , $V_{OUT} = 2.5\text{V}$ , Fsw = 1 MHz	-0.25	0	0.25	%
<b>Internal Oscillator and SYNC Capture</b>					
Internal oscillator frequency, <b>FOSC_FREQ</b>	SYNC = GND	336	550	690	kHz
	SYNC = Open or $V_{IN}$	0.740	1.10	1.31	MHz
Internal oscillator duty cycle, <b>FOSC_DC</b>		46		54	%
Min SYNC lock capture frequency, <b>Sync_lock</b>		40			kHz
External SYNC duty cycle, <b>SYNC_DC</b>		40		60	%
<b>Current Limiting and Current Mode Control Loop</b>					
Internal current limit max, <b>ILIMXINT</b>	$V_{OUT} = 1.0\text{V}$ , ISET = 3.0V, ICOMP = 0V, RSEL pin shorted to ground, not min-on-time limited & Fsw = 500 kHz	6	8	9.5	A
Externally set max current limit accuracy, <b>ILIMXEXT</b>	$V_{OUT} = 1.0\text{V}$ , RSET = 82Ω, ISET = 3.0V, ICOMP = 0V, RSEL = $V_{IN}$ , not min-on-time limited. Fsw = 500 kHz	6	8	9.5	A
Maximum voltage across R <sub>SET</sub> , <b>V<sub>MAXRSET</sub></b>		1.35	1.55	1.80	V
$I_{out}/I_{rset}$ , <b>G<sub>iref</sub></b>	$I_{OUT}$ set for 50% rated current	350	450	550	A/A
ICOMP cap, <b>CICOMP</b>			110		pF
Current compensation gain, ICOMP gain, <b>G<sub>icomp</sub></b>		4.3	6.5	8.7	A/V

Note: \*Parameter is tested in production at  $-55\text{ }^{\circ}\text{C}$ ,  $+25\text{ }^{\circ}\text{C}$  and  $+125\text{ }^{\circ}\text{C}$ , and guaranteed through characterization at  $-40\text{ }^{\circ}\text{C}$  and  $+85\text{ }^{\circ}\text{C}$ .

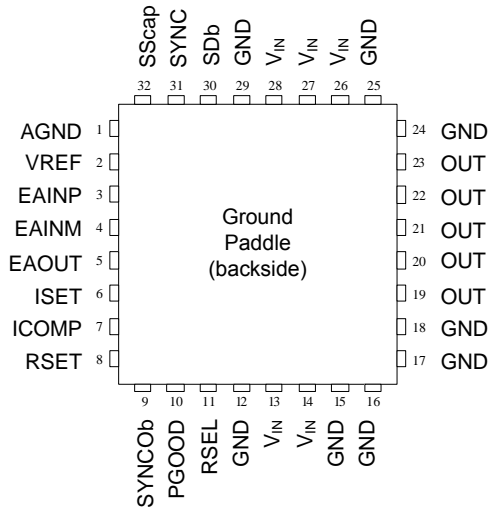
**Table 2. Electrical Specifications (Cont.)**

**Case Temp ( $T_c$ ) = -55 °C to +125 °C,  $V_{IN}$  = 4.6–6.0V,  $V_{OUT}$  = 1.0–3.6V (except as noted\*)**

PGOOD					
PGOOD threshold	EAINM_UP_THRESH entering PGOOD window (% of Vref)	104	110.5	117.5	%
	EAINM_LO_THRESH exiting PGOOD window (% of Vref)	84	90	96	%
PGOOD hysteresis	EAINM_UP (% of Vref)		2		%
	EAINM_LO (% of Vref)		1.7		%
PGOOD low sink current, <b>PGOOD I_OL</b>	$V_{PGOOD} = 0.4V$	4	8		mA
PGOOD high leakage current, <b>PGOOD I_OH</b>	$V_{PGOOD} = V_{IN}$		10	20	μA
PGOOD de-glitch time			64		SYNCOB cycles
Error Amp					
EAINM leakage	Measured at 1V input			0.2	μA
EAINP leakage	Measured at 1V input			0.2	μA
EAOUT source current	Measured at 1V input	-445	-350	-270	μA
EAOUT sink current	Measured at 1V input	125	220	270	μA
Error amplifier transconductance	EAOUT = 1.5V DC	0.7	1.4	2.1	mS
Error amplifier output resistance		4	6.4	10	MΩ
EA input offset	1 MHz internal	-6	3.1	6	mV
Undervoltage Lockout					
Under-voltage lockout	$V_{IN}$ rising**	3.5	4.2	4.59	V
	$V_{IN}$ falling	3.4	3.8	4.1	V
	$V_{IN}$ falling (100 kRad post rad, $T_c = +25$ °C)			4.2	V
Under-voltage lockout hysteresis			400		mV
Soft Start					
SScap pin pull-up resistance	$V_{SScap} = 0V$		1.2		MΩ
Internal <b>SSCAP</b>			16		pF
Vref track, <b>V_SScap - Vref_ext</b>	$V_{SScap} = 0.5V$	-170	0	170	mV
DC Characteristics					
SDB turn-on threshold	$V_{IH}$	2			V
	$V_{IL}$			1.3	V
SYNCOB low sink current, <b>SYNCOB I_OL</b>	$V_{SYNCOB} = 0.4$	4	8		mA
SYNCOB high leakage current, <b>SYNCOB I_OH</b>	$V_{SYNCOB} = V_{IN}$		9.6	20	μA
SYNC	$V_{IH}$	2.2			V
	$V_{IL}$			1.25	V
HSS leakage	$V_{OUT} = V_{SDB} = 0V$	-1.6	-0.01		mA
	$V_{OUT} = V_{SDB} = 0V$ (100 kRad post rad, $T_c = 25$ °C)	-4			mA
LSS leakage	$V_{OUT} = V_{IN}, V_{SDB} = 0V$		0.3	1.8	mA
Thermal					
Theta_JC	Junction to back side paddle		3		°C/W

Note: \*\*Not production tested at -55°C

Figure 3. Package Pin Layout (Top View)



Package Mechanical Details

500 mil x 500 mil CQFP hermetic with gullwing leads  
32 pins, 50-mil lead pitch  
Alumina body, Kovar lid

Table 3. Pin Descriptions

Pin #	Pin Name	Description
1	AGND	Analog ground
2	VREF	1.000V reference output, loop to EAINP additional low pass filtering may be necessary
3	EAINP	Error amplifier (+) input, loop to VREF
4	EAINM	Error amplifier (-) input, load feedback
5	EAOUT	Error amplifier output/loop to ISET
6	ISET	Current setpoint input/loop to EAOUT
7	ICOMP	Variable current compensation/resistor to V <sub>OUT</sub>
8	RSET	Resistor to set reference current
9	SYNCOB	Loophrough complement output
10	PGOOD	Power good flag output
11	RSEL	Reference resistor selection
12, 15, 16, 17, 18, 24, 25, 29	GND	Input power/signal ground
13, 14, 26, 27, 28	V <sub>IN</sub>	Input power supply
19, 20, 21, 22, 23	OUT	Switch power output
30	SDb	Shutdown (L)/enable input
31	SYNC	Oscillator sync input or int. osc freq select
32	SScap	Soft start timing cap input
Paddle	GND	Ground for proper operation

Table 4. Operating Ranges\*

Symbol	Parameter/Condition	Min	Max	Unit
V <sub>IN</sub>	Power supply voltage	4.6	6.0	V
T <sub>C</sub>	Operating temperature range (case)	-55	125	°C

Note: \*Operation should be restricted to the limits in the Operating Ranges table. V<sub>in</sub> recommended maximum slew rate is 100 V/s. Refer to application note TDAPN9915x.

Table 5. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V <sub>IN</sub>	Power supply voltage	-0.5	6.5	V
T <sub>J</sub>	Operating temperature range (junction)	-55	+145	°C
Θ <sub>JC</sub>	Theta JC		3	°C/W
T <sub>ST</sub>	Storage temperature range (case)	-65	+150	°C
I <sub>I</sub>	DC into any signal input	-10	10	mA
I <sub>O</sub>	DC into any signal output	-50	50	mA
I <sub>P</sub>	DC into any <i>single</i> power pin	-2	2	A

Exceeding absolute maximum ratings may cause permanent damage. Operation between maximum operating ranges and absolute maximum operating ranges for extended periods may reduce reliability.

Table 6. Electrostatic Discharge (ESD) Ratings

Model	Parameter/Condition	Min	Max	Unit
HBM	V <sub>ESD</sub> All pins*		1000	V

Note: \* Human Body Model ESD Voltage (HBM, MIL\_STD 883 Method 3015.7).

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

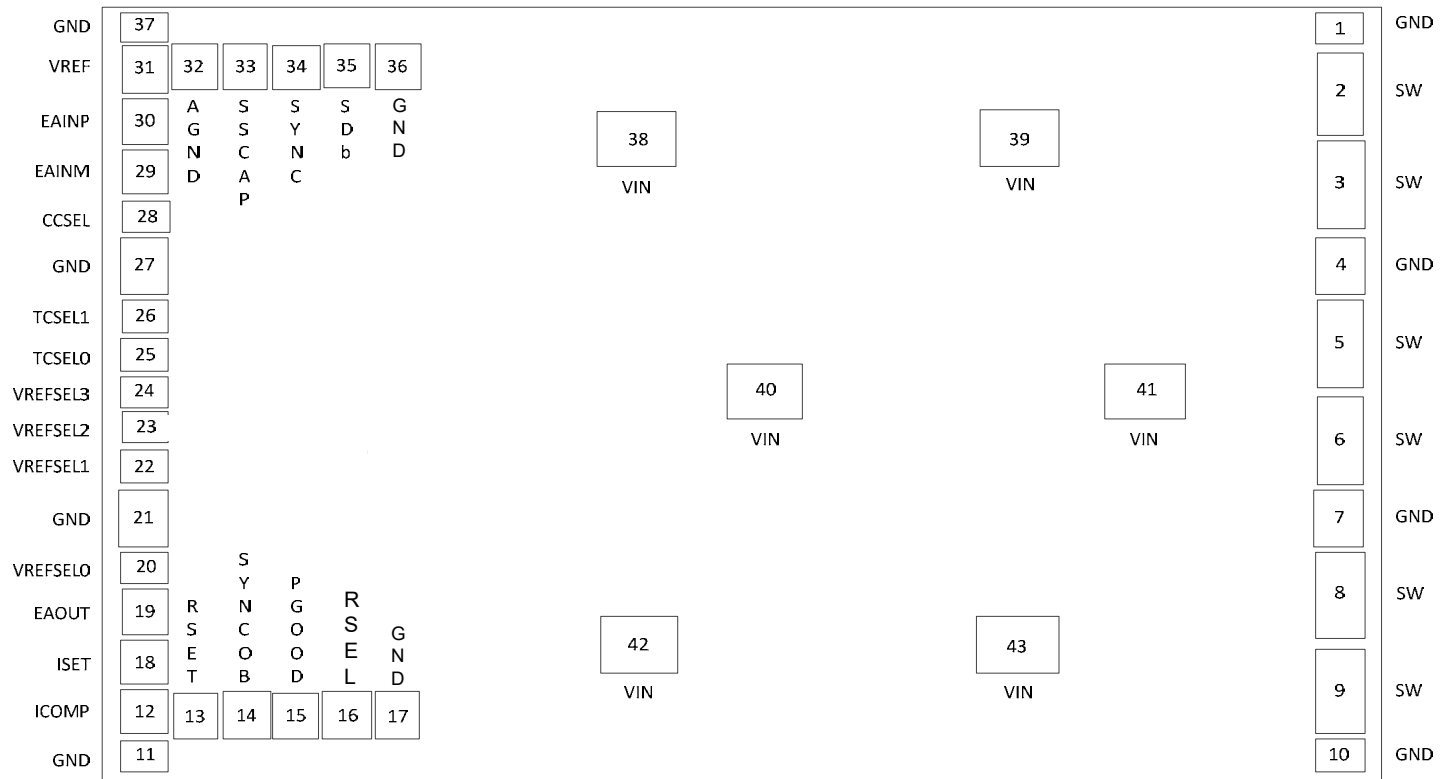
Latch-Up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

ELDRS

The UltraCMOS process does not exhibit enhanced low-dose-rate sensitivity (ELDRS) since bipolar minority carrier elements are not used.

**Figure 4. Die Pad Layout (Top View)\***



Note: \* All pin locations originate from the die center and refer to the center of the pin.

**Table 7. Die Pad Coordinates and Descriptions**

Pin No.	Pin Name	X	Y	Description
1	GND	2385.9	1433.4	Ground
2	SW	2366.9	1179.65	Switch
3	SW	2366.9	810.35	Switch
4	GND	2365.9	500	Ground
5	SW	2366.9	189.65	Switch
6	SW	2366.9	-189.65	Switch
7	GND	2365.9	-500	Ground
8	SW	2366.9	-810.35	Switch
9	SW	2366.9	-1179.65	Switch
10	GND	2385.9	-1433.4	Ground
11	GND	-2343.9	-1437.25	Ground
12	ICOMP	-2343.9	-1266.9	Variable Current Compensation/Resistor to VOUT
13	RSET	-2142.8	-1283.2	Resistor to Set Reference Current
14	SYNCOB	-1944.2	-1283.2	Loop-Through Complement Output

Pin No.	Pin Name	X	Y	Description
15	PGOOD	-1745.6	-1283.2	Power Good Flag Output
16	RSEL	-1547	-1283.2	Reference Resistor Selection
17	GND	-1348.4	-1283.2	Ground
18	ISET	-2343.9	-1068.3	Current Set-Point Input/ Loop to EAOUT
19	EAOUT	-2343.9	-869.7	Error Amplifier Output/ Loop ISET
20	VREFSELO	-2343.9	-696.1	Bandgap Reference Voltage Fine Adjust (0)
21	GND	-2343.9	-500	Ground
22	VREFSEL1	-2343.9	-297.3	Bandgap Reference Voltage Fine Adjust (1)
23	VREFSEL2	-2343.9	-148.7	Bandgap Reference Voltage Fine Adjust (2)
24	VREFSEL3	-2343.9	-0.1	Bandgap Reference Voltage Fine Adjust (3)

**Table 7. Die Pad Coordinates and Descriptions  
(continued)**

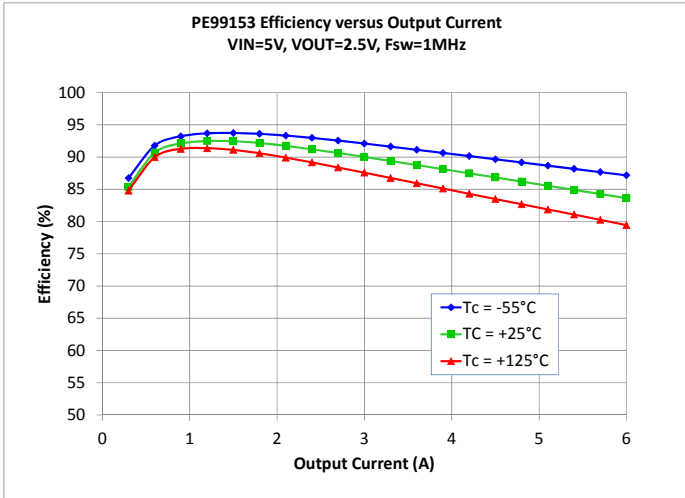
Pin No.	Pin Name	X	Y	Description
25	TCSEL0	-2343.9	148.5	Bandgap Reference Voltage Fine Adjust (0)
26	TCSEL1	-2343.9	297.2	Bandgap Reference Voltage Fine Adjust (0)
27	GND	-2343.9	500	Ground
28	CCSEL	-2343.9	696.1	Course trim code
29	EAINM	-2343.9	869.7	Error Amplifier (-) Input, Loop to VREF
30	EAINP	-2343.9	1068.3	Error Amplifier (+) Input, Load Feedback
31	VREF	-2343.9	1266.9	1.000V Reference output, Loop to EAINP. Additional Low Pass Filtering May be Necessary
32	AGND	-2142.8	1283.2	Bandgap ground
33	SScap	-1944.2	1283.2	Resistor to Set Reference Current
34	SYNC	-1745.6	1283.2	Loop-Through Complement Output
35	SDb	-1547	1283.2	Shutdown (L)/enable input
36	GND	-1348.4	1283.2	Ground
37	GND	-2343.9	1437.25	Ground
38	VIN	-397.5	1000	Input Power Supply
39	VIN	1102.5	1000	Input Power Supply
40	VIN	102.5	0	Input Power Supply
41	VIN	1602.5	0	Input Power Supply
42	VIN	-397.5	-1000	Input Power Supply
43	VIN	1102.5	-1000	Input Power Supply

**Table 8. Die Pad Bond Options**

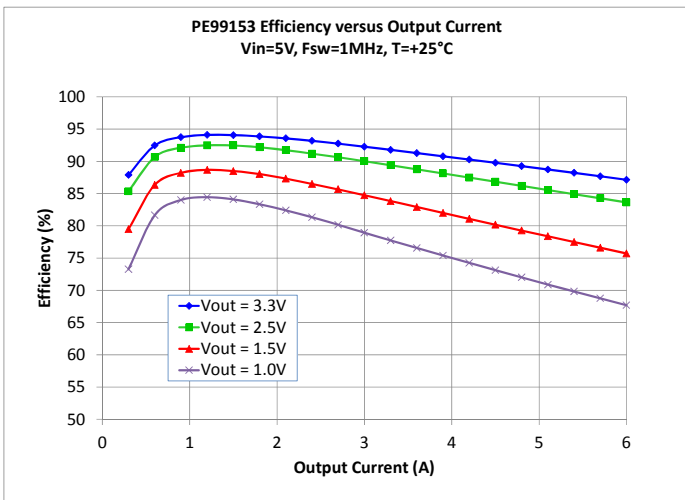
PE99153							
Bond Option	PAD 24	PAD 23	PAD 22	PAD 20	PAD 26	PAD 25	PAD 28
	VREFSEL3	VREFSEL2	VREFSEL1	VREFSEL0	TCSEL1	TCSEL0	CCSEL
A	Ground	Ground	N/C	Ground	N/C	Ground	Ground
B	Ground	Ground	N/C	N/C	N/C	Ground	Ground
C	Ground	N/C	Ground	Ground	N/C	Ground	Ground
D	Ground	N/C	Ground	N/C	N/C	Ground	Ground
E	Ground	N/C	N/C	Ground	N/C	Ground	Ground
F	Ground	N/C	N/C	N/C	N/C	Ground	Ground
G	N/C	Ground	Ground	Ground	N/C	Ground	Ground
H	N/C	Ground	Ground	N/C	N/C	Ground	Ground

**Typical Performance Characteristics**

**Figure 5. Efficiency Curves Over Output Load Current and Temperature**



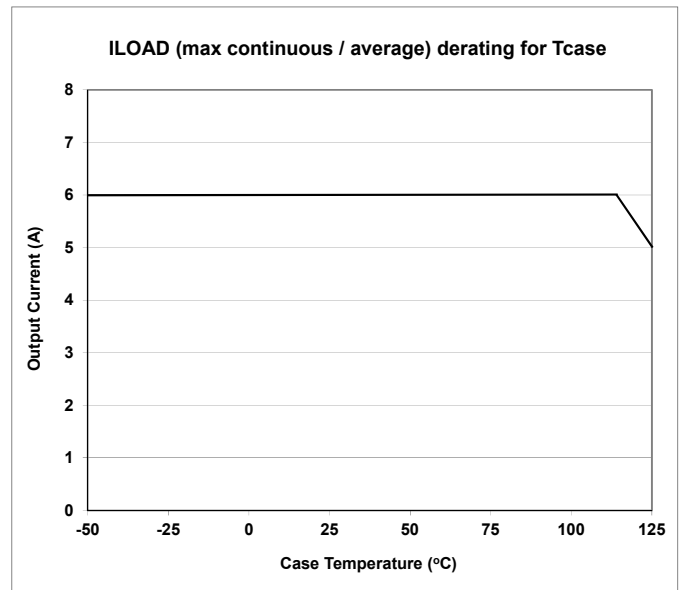
**Figure 6. Efficiency Curves Over Typical Output Voltages**



**Thermal Derating Curve**

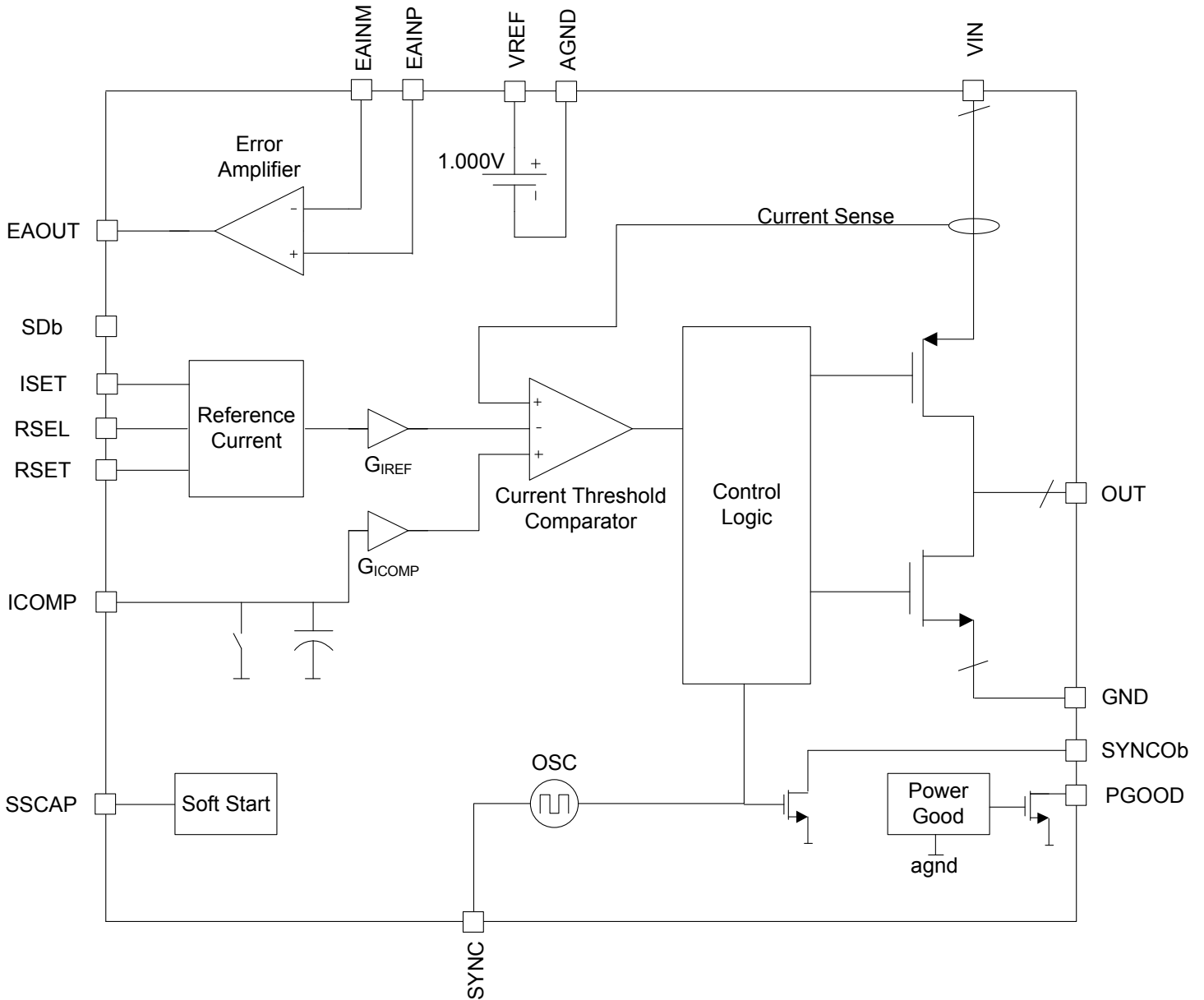
The thermal derating curve plots the case temperature against the maximum current allowed while maintaining safe electrical operation below the maximum junction temperature. Reliability guidelines require the continuous or average output current to remain below 6A at 125 °C junction temperature. At full load and 125 °C case temperature, the die temperature will exceed 125 °C. The output current should be derated starting at 114 °C case based on the specific application’s worst-case time averaged current analysis using *Figure 7*.

**Figure 7. Thermal Derating Curve**



The PE99153 meets the maximum allowable requirement of MIL-PRF-38535 ( $<2 \times 10^5$  A/cm<sup>2</sup>) by achieving a current density of  $<1.5 \times 10^5$  A/cm<sup>2</sup>.

Figure 8. Block Diagram





## Theory of Operation

### General

The PE99153 is a radiation-hardened point-of-load buck regulator. This highly integrated switching regulator contains two synchronous power switches capable of delivering up to 6A of continuous current. The PE99153 is designed to operate from a wide 5V bus and provide 1.0V to 3.6V supply rails for analog, digital and RF payloads. The internal oscillator can operate at 500 kHz or 1 MHz. Optionally, the switching frequency can be synchronized to an external reference from 100 kHz to 5 MHz. Current limiting is adjustable with an external resistor and is achieved through peak current mode control. An external resistor also provides adjustable slope compensation to optimize stability and closed loop bandwidth across output voltage and switching frequency range. Loop compensation is externally adjustable to meet application transient response while still maintaining stability requirements. The output is tri-stated when the SDb pin is low to enable hot-spare capability.

### Peak Current Mode Control Loop

The PE99153 uses a peak current mode control architecture. At the falling edge of either the internal oscillator or, if present, the external reference, the high side switch turns on. The input voltage is then connected to the load voltage through the high side switch and the inductor for a time greater than the minimum-on-time. Current in the inductor begins to ramp approximately as  $(V_{IN} - V_{OUT})/L$ . Energy is stored in the inductor during this period. As the inductor current rises, current through the high side switch is sensed and compared to a current threshold. The inductor current continues to ramp until the current threshold is reached. At this point the high side switch turns off and the low side switch turns on for at least the minimum-off-time. Energy stored in the inductor during the previous phase is discharged into the load supply rail through the low side switch and the inductor. Inductor current decreases at a rate of approximately  $V_{OUT}/L$ . The low side switch stays on until the next falling edge of the reference clock. In order to prevent unintended harmonics or spurs, the part does not exit continuous conduction mode.

Whether the current threshold was met in the previous clock cycle or not, a minimum-off-time, followed by a minimum-on-time immediately follows the falling edge of the reference clock.

While providing improved bandwidth and inherent current limiting, all current mode control switching regulators require slope compensation to ensure stability

across all application conditions. The PE99153 provides adjustable slope compensation to allow the designer to optimize transient response and stability requirements. The compensation ramp is provided through the ICOMP pin. Inboard of the ICOMP pin is the CCOMP capacitor which can be used to generate an RC compensation ramp by tying the ICOMP pin to either  $V_{OUT}$  or  $V_{IN}$  through an external resistor to produce the desired ramp. See the design guide for selection of the appropriate resistor value. The RC ramp is reset anytime the low side switch is on by a FET switch.

### Current Threshold and Over Current Protection

The current mode control threshold current is set by the ISET pin which is driven by the voltage control loop from the EAOUT pin. The PE99153 takes the voltage applied to the ISET pin, subtracts 0.7V (typ) and applies that voltage to the  $R_{SET}$  resistor. An internal  $R_{SET}$  resistor will be used if the RSEL pin is grounded or an external  $R_{SET}$  resistor connected to the RSET pin is used if the RSEL pin is tied high. The current flowing through the  $R_{SET}$  resistor is then used as a scaled current reference for the inductor current threshold comparison. The scaling ratio is defined as  $G_{REF}$  in *Table 2*.

Over current protection is achieved by limiting the maximum voltage applied to the internal or external  $R_{SET}$  resistor to the VMAXRSET value listed in *Table 2*. Thus, the current limit can be adjusted by selection of the external  $R_{SET}$  resistor. This flexibility allows characterization and testing to a high current in the lab while still limiting the current to lower level in the application.

### Voltage Control Loop

The output voltage is achieved by controlling the ISET pin. The PE99153 contains an amplifier with both of the positive and negative input terminals, EAINP and EAINM respectively, and the output terminal EAOUT all pinned out to package pins. This allows for flexible configurations of the voltage reference, error amplifier, feedback networks and the current mode control loop. In normal configuration the error amp senses the output voltage,  $V_{OUT}$ , through a resistor divider that produces a 1.000V division at the target  $V_{OUT}$ . It compares that feedback voltage to the 1.000V reference and increases the voltage applied to the ISET pin when the output voltage is low and decreases the voltage applied to the ISET pin when the output voltage is high. Loop compensation is required to attenuate the frequency content at and above the switching frequency and to achieve the desired phase margin in the voltage control loop. See the *Design Guide* for instructions on designing the compensation network.

### **Accurate Voltage Reference**

The PE99153 contains an accurate 1.000V reference which is used to drive an accurate output voltage. The 1.000V reference is trimmed at the factory to within  $\pm 1\%$  of 1.000V at 25 °C.

### **Soft Start**

The soft start circuit uses the voltage on the SSCAP pin to limit (pull down) the external VREF pin. This allows the designer to limit the output voltage ramp rate.

Voltage tracking is specified on the VREF pin for applications that require an external tracking capability.

The SSCAP pin is internally connected to a 16 pF (typ) cap to ground and to a 3V internal rail through a 1.2 M $\Omega$  (typ) resistor. When the SDb pin is low, the SSCAP pin is pulled to ground by a 12 K $\Omega$  (typ) resistor. When the shutdown signal is released the pull down switch is released and the voltage on the SSCAP pin begins to ramp up toward 3V. The ramp rate can be increased by tying the SSCAP pin to the 5V input rail through an external resistor. The pin is 5V capable. The ramp rate can also be slowed by connecting the SSCAP pin to ground through a supplemental capacitor.

### **Under Voltage Lockout**

An internal under voltage lockout feature prevents the PE99153 from powering up before input voltage rises above the UVLO threshold of 4.2V (typ). 400 mV (typ) of hysteresis is built-in to prevent false-triggering of the UVLO circuit. The under voltage lockout must be cleared and the SDb pin must be released before the part will be enabled.

### **Power Good Flag**

The PGOOD pin is an open drain output that can be used to sense when the output voltage of the converter has converged to within 10% (typ) of its final value. This pin can also be used to provide limited power sequencing when cascaded with the SDb pin of another PE99153 part.

Internal circuitry senses when the voltage at the EAINM pin has reached to within 10% (typ) of an internal 1.000V reference voltage. When this happens, an internal counter begins counting reference clock cycles and continues counting as long as this condition remains true. When the counter has reached 64, the circuit will assert PGOOD.

When EAINM exits the PGOOD window, there is a 30 mV (typ) hysteresis to prevent chatter when entering or exiting the window. If during the count, the EAINM pin exits the PGOOD threshold, the counter is reset, PGOOD is not asserted and the count will begin again when EAINM re-enters the PGOOD window.

When exiting the PGOOD state, once EAINM is outside of the PGOOD threshold window, an internal counter begins counting and will de-assert PGOOD when it counts 64 reference clock cycles. If during the count, the EAINM pin re-enters the PGOOD threshold, the counter is reset, PGOOD is not de-asserted and the count will begin again when EAINM exits the PGOOD window.

### **Synchronous (External Reference) or Asynchronous (Internal Reference) Switching Frequency**

The PE99153 contains an internal oscillator capable of operating at 1 MHz when the SYNC pin is tied to  $V_{IN}$  or left open or at 500 kHz when the SYNC pin is tied to ground. This reference clock is used in the current mode control loop to time the rising edge of the OUT pin and as a global internal clock reference. When the SYNC pin is actively clocked at a rate of 100 kHz-to-5 MHz, the internal oscillator uses the clocked sync pulse train as the global internal clock reference.

Whether operating synchronously or asynchronously, the open drain SYNCOb pin contains the inverted internal clock reference. This inverted clock signal can be used to aid in the design of polyphase ( $n=2$ ) power supplies.

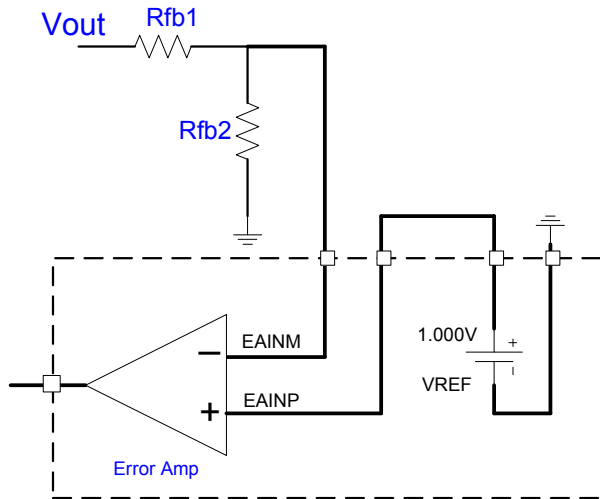
## DESIGN GUIDE

### Setting the Output Voltage

The PE99153 can be configured to output a DC voltage from +1.0V to +3.6V. The user can set the output voltage by selecting the external feedback resistors  $R_{fb1}$  and  $R_{fb2}$ . The feedback resistors divide down the output voltage to be compared to a +1.000V reference voltage. The error amplifier uses this comparison to determine the amount of current to send to the load.

To set the output voltage, a resistor divider must be selected that will produce at +1.000V DC voltage at the EAINM pin when  $V_{OUT}$  has reached the target output voltage.

**Figure 9. Output Voltage Selection**



$$V_{OUT} = (R_{fb1} + R_{fb2}) / R_{fb2} = 1 + R_{fb1} / R_{fb2}, \text{ and}$$

$$R_{fb1} = R_{fb2} * (V_{OUT} - 1), +1V < V_{OUT} \leq +3.6V$$

The PE99153 reference design uses a value of 10 k $\Omega$  for  $R_{fb2}$ .

#### Example:

Desired  $V_{OUT} = +2.5V$

$R_{fb2} = 10 \text{ k}\Omega$

$R_{fb1} = 10 \text{ k}\Omega * (+2.5V - 1) = 15 \text{ k}\Omega$

\* For a desired output voltage of 1V,  $R_{fb1}$  can be replaced with a 0 $\Omega$  resistor and  $R_{fb2}$  not installed. This is equivalent to directly connecting  $V_{OUT}$  to EAINM.

### Output Inductor Selection

The output Inductor serves as the main energy storage element in a switching regulator. It is perhaps the most critical component influencing the performance of the buck regulator. It impacts many aspects of the power supply system performance, including power supply bandwidth, output voltage ripple and ripple spectrum, and switching, conduction, and core losses. Additionally, specific aspects

of the buck regulator itself place requirements on the range of allowable Inductor values. These aspects include the internal current detector sensitivity, the slope compensation ramp dynamic range, and the current limitations of the part. The selection of the Inductor is also a function of the specifics of the application including input voltage, output voltage, load current range, switching frequency, PCB area, efficiency targets, power supply bandwidth, and ripple requirements, to name a few.

Many performance requirements and other component selections place restrictions on the Inductor selection. However, since the Inductor selection plays a central role in the performance of the power supply, its selection needs to be made early in the design process.

Therefore, as a starting point, the Inductor needs to be initially selected based on a few rough calculations and selection can be refined iteratively as more system requirements are introduced.

The voltage across the Inductor is  $V_L = L \times \Delta I_L / \Delta t$ , where  $\Delta I_L$  is defined to be the Inductor peak-to-peak current ripple. The ripple current is the change in the Inductor current during each switching cycle. For the PE99153, the lower limit of  $\Delta I_L$  is set by the current threshold comparator sensitivity, while the upper limit of  $\Delta I_L$  is set by the current mode compensation dynamic range.

Given the output voltage, switching frequency, input voltage and the minimum  $\Delta I_L$  required by the part, the Inductance can be calculated as:

$$L = V_L \times \Delta t / \Delta I_L$$

$$L = V_{OUT} / (F_{SW} \times \Delta I_L) \times [1 - D], \text{ where}$$

Duty cycle =  $D = V_{OUT} / V_{IN}$

Switching frequency =  $F_{SW}$

Duration of Inductor voltage =  $\Delta t = D / F_{SW}$

As the output switches pull the OUT pin alternately to  $V_{IN}$  and to GND, the inductor peak to peak current ripple (triangular current waveform magnitude) is expressed as:

$$\Delta I_L = V_{OUT} / (L \times F_{SW}) * (1 - D)$$

#### Example:

$V_{IN} = +5.0V$

$V_{OUT} = +2.5V$

$F_{SW} = 1 \text{ MHz}$

$\Delta I_L = 0.5A$

$L = V_{OUT} / (F_{SW} \times \Delta I_L) \times [1 - D]$

$L = (+2.5 / (1 \text{ MHz} \times 0.5)) * [(1 - (+2.5 / +5.0))] = 2.5 \mu H$

The Inductor self resonant frequency (SRF) should be selected to be at least 10x higher than the switching frequency  $F_{SW}$ . Meeting this requirement will ensure stability, reduce output ripple and improve efficiency.

**Note:**  $V_{in}$  recommended maximum slew rate is 100 V/s.

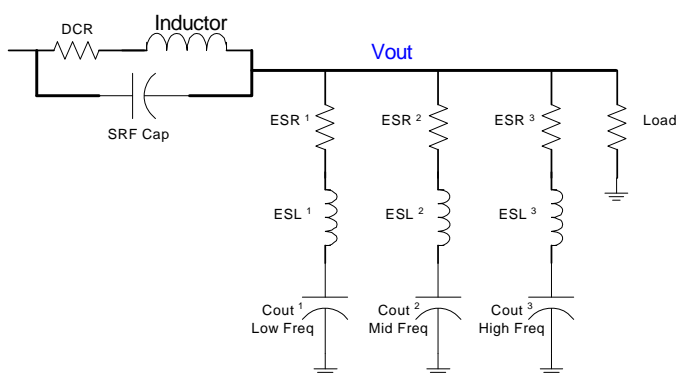
Refer to application note TDAPN9915x.

The DC resistance of the Inductor will primarily impact efficiency. For optimal efficiency, the inductor DC resistance should be selected to be on the order of magnitude of the  $R_{ON}$  of the high side switch and low side switch. Calculation of the efficiency impact will be discussed in the efficiency section of the Design Guide. A smaller DC resistance will improve efficiency but will likely impact PCB area, a subject not addressed in this Design Guide.

### Output Capacitor Selection

The output Capacitor works in tandem with the output Inductor to filter the Inductor ripple current and to source and sink current to meet the load demand during a load step. The output Capacitor is implemented as a network of parallel capacitors covering low, mid, and high frequency operation. The capacitor Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL) have a direct impact on the output voltage ripple, output voltage droop under transient loading, and loop stability. Ceramic X7R dielectric capacitors are recommended for their thermal and electrical properties, along with their size and cost.

Figure 10. Output Capacitor Selection



The output voltage droop should be empirically determined to satisfy the application load step response requirements. During a transient step in the load current, the output voltage will initially experience an IR drop of  $\Delta I_{LOAD} \times ESR$ . If the output capacitor bank is too large, the IR drop is minimized but the  $V_{OUT}$  recovery time is longer. If the output capacitor bank is too small, the IR drop is increased but the  $V_{OUT}$  recovery time is shorter.

The output voltage ripple should be chosen to meet the application requirements and tradeoff with the physical size of the capacitor bank. The output voltage ripple waveform can be estimated by taking the inverse Fourier transform of the product of the Fourier transform of the input signal and the frequency domain transfer function of the network in Figure 10. (The input to the transfer

function can be approximated as an ideal square wave with period of  $F_{SW}$ , amplitude of  $V_{IN}$  and a duty ratio of  $V_{OUT}/V_{IN}$ .)

If a SPICE simulation tool is available, the above estimation can be done by placing the above mentioned square wave at the input of the filter network and solving for the output waveform.

Additionally, the total output capacitance and load resistance set the dominant pole of the voltage mode control loop. Voltage mode loop stability is described in the "Voltage Control Loop Compensation Network Design" section.

In addition to playing a role in stability and output voltage ripple, the output capacitor bank must be able to absorb the inductor ripple current. The inductor peak-to-peak ripple current, calculated as  $\Delta I_L$  in the inductor selection section, will be absorbed by the capacitor bank. Note that the RMS current through the output cap can be calculated as  $\Delta I_L/\sqrt{3}$  since inductor ripple current waveform is triangular. The frequency range of capacitors absorbing the ripple current must be rated to handle this ripple current.

The PE99153 reference design features three output capacitors (Cout1, Cout2, and Cout3) that have been chosen to blend total capacitance, ESR, and ESL to meet the ripple, droop, and stability requirements over frequency.

### Input Capacitor Selection

The input capacitor network sources the trapezoidal current wave through the source terminal of the high side switch. Therefore, the RMS current handling and maximum voltage rating are the main considerations in selecting the input capacitors.

Neglecting the small (as compared with the load) Inductor ripple current and assuming that the input capacitor sources all of the ripple current, the RMS current through the input capacitor can be calculated as

$$I_{RMS-CIN} = I_{LOAD(max)} \times \sqrt{[D \times (1-D)]}$$

In addition to sourcing the trapezoidal current wave through the high side switch, the input bypass capacitors absorb the high frequency components of the switching power supply preventing conducted EMI from reaching the up stream supply. As such, the input bypass capacitor SRF should be on the order of 10x higher than the switching frequency of the buck regulator. Additional high frequency capacitors may be added to further attenuate the high frequency conducted EMI.

Like the output capacitors, Ceramic X7R dielectric capacitors are recommended with the added benefit that the X7R capacitors have very low DC voltage de-rating.

### Efficiency Estimation and Improvement

The efficiency of a switch mode power supply can be estimated by identifying and estimating all sources of loss in the power supply system. These loss terms include switching losses, resistive losses, losses incurred on chip and losses associated with external passive components. External passive losses occur primarily in the output inductor, the output capacitor and the input capacitor. Internal losses at high current are dominated by the high and low side switch resistance. At low current, internal losses are dominated by quiescent bias current and switching related losses.

The PE99153 Design Guide provides a simple tool for estimating loss. Losses are parameterized across input voltage, output voltage and switching frequency to provide accurate estimates of the performance of the part under a variety of conditions.

The following sections give the mathematical expressions of six main loss terms calculated in the design guide spreadsheet.

#### Input Capacitor

The loss in the input capacitor can be calculated by using the estimate of the RMS capacitor current calculated in the input capacitor selection section. Given that:

$$I_{RMS-CIN} = I_{LOAD(max)} \times \sqrt{[D \times (1-D)]}$$

Power lost in the input capacitor can be calculated as:

$$P_{LOSS-CIN} = I_{RMS-CIN}^2 \times R_{CIN-ESR}$$

#### Output Capacitor

The RMS current through the output capacitor in steady state was calculated in the output capacitor selection section as  $\Delta IL/\sqrt{3}$ . Power loss in the output capacitor is then calculated as:

$$P_{LOSS-COUT} = (\Delta IL^2 / 3) \times R_{COUT-ESR}$$

Note that  $R_{COUT-ESR}$  is the ESR of the frequency range of capacitors absorbing the ripple current.

#### Inductor

The inductor RMS current is given by:

$$I_{LRMS} = I_{LOAD} - \Delta IL/2 + \Delta IL/\sqrt{3}$$

Power lost in the DC resistance of the inductor is then given as:

$$P_{LOSS-LOUT-DCR} = I_{LRMS}^2 \times R_{LOUT-DCR}$$

#### High Side Switch Loss

During the time the HSS is on, it is supporting the load current plus the inductor ripple current. RMS current through the HSS, when it is on, is given by:

$$I_{RMS-HSS} = I_{LOAD} - \Delta IL/2 + \Delta IL/\sqrt{3}$$

$$P_{LOSS-HSS} = I_{RMS-HSS}^2 \times R_{ON-HSS} \times D$$

Where the extra factor of  $D = V_{OUT}/V_{IN}$  is the duty ratio and is included because power is only dissipated in the HSS when it is on.

#### Low Side Switch Loss

During the time the LSS is on, it is supporting the load current plus the inductor ripple current. RMS current through the LSS, when it is on, is given by:

$$I_{RMS-LSS} = I_{LOAD} - \Delta IL/2 + \Delta IL/\sqrt{3}$$

$$P_{LOSS-LSS} = I_{RMS-LSS}^2 \times R_{ON-LSS} \times (1 - D)$$

Where the extra factor of  $1 - D = V_{OUT}/V_{IN}$  is the duty ratio of the LSS and is included because power is only dissipated in the LSS when it is on.

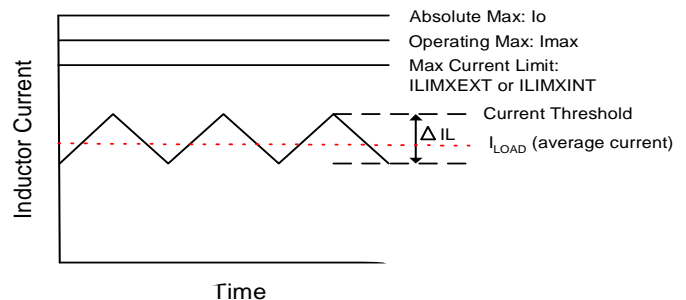
#### Other Internal Loss

A complete list of internal losses in the PE99153 regulator is estimated and available in the PE99153 design guide spreadsheet available online. The internal losses are parameterized across input voltage, output voltage and switching frequency to provide accurate estimates of the performance under a variety of conditions.

#### Setting the Current Limit

When the RSEL pin is grounded, the PE99153 uses an internal current limiting resistor that will limit the output current to a value of  $I_{LIMXINT}$  listed in *Table 2* of the datasheet. See *Figure 11* for a visual description of the various current limits. The part can be programmed to use an alternate current limit by tying the RSEL pin to  $V_{IN}$ . In this mode, the PE99153 can be programmed to various output current limits through the selection of a resistor connecting the RSET pin to ground.

Figure 11. PE99153 Current Limit



In external RSET mode, the PE99153 senses the voltage applied to the ISET pin (from the EAOUT pin, through the compensation network) and subtracts the resulting reference current offset. This subtraction is then applied to the RSET pin. This voltage at the RSET pin draws current through the RSET resistor. This current is used as a current threshold to set the peak inductor current in the current mode control loop. The maximum voltage at the RSET pin is limited to VMAXRSET in Table 2 independent of the voltage applied to the ISET pin. Since this voltage is limited, the maximum reference current through the RSET resistor is limited to VMAXRSET/RSET.

After a reference current is generated through the RSET pin, the current is multiplied by the GIREF parameter listed in Table 2. Thus the peak current allowed by the current mode control loop will be limited to:

$$I_{LIMIT} = G_{IREF} \times (V_{MAXRSET}/R_{SET}) - \Delta I_{COMP}$$

Solving for RSET

$$R_{SET} = (G_{IREF} \times V_{MAXRSET}) / (I_{LIMIT} + \Delta I_{COMP})$$

### Slope Compensation Ramp Selection

While providing improved bandwidth and inherent current limiting, all current mode control switching regulators require slope compensation to ensure stability across all applications conditions. The PE99153 provides adjustable slope compensation to allow the designer to optimize transient response and stability requirements.

During steady state, a compensation ramp is created at the ICOMP pin. The RC ramp is created by the external RCOMP resistor and an internal capacitor. The ramp is reset any time the low side switch is on by means of a reset switch. The voltage at the ICOMP pin is multiplied by the GIREF parameter in Table 2 and is subtracted from the reference current of the current threshold comparator.

Before calculating the required slope compensation to ensure stability, a related slope is defined. In steady state, when the low side switch is on, the inductor current ramps down at a rate of M2. M2 is given as VOUT/L, where L is the inductance of the output inductor.

The minimum slope compensation ramp current, Ma required for mathematical steady state stability under all conditions is one half of M2. That is:

$$M_a \geq M_2/2$$

To provide margin to the minimum, a compensation slope equal to M2 is recommended:

$$M_a = M_2$$

Given the required compensation current (Ma), the voltage ramp rate at the ICOMP pin can be calculated by dividing by the GICOMP parameter in Table 2.

$$\Delta V_{ICOMP} = \Delta I_{COMP} / G_{ICOMP}, \text{ where}$$

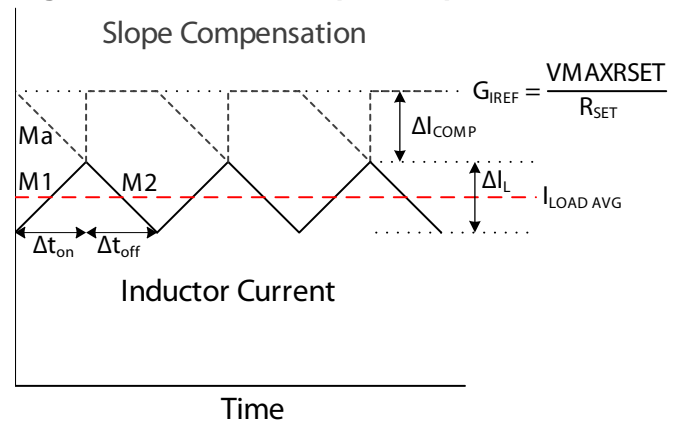
$$\Delta I_{COMP} = (\Delta I_L \times \Delta t_{on} \times M_a/M_2) / \Delta t_{off} \text{ and } \Delta V_{ICOMP} = (0.95 \times V_{OUT}^2) / (C_{ICOMP} \times R_{COMP} \times F_{SW} \times V_{IN})$$

Next, substituting for ΔIL from the output inductor equation and given the required voltage ramp rate and the internal capacitance connected to the ICOMP pin, CCOMP in Table 2, the resistor connected from VOUT to the ICOMP pin can be calculated:

$$R_{COMP} = (0.95 \times G_{ICOMP} \times L) / (C_{ICOMP} \times M_a/M_2),$$

where 95% of VOUT is used to achieve a linear approximation of the average current through CCOMP, assuming the voltage drop over 1 cycle varies from 100 to 90%.

Figure 12. PE99153 Slope Compensation



### Voltage Control Loop Compensation Network Design

The PE99153 contains a current mode control loop and a voltage mode control loop as shown in Figure 13.

The current mode control loop, to first order, controls average inductor current and so behaves as a current source. Conceptually, the current mode control loop can be replaced with a voltage controlled current source.

External to the compensation network, the resulting network contains one pole in the voltage control loop. This pole is created by the parallel combination of Cout and the Load Resistance and is located at:  $1/(2\pi R_{LOAD} C_{OUT})$

One requirement of the voltage control loop stability analysis and design is to maintain significant attenuation at the switching frequency of the converter. If this requirement is not met, the switching noise can enter the control loop and loop stability will be lost. To ensure sufficient attenuation at the switching frequency, a unity gain cross over frequency one decade below the switching frequency is recommended. Additional margin may be desired depending on the application requirements.

The pole created by the load and the output capacitor is dependent on load current. The load current can vary, likely all the way down to zero load current. When this happens the output pole frequency falls arbitrarily low. It is clear that this highly variable pole will not be sufficient to set a dominant pole in the loop to ensure stability.

The recommended compensation technique is a combined pole-zero compensation network. The zero is set to cancel the variable load pole at minimum load so that the load pole does not affect phase margin of the system when the pole location is at its minimum value, possibly even in the bandwidth of the control loop. With the load pole canceled by the additional zero, the added pole in the compensation network acts as a stable dominant pole. This dominant pole location can be

selected for both attenuation of the  $F_{SW}$  switching noise and for the required phase margin and loop bandwidth.

With this compensation technique, the zero location is calculated as  $1/(2\pi R_C C_C)$ .  $R_C$  and  $C_C$  should be selected to cancel the load pole at minimum load.

If the compensation network resistor is selected to be much less than the output impedance  $R_{OUT}$  of the error operational transconductance amplifier (OTA), the dominant pole location can then be approximated as  $1/(2\pi R_{OUT} C_C)$ . At first glance this may seem to make the dominant pole location dependent on the loosely controlled error amp output impedance. However, as the error amp output impedance drops, the DC gain of the system and the dominant pole location reduce together. The result is that the unity gain cross over frequency (set by the dominant pole) is independent of OTA output impedance variation over process and temperature. A compensation network design spreadsheet is available in the PE9915x Design Tool.

**Figure 13. PE99153 Control Loops**

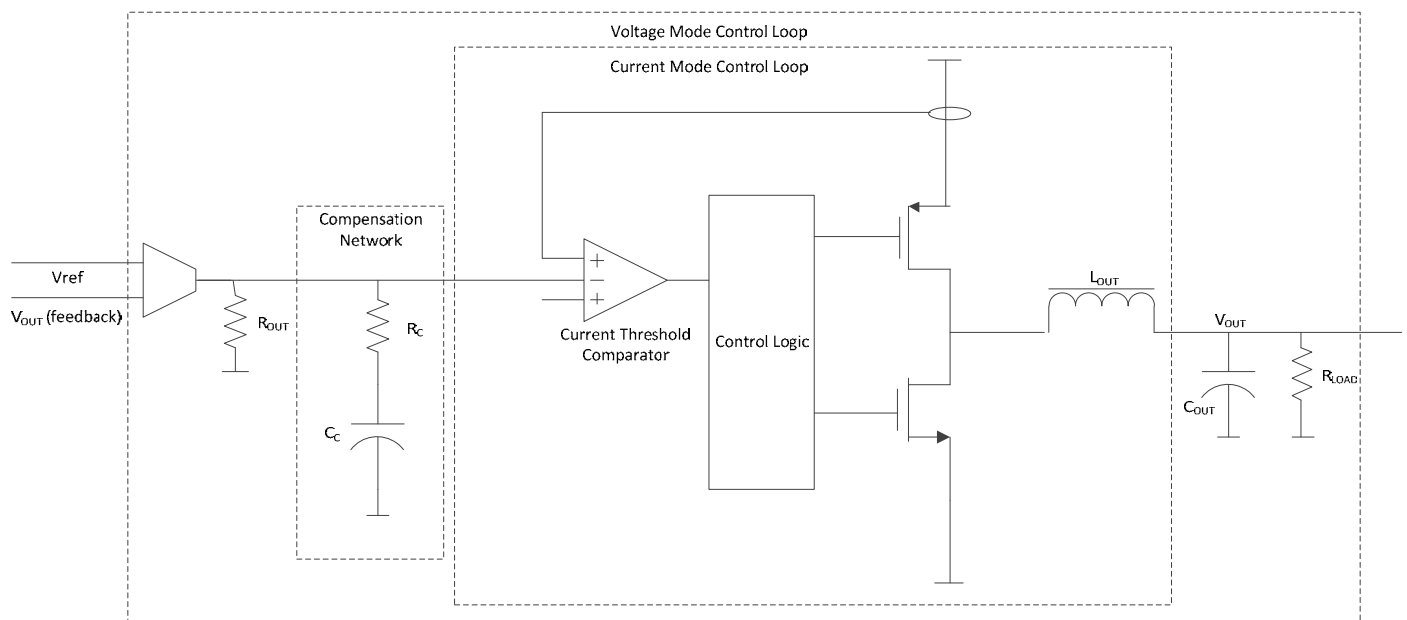
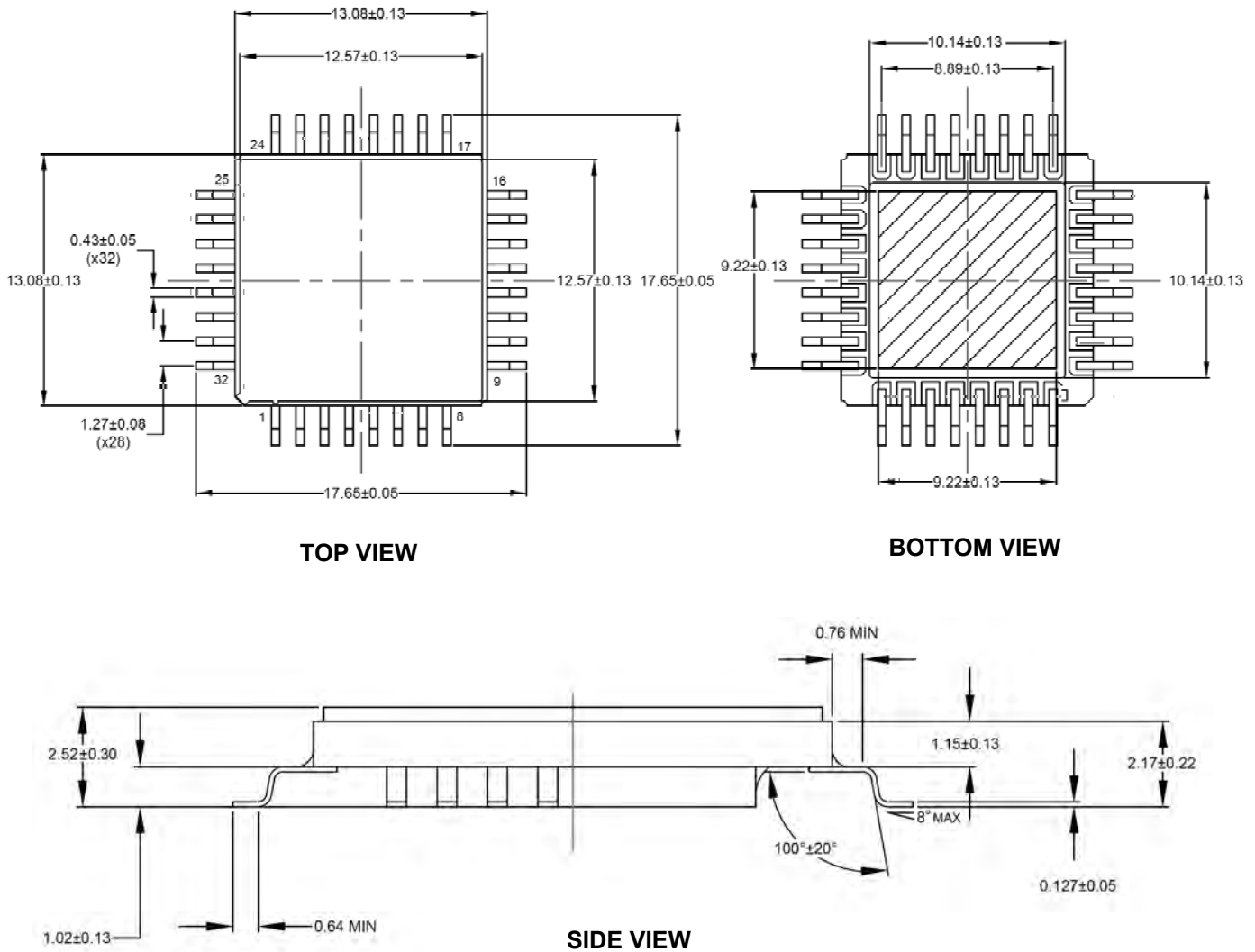


Figure 14. Package Drawing (dimensions are in millimeters)

# 32L CQFP Gullwing

## Mechanical Outline Drawing



DIMS IN MM  
 NOT TO SCALE

Rev. 01 050817  
 IIGNALB



**Figure 15. Top Marking Specifications**



- Line 1: Pin 1 indicator △, e2v and Peregrine logo
- Line 2: Part number (XX will be specified by the purchase order)
- Line 3: Date code (last two digits of the year and work week)
- Line 4: Wafer lot # (as many characters as room allows)
- Line 5: DOP # (e2v internal / 5 digits / optional, as room allows)
- Line 6: aa = wafer #, b = bond option (A-H), ccc = serial number

Note: There is **NO** backside marking on any of the Peregrine products.

**Table 9. Ordering Information**

Order Code	Description	Package	Shipping Method
99153-01 <sup>*</sup>	Engineering samples	32-lead CQFP	24 units / Jedec tray
99153-11	Flight units	32-lead CQFP	24 units / Jedec tray
99153-00	Evaluation kit		1 / Box
99153-98	Engineering sample die	Die	Waffle Pack
99153-99	Flight die	Die	Waffle Pack

Note: \* The PE99153-01 devices are engineering sample (ES) prototype units intended as initial evaluation units for customers of the PE99153-01 flight units. The PE99153-01 device provides the same functionality and footprint as the PE99153-11 space qualified device, and intended for engineering evaluation only. They are tested at +25 °C only and processed to a non-compliant flow (e.g. No burn-in, non-hermetic, etc). These units are non-hermetic and are not suitable for qualification, production, radiation testing or flight use. Flight bare die is probed at 25 °C only.

## Sales Contact and Information

**Contact Information:**  
e2v - <http://www.teledyne-e2v.com> - inquiries@e2v-us.com

**Advance Information:** The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.  
**Preliminary Specification:** The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product. **Product Specification:** The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

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