REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 02. Technical changes to 1.3, 1.4, and table I. Change to figures 1, 2, and 3. Add vendor CAGE 01295. Editorial changes throughout. Remove JAN replacement part number M38510/75652BRX and 2X.	89-06-05	M. A. Frye
B	Add vendor CAGE F8859. Add device type 03. Add case outline X. Add table III, delta limits. Update drawing to MIL-PRF-38535 requirements. – jak	02-12-23	Thomas M. Hess
C	Add radiation features for device type 03 in section 1.5. Update the boilerplate to include radiation hardness assured requirements for device type 03. Editorial changes throughout. – jak	05-02-22	Thomas M. Hess
D	Update radiation features in section 1.5. Add table IB and paragraphs 4.4.4.1 - 4.4.4.2. Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. – LTG	11-12-19	Thomas M. Hess
E	Update dimensions of case outline X to figure 1. - LTG	12-08-23	Thomas M. Hess
F	Update absolute rating maximum supply voltage range in section 1.3 for Vendor cage code F8859 supplying devices.- MAA	17-05-30	Thomas M. Hess
G	Add device with case outline Y for grounded lid for class V device. Update device supplier's information and boilerplate paragraphs as required by the MIL-PRF-38535. – MAA	19-02-22	Thomas M. Hess

REV																				
SHEET																				
REV	G	G	G																	
SHEET	15	16	17																	
REV STATUS			REV			G	G	G	G	G	G	G	G	G	G	G	G	G	G	
OF SHEETS			SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A	PREPARED BY James E. Nicklaus	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/landandmaritime**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY D. A. DiCenzo	
	APPROVED BY Michael A. Frye	MICROCIRCUIT, DIGITAL, ADVANCED CMOS, OCTAL D-TYPE FLIP-FLOP, TTL COMPATIBLE INPUTS, THREE-STATE OUTPUTS, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 88-03-02	
	REVISION LEVEL G	SIZE: A · CAGE CODE: **67268** · **5962-87631**
		SHEET 1 OF 17

DSCC FORM 2233
APR 97

5962-E206-19

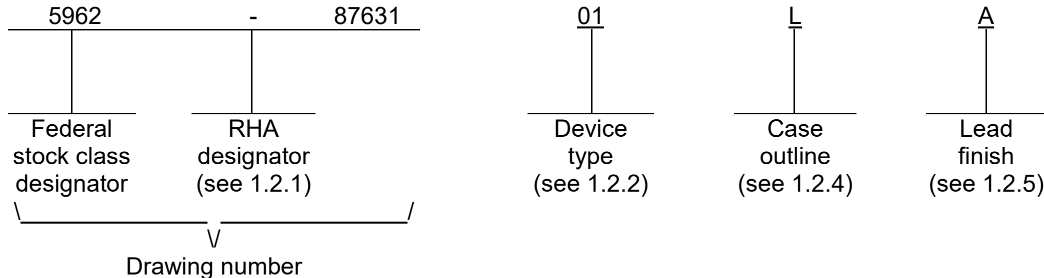
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

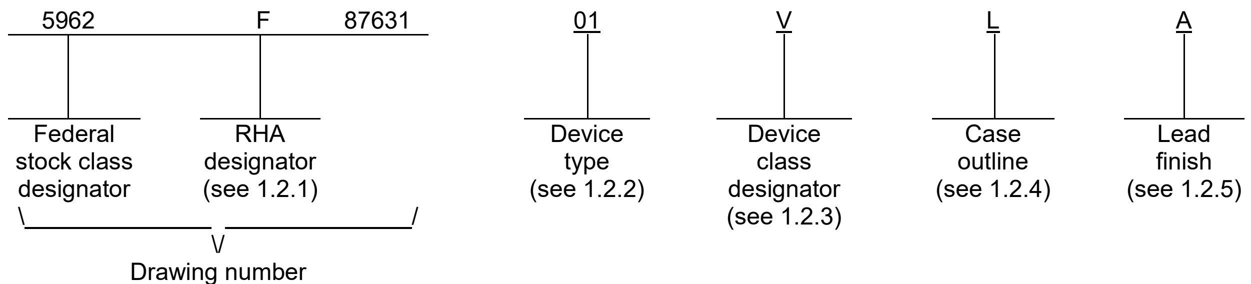
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACT374	Octal D-type flip-flop with three-state outputs and TTL compatible inputs
02	54ACT11374	Octal D-type flip-flop with three-state outputs and TTL compatible inputs
03	54ACT374	Octal D-type flip-flop with three-state outputs and TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
X	See figure 1	20	Flat pack
Y	See figure 1	20	Flat pack 5/
2	CQCC1-N20	20	Square leadless chip carrier
3	CQCC1-N28	28	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC}):
For device types 01 and 02 .... -0.5 V dc to +6.0 V dc
For device type 03 (Vendor cage code F8859) .... -0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN}) .... -0.5 V dc to V_{CC}+ 0.5 V dc
DC output voltage range (V_{OUT}) .... -0.5 V dc to V_{CC}+ 0.5 V dc
Clamp diode current .... ±20 mA
DC output current (I_{OUT}) (per pin) .... ±50 mA
DC V_{CC} or GND current (per pin) .... ±100 mA
Storage temperature range (T_{STG}) .... -65°C to +150°C
Maximum power dissipation (P_D) .... 500 mW
Lead temperature (soldering, 10 seconds) .... +260°C
Thermal resistance, junction-to-case (θ_{JC}) .... See MIL-STD-1835
Junction temperature (T_J) .... +175°C 3/

1.4 Recommended operating conditions. 2/ 4/

Supply voltage range (V_{CC}) .... +4.5 V dc to +5.5 V dc
Input voltage range (V_{IN}) .... +0.0 V dc to V_{CC}
Output voltage range (V_{OUT}) .... +0.0 V dc to V_{CC}
Case operating temperature range (T_C) .... -55°C to +125°C
Input rise or fall rate ($\Delta t/\Delta t$):
V_{CC} = 4.5 V to 5.5 V .... 0 to 8 ns/V

Minimum setup time, Dn to CP (t_s):
Device types 01, 03, T_C = +25°C, V_{CC} = 4.5 V .... 4.5 ns
Device type 02, T_C = +25°C, V_{CC} = 4.5 V .... 3.0 ns
Device types 01, 03, T_C = -55°C to +125°C, V_{CC} = 4.5 V .... 5.5 ns
Device type 02, T_C = -55°C to +125°C, V_{CC} = 4.5 V .... 3.0 ns

Minimum hold time, Dn to CP (t_h):
Device types 01, 03, T_C = +25°C, V_{CC} = 4.5 V .... 2.0 ns
Device type 02, T_C = +25°C, V_{CC} = 4.5 V .... 5.5 ns
Device types 01, 03, T_C = -55°C to +125°C, V_{CC} = 4.5 V .... 2.0 ns
Device type 02, T_C = -55°C to +125°C, V_{CC} = 4.5 V .... 5.5 ns

Minimum pulse width, Dn to CP (t_w):
Device types 01, 03, T_C = +25°C, V_{CC} = 4.5 V .... 5.5 ns
Device type 02, T_C = +25°C, V_{CC} = 4.5 V .... 9.0 ns
Device types 01, 03, T_C = -55°C to +125°C, V_{CC} = 4.5 V .... 7.4 ns
Device type 02, T_C = -55°C to +125°C, V_{CC} = 4.5 V .... 9.0 ns

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1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
4/ Unless otherwise specified, the values listed above shall apply over the full V_{CC} and T_C recommended operating range.
5/ Package case outline Y flat pack with grounded lid.

1.4 Recommended operating conditions – Continued. 2/ 4/

Minimum clock frequency (f_{MAX}):
- Device types 01, 03, T_C = +25°C, V_{CC} = 4.5 V .... 92 MHz
- Device type 02, T_C = +25°C, V_{CC} = 4.5 V.. 55 MHz
- Device types 01, 03, T_C = -55°C to +125°C, V_{CC} = 4.5 V.................................. 68 MHz
- Device type 02, T_C = -55°C to +125°C, V_{CC} = 4.5 V... 55 MHz

1.5 Radiation features.

Device type 03:
- Maximum total dose available (high dose rate = 50 – 300 rad (Si)/s) .... 300 krad (Si)
- No single event latch-up (SEL) occurs at effective LET (see 4.4.4.2)............... ≤ 93 MeV-cm^2/mg 6/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC Standard JESD20 - Standard for Description of 54/74ACXXXXX and 54/74ACTXXXXX Advanced High-Speed CMOS Devices.

(Copies of these documents are available online at http://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S Arlington, VA 22201).

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at http://www.astm.org/ or from ASTM International, P. O. Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959).

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

6/ Limits obtained during technology characterization/qualification, guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 38 (see MIL-PRF-38535, appendix A).

TABLE IA. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5 V \le V_{CC} \le +5.5 V$ unless otherwise specified	Device type and 4/ device class	V_{CC}	Group A subgroups	Limits 5/		Unit
						Min	Max	
Positive input clamp voltage 3022	V_{IC+}	For input under test, I_{IN} = 1.0 mA	01, 03 V	0.0 V	1	0.4	1.5	V
Negative input clamp voltage 3022	V_{IC-}	For input under test, I_{IN} = -1.0 mA	01, 03 V	Open	1	-0.4	-1.5	V
High level output voltage 3006	V_{OH} 6/	$V_{IN} = V_{IH}$ = 2.0 V or V_{IL} = 0.8 V I_{OH} = -50 µA	All	4.5 V	1, 2, 3	4.4		V
			All	5.5 V		5.4		
		$V_{IN} = V_{IH}$ = 2.0 V or V_{IL} = 0.8 V I_{OH} = -24 mA	All	4.5 V		3.7		
			All	5.5 V		4.7		
		$V_{IN} = V_{IH}$ = 2.0 V or V_{IL} = 0.8 V I_{OH} = -50 mA	All All	5.5 V		3.85		
Low level output voltage 3007	V_{OL} 6/	$V_{IN} = V_{IH}$ = 2.0 V or V_{IL} = 0.8 V I_{OL} = +50 µA	All	4.5 V	1, 2, 3		0.1	V
			All	5.5 V			0.1	
		$V_{IN} = V_{IH}$ = 2.0 V or V_{IL} = 0.8 V I_{OL} = +24 mA	All	4.5 V			0.5	
			All	5.5 V			0.5	
		$V_{IN} = V_{IH}$ = 2.0 V or V_{IL} = 0.8 V I_{OL} = +50 mA	All All	5.5 V			1.65	
High level input voltage	V_{IH} 7/		All	4.5 V	1, 2, 3	2.0		V
			All	5.5 V		2.0		
Low level input voltage	V_{IL} 7/		All	4.5 V	1, 2, 3		0.8	
			All	5.5 V			0.8	
Input leakage current low 3009	I_{IL}	V_{IN} = 0.0 V	All All	5.5 V	1, 2, 3		-1.0	µA
Input leakage current high 3010	I_{IH}	V_{IN} = 5.5 V	All All	5.5 V	1, 2, 3		1.0	µA
Off-state output leakage current (high) 3021	I_{OZH}	$V_{IN} = V_{CC}$ or GND $V_{OUT} = V_{CC}$ or GND	All All	5.5 V	1, 2, 3		10.0	µA
Off-state output leakage current (low) 3020	I_{OZL}	$V_{IN} = V_{CC}$ or GND $V_{OUT} = V_{CC}$ or GND	All All	5.5 V	1, 2, 3		-10.0	µA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ -55°C ≤ T_C ≤ +125°C +4.5 V ≤ V_{CC} ≤ +5.5 V unless otherwise specified		Device type and 4/ device class	V_{CC}	Group A subgroups	Limits 5/		Unit
							Min	Max	
Quiescent supply current delta, TTL input levels 3005	ΔI_{CC} 8/	V_{IN} = V_{CC} - 2.1 V All other inputs = V_{CC} or GND	Dn, $\overline{OE}$	01, 02 All	5.5 V	1, 2, 3		1.6	mA
			CP					3.0	
			Dn, $\overline{OE}$, CP	03 All	5.5 V	1, 2, 3		1.6	mA
Quiescent supply current, outputs high 3005	I_{CCH}	V_{IN} = V_{CC} or GND		01, 02 All	5.5 V	1, 2, 3		160	µA
				03 All	5.5 V	1		2.0	
						2, 3		160	
			M, D, P, L, R, F 9/	03 Q, V		1		50	
Quiescent supply current, outputs low 3005	I_{CCL}	V_{IN} = V_{CC} or GND		01, 02 All	5.5 V	1, 2, 3		160	µA
				03 All	5.5 V	1		2.0	
						2, 3		160	
			M, D, P, L, R, F 9/	03 Q, V		1		50	
Quiescent supply current, outputs tri-state 3005	I_{CCZ}	V_{IN} = V_{CC} or GND		01, 02 All	5.5 V	1, 2, 3		160	µA
				03 All	5.5 V	1		2.0	
						2, 3		160	
			M, D, P, L, R, F 9/	03 Q, V		1		50	
Input capacitance 3012	C_{IN}	See 4.4.1c T_C = +25°C		All All	GND	4		10.0	pF
Power dissipation capacitance	C_{PD} 10/	See 4.4.1c T_C = +25°C		01, 03 All	5.0 V	4		95	
				02 All	5.0 V	4		134	
Functional tests 3014	11/	See 4.4.1b V_{IN} = V_{IH} = 2.0 V or V_{IL} = 0.8 V Verify output V_{OUT}		All All	4.5 V	7, 8	L	H	
					5.5 V	7, 8	L	H	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and 4/ device class	V_{CC}	Group A subgroups	Limits 5/		Unit
						Min	Max	
Propagation delay time, CP to Qn 3003	t_{PHL}, t_{PLH} 12/	C_L = 50 pF minimum R_L = 500Ω See figure 5	01, 03 All	4.5 V	9	1.0	10.0	ns
					10, 11	1.0	12.6	
			02 All	4.5 V	9	1.0	11.3	ns
					10, 11	1.0	13.9	
Propagation delay time, output enable, $\overline{OE}$ to Qn 3003	t_{PZH}, t_{PZL} 12/	C_L = 50 pF minimum R_L = 500Ω See figure 5	01, 03 All	4.5 V	9	1.0	10.7	ns
					10, 11	1.0	14.5	
			02 All	4.5 V	9	1.0	11.0	ns
					10, 11	1.0	13.2	
Propagation delay time, output disable, $\overline{OE}$ to Qn 3003	t_{PHZ}, t_{PLZ} 12/	C_L = 50 pF minimum R_L = 500Ω See figure 5	01, 03 All	4.5 V	9	1.0	11.0	ns
					10, 11	1.0	14.5	
			02 All	4.5 V	9	1.0	12.7	ns
					10, 11	1.0	13.6	

1/ For tests not listed in the referenced MIL-STD-883 [e.g. ΔI_{CC}], utilize the general test procedure under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature for the specified limits, to the tests in table IA herein. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

a. V_{IC} (pos) tests, the GND terminal can be open. T_C = +25°C.

b. V_{IC} (neg) tests, the V_{CC} terminal shall be open. T_C = +25°C.

c. All I_{CC} and ΔI_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ RHA parts for device type 03 have been characterized through all levels M, D, P, L, R, and F of irradiation. However, this device is only tested at the 'F' level. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level for any device, T_A = +25 °C.

4/ The word "All" in the device type and device class column, means limits for all device types and device classes.

5/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

6/ V_{OH} and V_{OL} tests will be tested at V_{CC} = 4.5 V. V_{OH} and V_{OL} are guaranteed, if not tested, for V_{CC} = 5.5 V. Limits shown apply to operation at V_{CC} = 5.0 V ±0.5 V. Transmission driving tests are performed at V_{CC} = 5.5 V with a 2 millisecond duration maximum.

7/ The V_{IH} and V_{IL} tests are not required if applied as forcing functions for V_{OH} and V_{OL} tests.

8/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC}$ - 2.1 V (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times ΔI_{CC} maximum; and the preferred method and limits are guaranteed.

TABLE IA. Electrical performance characteristics - Continued.

9/ The maximum limit for this parameter at 100K Rad(si) is 2.0 μA.

10/ Power dissipation capacitance (C_{PD}) determines the no load dynamic power consumption, $P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$ and the dynamic current consumption, $I_S = (C_{PD} + C_L)V_{CC}f + I_{CC} + n \times d \times \Delta I_{CC}$. For both P_D and I_S, n is the number of device inputs at TTL levels, f is the frequency of the input signal, and d is the duty cycle of the input signal.

11/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. After incorporating allowable tolerances in accordance with MIL-STD-883, V_{IL} = 0.4 V and V_{IH} = 2.4 V. For outputs, L < 2.5 V, H ≥ 2.5 V.

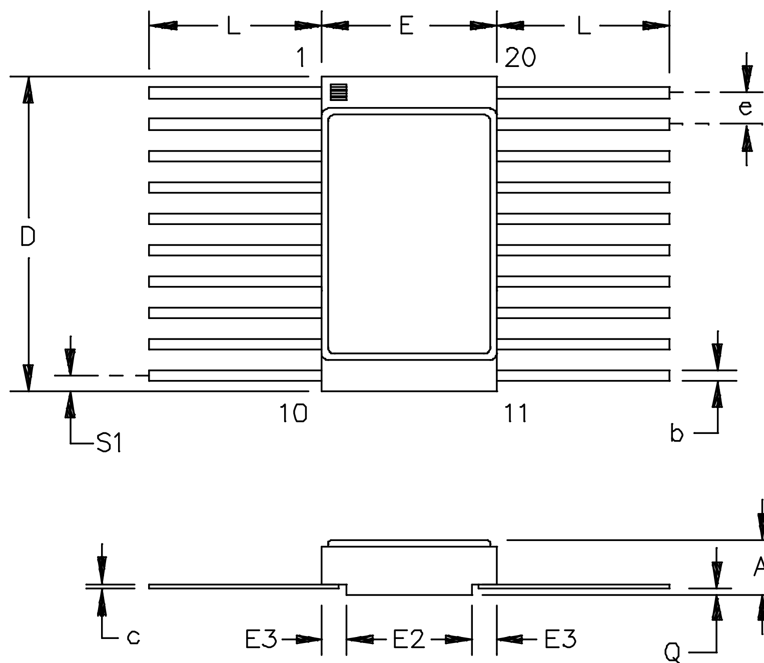
12/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum ac limits for V_{CC} = 5.5 V are 1.0 ns and guaranteed by guard banding the V_{CC} = 4.5 V minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

TABLE IB. SEP test limits. 1/ 2/

Device type	Bias V_{CC} = 5.5 V No SEL at effective LET 3/
03	LET ≤ 93 MeV/(mg/cm^2)

1/ For SEP test conditions, see 4.4.4.2 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Tested at worst case temperature, T_A = +125°C ± 10°C for latch-up.

Case outline X and Y



Symbol	Dimensions					
	Inches			Millimeters		
	Typical	Min	Max	Typical	Min	Max
A		0.075	0.087		1.91	2.21
b		0.015	0.019		0.38	0.48
c		0.003	0.006		0.076	0.152
D		0.505	0.515		12.83	13.08
E		0.275	0.285		6.99	7.24
E2		0.199	0.211		5.05	5.36
E3	0.037			0.95		
e		0.045	0.055		1.14	1.40
L		0.250	0.370		6.35	9.39
Q		0.010	---		0.25	---
S1	0.021			0.55		

Note:
1. Deviation from MIL-STD-1835 REF. F-9, CONFIG. B the dimension c is 0.003 inches minimum instead of 0.004 inches minimum and dimension Q is 0.010 inches Minimum instead of 0.026 inches minimum.
2. Package case outline X flat pack without grounded lid and case outline Y flat pack with grounded lid.

FIGURE 1. Case outline X.

Device types	01 and 03	02	
Case outlines	R, S, X, Y and 2	L	3
Terminal number	Terminal symbol		
1	$\overline{OE}$	Q0	NC
2	Q0	Q1	V_{CC}
3	D0	Q2	D3
4	D1	Q3	D2
5	Q1	GND	D1
6	Q2	GND	D0
7	D2	GND	$\overline{OE}$
8	D3	GND	NC
9	Q3	Q4	Q0
10	GND	Q5	Q1
11	CP	Q6	Q2
12	Q4	Q7	Q3
13	D4	CP	GND
14	D5	D7	GND
15	Q5	D6	NC
16	Q6	D5	GND
17	D6	D4	GND
18	D7	V_{CC}	Q4
19	Q7	V_{CC}	Q5
20	V_{CC}	D3	Q6
21	- - -	D2	Q7
22	- - -	D1	NC
23	- - -	D0	CP
24	- - -	$\overline{OE}$	D7
25	- - -	- - -	D6
26	- - -	- - -	D5
27	- - -	- - -	D4
28	- - -	- - -	V_{CC}

NC = No internal connection

Terminal descriptions	
Terminal symbol	Description
$\overline{OE}$	Output enable inputs (active low)
CP	Clock pulse input
Dn (n = 0 to 7)	Data inputs
Qn (n = 0 to 7)	Data outputs

FIGURE 2. Terminal connections.

Input			Output
Dn	CP	$\overline{OE}$	Qn
H	↑	L	H
L	↑	L	L
X	X	H	Z

H = High voltage level
L = Low voltage level
X = Irrelevant
↑ = Low-to-high transition of the clock.
Z = High impedance

FIGURE 3. Truth table.

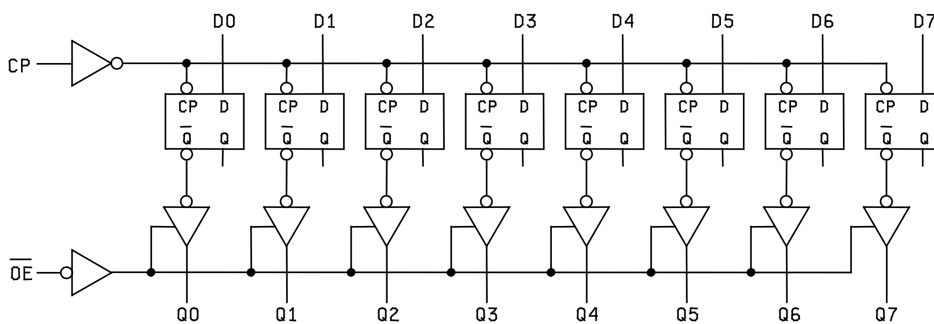


FIGURE 4. Logic diagram.

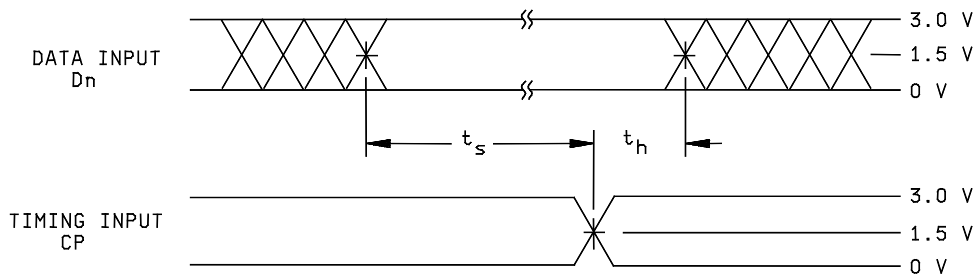
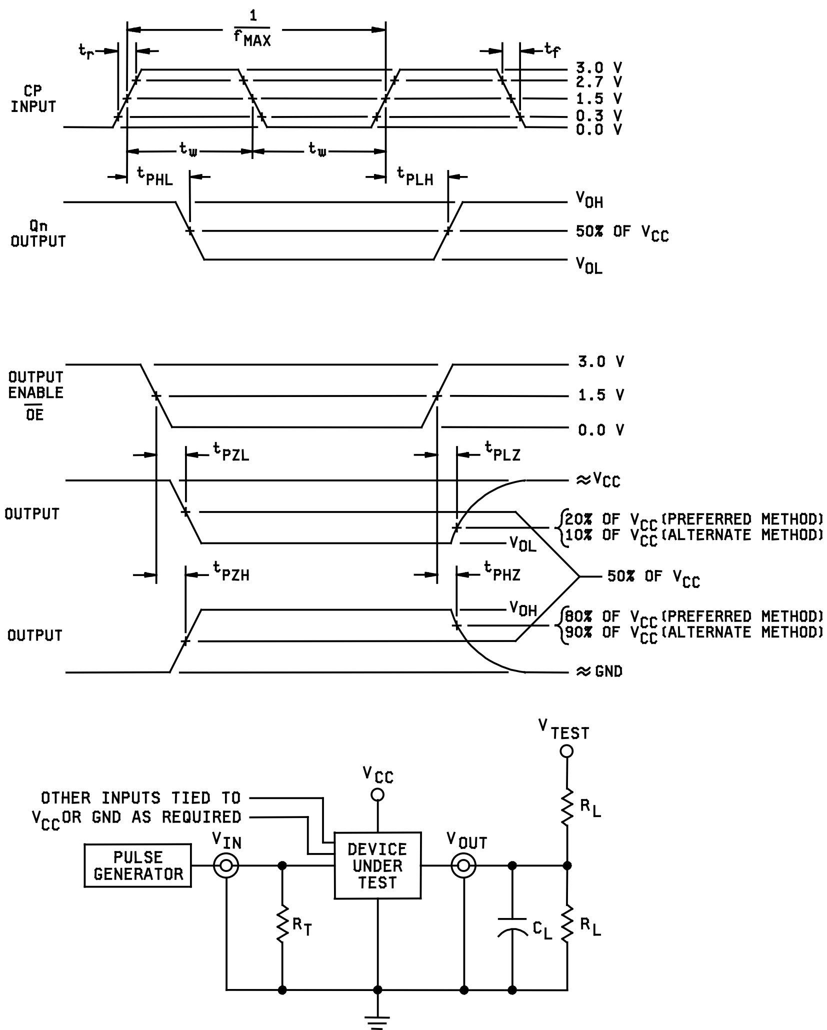


FIGURE 5. Switching waveforms and test circuit.



NOTES:

1. Preferred method:
   When measuring t_{PHZ} and t_{PZH}: V_{TEST} = GND
   When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 2 X V_{CC}
   When measuring t_{PLH} and t_{PHL}: V_{TEST} = open
   Alternate method:
   When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 2 X V_{CC}
   When measuring t_{PHZ}, t_{PZH}, t_{PLH}, and t_{PHL}: V_{TEST} = open
2. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
3. R_T = 50Ω or equivalent. R_L = 500Ω or equivalent.
4. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; t_r ≤ 3 ns; t_f ≤ 3 ns; duty cycle = 50 percent.
5. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
6. Outputs are measured one at a time with one output per measurement.

FIGURE 5. Switching waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 3 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard JESD20 and table IA herein. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table IA)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)			1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 3/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	3/ 1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 7, and deltas.
3/ Delta limits, as specified in table IIB, shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameter 1/	Symbol	Device type	Delta limits
Quiescent supply current	I_{CCH}, I_{CCL}, I_{CCZ}	01 2/	±100 nA
		03	±150 nA
Input current low level	I_{IL}	03	±20 nA
Input current high level	I_{IH}	03	±20 nA
Output voltage low level (I_{OL} = 24 mA, V_{CC} = 5.5 V)	V_{OL}	03	±0.04 V
Output voltage high level (I_{OH} = -24 mA, V_{CC} = 5.5 V)	V_{OH}	03	±0.20 V

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.
2/ The limit may not be production tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein. Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

Device type 03:

(1) Inputs tested high, V_{CC} = 5.5 V dc ±5%, V_{IN} = 5.0 V dc +10%, R_{IN} = 1 kΩ ±20%, and all outputs are open.

(2) Inputs tested low, V_{CC} = 5.5 V dc ±5%, V_{IN} = 0.0 V dc, R_{IN} = 1 kΩ ±20%, and all outputs are open.

4.4.4.1.1 Accelerated annealing testing. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krad (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 or JESD57 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be +25°C and the latchup test temperature is maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA test conditions of SEP.

b. Number of upsets (SEU).

c. Number of transients (SET).

d. Occurrence of latch-up (SEL).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-02-22

Approved sources of supply for SMD 5962-87631 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8763101RA	0C7V7	54ACT374DMQB
	01295	SNJ54ACT374J
5962-8763101SA	0C7V7	54ACT374FMQB
	01295	SNJ54ACT374W
5962-87631012A	0C7V7	54ACT374LMQB
	01295	SNJ54ACT374FK
5962-8763101VRA	01295	SNV54ACT374J
5962-8763101VSA	01295	SNV54ACT374W
5962-8763102LA	3V146	54ACT11374/BLA
5962-87631023A	3V146	54ACT11374/B3A
5962-8763103XA	3/	54ACT374K02Q
5962-8763103XC	3/	54ACT374K01Q
5962-8763103VXA	3/	54ACT374K02V
5962-8763103VXC	3/	54ACT374K01V
5962F8763103RA	F8859	RHFACT374D04Q
5962F8763103RC	F8859	RHFACT374D03Q
5962F8763103XA	F8859	RHFACT374K02Q
5962F8763103XC	F8859	RHFACT374K01Q
5962F8763103VRA	F8859	RHFACT374D04V
5962F8763103VRC	F8859	RHFACT374D03V
5962F8763103VXA	F8859	RHFACT374K02V
5962F8763103VYA	F8859	RHFACT374K04V
5962F8763103VXC	F8859	RHFACT374K01V
5962F8763103VYC	F8859	RHFACT374K03V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

DATE: 19-02-22

Vendor CAGE number	Vendor name and address
0C7V7	Teledyne e2v, Inc. 765 Sycamore Drive Milpitas, CA 95035
01295	Texas Instruments Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243
F8859	ST Microelectronics 3 rue de Suisse CS 60816 35208 RENNES cedex2-FRANCE
3V146	Rochester Electronics 16 Malcolm Hoyt Drive Newburyport, MA 01950

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