The documentation and process conversion measures necessary to comply with this document shall be completed by 30 October 2015.

INCH-POUND
MIL-PRF-19500/455L
30 July 2015
SUPERSEDING
MIL-PRF-19500/455K
16 June 2014

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, NPN, SILICON, POWER SWITCHING, TYPES 2N5664, 2N5665, 2N5666, AND 2N5667, JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for NPN, silicon, power transistors for use in high-speed power-switching applications. Four levels of product assurance are provided for each encapsulated device type as specified in MIL-PRF-19500. Two levels of product assurance are provided for each un-encapsulated device type as specified in MIL-PRF-19500. Provisions for radiation hardness assurance (RHA) to two radiation levels ("R" and "F") are provided for JANTXV and JANHC product assurance level. Provisions for RHA to eight radiation levels are provided for JANS and JANKC product assurance level. RHA level designators; "M", "D", "P", "L", "R", "F", "G", and "H" are appended to the device prefix to identify devices which have passed RHA requirements.

* 1.2 Package outlines and die topography. The device package for the encapsulated device types are as follows: TO-66 in accordance with figure 1, TO-5 and TO-39 in accordance with figure 2, surface mount version U3 in accordance with figure 3. The dimensions and topography for JANHC and JANKC unencapsulated die are as follows: The A version die (for 2N5665/2N5667) in accordance with figure 4, the A version die (for 2N5664/2N5666) in accordance with figure 5, and B version die (for 2N5664/2N5666) in accordance with figure 6.

1.3 Maximum ratings T_A = +25°C unless otherwise specified.

Type	P_{T1} T_A = +25°C (1)	P_{T2} T_C = +100°C (1)	$R_{\theta JA}$ (2)	$R_{\theta JC}$ (2)	V_{CBO}	V_{CEO}	V_{EBO}	I_C	I_B	T_{stg} and T_J
	W	W	°C/W (max)	°C/W (max)	V dc	V dc	V dc	A dc	A dc	T_C°C
2N5664	2.5	30	70	2.6	250	200	6	5	1	
2N5665	2.5	30	70	2.6	400	300	6	5	1	
2N5666, S	1.2	15	145	6.7	250	200	6	5	1	-65 to +200
2N5666U3	1.5	35	116	2.3	250	200	6	5	1	
2N5667, S	1.2	15	145	6.7	400	300	6	5	1	

(1) For derating, see figures 7, 8, 9, 10, and 11.
(2) For thermal impedance see figures 12, 13, 14, and 15.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

AMSC N/A

FSC 5961

1.4 Primary electrical characteristics at T_A = +25°C.

Limits	h_{FE} V_{CE} = 5 V I_C = 1 A		$\|h_{fe}\|$ V_{CE} = 5 V I_C = 0.5 A dc f = 10 MHz	$V_{BE(sat)}$ I_C = 3 A dc (1)	$V_{CE(sat)}$ I_C = 3 A dc (1)	Pulse response		
						t_{on} I_C = 1 A dc	t_{off} I_C = 1 A dc	
	2N5665 2N5667, S	2N5664 2N5666, S, U3					2N5664 2N5666, S, U3	2N5665 2N5667, S
				V dc	V dc	µ s	µ s	µ s
Min	25	40	2.0					
Max	75	120	7.0	1.2	0.4	0.25	1.5	2.0

(1) I_B = 0.3 A dc for 2N5664, 2N5666, 2N5666S, 2N5666U3; I_B = 0.6 A dc for 2N5665, 2N5667, 2N5667S.

* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.6 for a list of available PINs.

* 1.5.1 JAN certification mark and quality level.

* 1.5.1.1 Quality level designators for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV", and "JANS".

* 1.5.1.2 Quality level designators for unencapsulated devices (die). The quality level designators for unencapsulated devices (die) that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANHC" and "JANKC".

* 1.5.2 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for JANS devices in this specification sheet from lowest to highest are as follows: "M", "D", "P", "L", "R", "F", "G", and "H"). The RHA levels that are applicable for JANTXV devices in this specification sheet from lowest to highest are as follows: ("R", and "F").

* 1.5.3 Device type. The designation system for the device types covered by this specification sheet is as follows.

* 1.5.3.1 First number and first letter symbols. The semiconductors of this specification sheet use the first number and letter symbols “2N”.

* 1.5.3.2 Second number symbols. The second number symbols for the semiconductors covered by this specification sheet are as follows: “5664”, “5665”, “5666", and “5667”.

* 1.5.4 Suffix symbols. The following suffix symbols are incorporated in the PIN as applicable.

	A blank suffix symbol indicates a through-hole mount package TO-66 metal can applicable for 2N5664 and 2N5665 only(see figure 1) or a through-hole mount package TO-5 metal can applicable for 2N5666 and 2N5667 only (see figure 2).
S	Indicates a through-hole mount package TO-39 metal can with shorter lead lengths than the corresponding blank second suffix symbol device applicable for 2N5666 and 2N5667 only (see figure 2).
U3	Indicates a 3 pad surface mount package applicable for 2N5666 only (see figure 3).

* 1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on QML-19500.

* 1.5.6 Die identifiers for unencapsulated devices (manufacturers and critical interface identifiers). The manufacturer die identifiers that are applicable for this specification sheet are "A", and "B" (See figure 4 through figure 6, and 6.5).

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

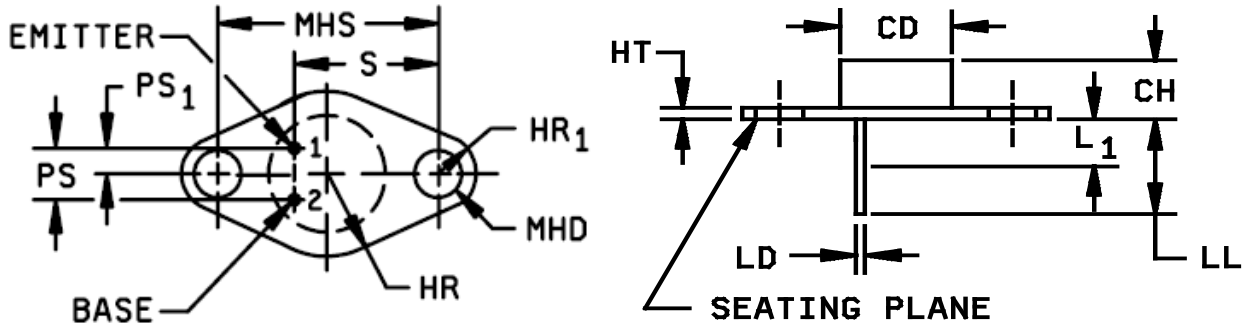
MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at http://quicksearch.dla.mil.)

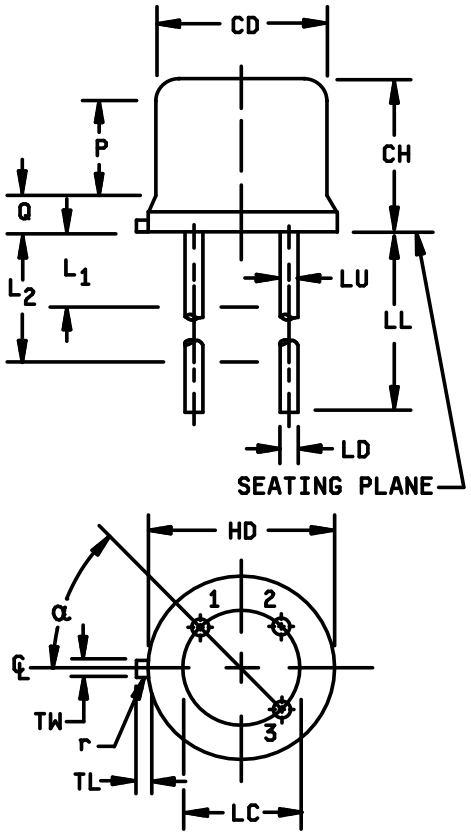
2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.



Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CH	.250	.340	6.35	8.64	
LD	.028	.034	0.71	0.86	7,9
CD	.470	.500	11.94	12.70	2
PS	.190	.210	4.83	5.33	3
PS_1	.093	.107	2.36	2.72	3
HT	.050	.075	1.27	1.91	2, 5
LL	.360	.500	9.14	12.70	7
L_1		.050		1.27	4
MHD	.142	.152	3.61	3.86	
MHS	.958	.962	24.33	24.43	
HR		.350		8.89	
HR_1	.115	.145	2.92	3.68	
S	.570	.590	14.48	14.99	3

NOTES:
1. Dimensions are in inches. Millimeters are given for general information only.
2. Body contour is optional within zone defined by CD.
3. These dimensions shall be measured at points .050 inch (1.27 mm) to .055 inch (1.40 mm) below seating plane. When gauge is not used, measurement shall be made at seating plane.
4. Within this zone the lead diameter may vary to allow for lead finishes and irregularities.
5. HT dimension does not include sealing flanges.
6. The seating plane of header shall be flat within .001 inch (0.025 mm), concave to .004 inch (0.101 mm), convex inside a .520 inch (13.20 mm) diameter circle on the center of the header, and flat within .001 inch (0.025 mm), concave to .006 inch (0.152 mm), convex overall.
7. Both terminals.
8. The collector shall be electrically connected to the case.
9. LD applies between L_1 and LL. Lead diameter shall not exceed twice LD within L_1.
10. Pin 1 is the emitter, pin 2 is the base.
11. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

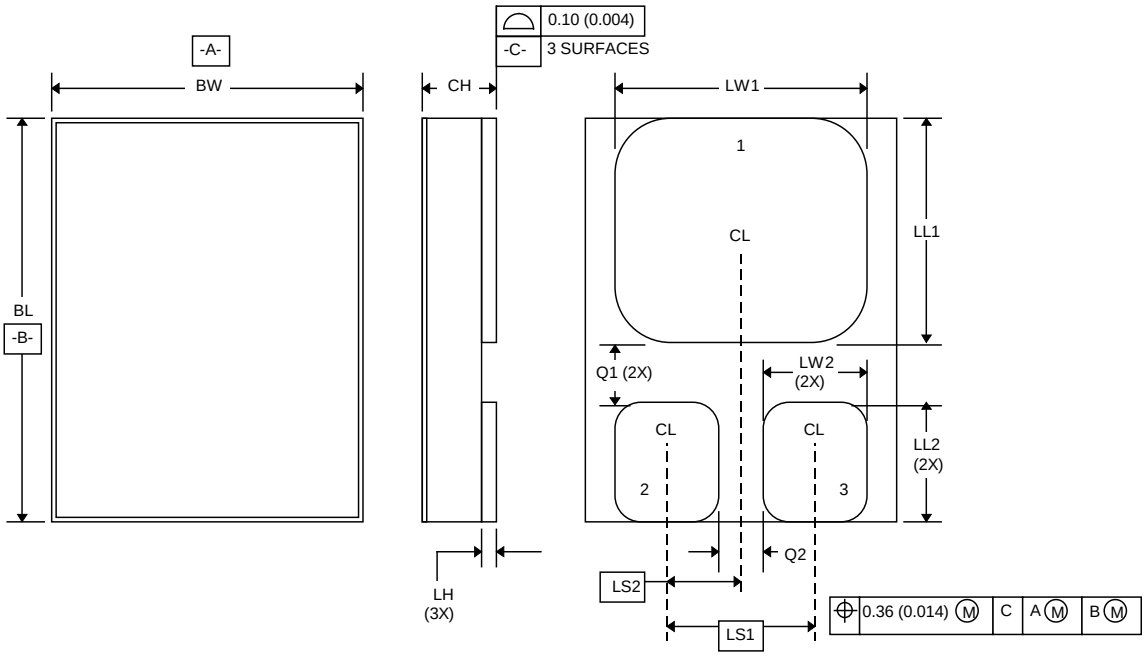
FIGURE 1. Physical dimensions of transistor types 2N5664 and 2N5665 (TO-66).



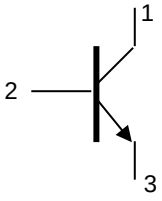
Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		6
LD	.016	.021	0.41	0.53	3
LL	See notes 13 and 14				
L_1		.050		1.27	10
L_2	.250		6.35		10
LU	.016	.019	0.41	0.48	4
P	.100		2.54		5
Q					6
r		.007		0.18	
α	45° TP		45° TP		7
TL	.029	.045	0.74	1.14	
TW	.028	.034	0.71	0.86	

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Measured in the zone beyond .250 inch (6.35 mm) from the seating plane.
4. Measured in the zone .050 inch (1.27 mm) and .250 inch (6.35 mm) from the seating plane.
5. Variations on dimension CD in this zone shall not exceed .010 inch (0.25 mm).
6. Outline in this zone is not controlled.
7. When measured in a gauging plane .054 inch +.001, -.000 (1.37 mm +.03, -.00) below the seating plane of the transistor, maximum diameter leads shall be within .007 inch (.18 mm) of their true location relative to a maximum width tab. Smaller diameter leads shall fall within the outline of the maximum diameter lead tolerance.
8. The collector shall be electrically connected to the case.
9. Measured from the maximum diameter of the actual device.
10. All three leads
11. Diameter of leads in this zone is not controlled.
12. Lead 1 - emitter; lead 2 - base, lead 3 - collector.
13. For transistor types 2N5666 and 2N5667, LL is 1.500 inch (38.1 mm) minimum and 1.75 inch (44.45 mm) maximum.
14. For transistor types 2N5666S and 2N5667S, LL is .500 inch (12.7 mm) minimum and .75 inch (19.05 mm) maximum.
15. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Physical dimensions of transistor types 2N5666, 2N5666S, 2N5667 and 2N5667S (TO-5 and TO-39).



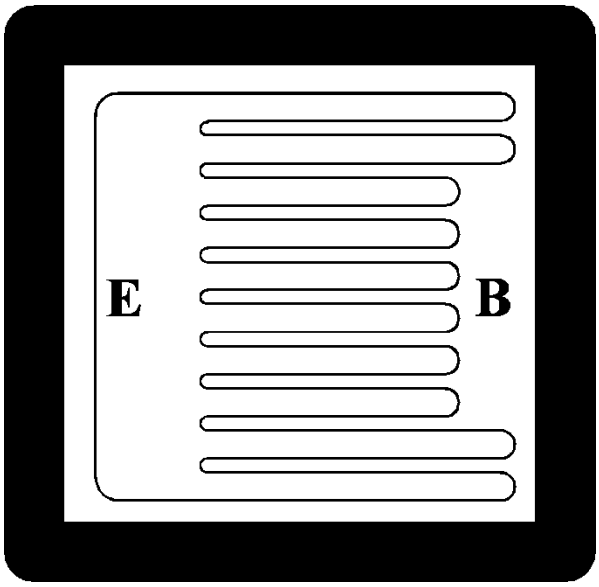
SCHEMATIC



Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.395	.405	10.04	10.28
BW	.291	.301	7.40	7.64
CH	.1085	.1205	2.76	3.06
LH	.010	.020	0.25	0.51
LW1	.281	.291	7.14	7.39
LW2	.090	.100	2.29	2.54
LL1	.220	.230	5.59	5.84
LL2	.115	.125	2.93	3.17
LS1	.150 BSC		3.81 BSC	
LS2	.075 BSC		1.91 BSC	
Q1	.030		0.762	
Q2	.030		0.762	

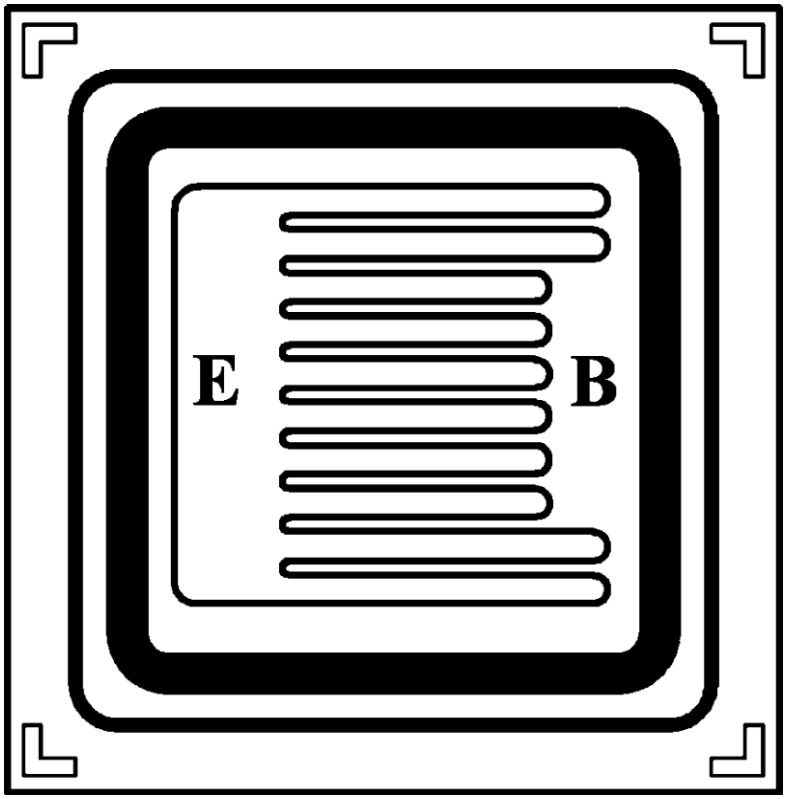
NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
4. Terminal 1 - collector, terminal 2 - base, terminal 3 - emitter.

FIGURE 3. Physical dimensions, surface mount (2N5666U3 version).



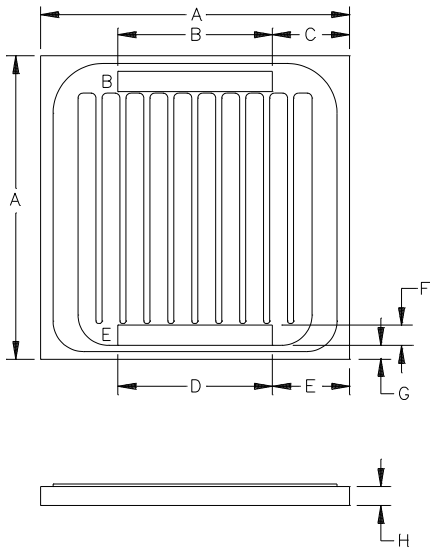
1. Chip size: .120 x .120 inch ±.002 inch (3.05 mm x 3.05 mm ±0.051 mm).
2. Chip thickness: .015 inch nominal, (0.381 mm).
3. Top metal: Aluminum 54kÅ minimum, 66kÅ nominal
4. Back metal: Al/Ti/Ni/Au10kÅ minimum, 12.5kÅ nominal.
5. Backside: Collector
6. Bonding pad: B = .038 x .022 inch (0.97 mm x 0.56 mm),
   E = .042 x .020 inch (1.07 mm x 0.51 mm).

FIGURE 4. JANHC and JANKC (A-version) die dimensions for 2N5665/2N5667.



1. Chip Size: .128 x .128 inch ± .002” (3.25 x 3.25 mm ±0.051 mm)
2. Chip Thickness: .015 inch nominal (0.381 mm)
3. Top Metal: Aluminum: 30KÅ min, 33KÅ nominal
4. Back Metal: Al/Ti/Ni/Au: 10KÅ min, 12.5KÅ nominal (totals)
5. Backside Contact: Collector
6. Bonding Pads: B = .052 x .012 inch (1.32 x 0.31 mm)
   E = .074 x .012 inch (1.88 x 0.31 mm)

FIGURE 5. JANHC and JANKC (A-version) die dimensions for 2N5664/2N5666.



Symbol	Dimensions			
	Inches		Millimeters	
A	.119	.123	3.02	3.12
B	.061	.065	1.55	1.65
C	.026	.031	0.66	0.79
D	.058	.062	1.47	1.57

Symbol	Dimensions			
	Inches		Millimeters	
E	.028	.032	0.71	0.81
F	.006	.010	0.15	0.25
G	.004	.008	0.10	0.20
H	.006	.010	0.15	0.25

1. Chip Size: 0.121 x 0.121 inch ± 0.002” (3.07 x 3.07 mm ± 0.051 mm)
2. Chip Thickness: 0.008 inch nominal (0.203 mm)
3. Top Metal: Aluminum: 17.5KÅ min, 20KÅ nominal
4. Back Metal: Au: 1.7KÅ min, 2.4KÅ nominal (totals)
5. Backside Contact: Collector
6. Bonding Pads: B = 0.063 x 0.008 inch (1.600 x 0.205 mm)
   E = 0.060 x 0.008 inch (1.535 x 0.205 mm)

FIGURE 6. JANHCB and JANKCB die dimensions for 2N5664 and 2N5666.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1 (TO-66), figure 2 (TO-5 and TO-39), figure 3 (surface mount), figure 4 (JANHC, JANKC 2N5665/2N5667), figure 5 (JANHC, JANKC 2N5664/2N5666), and figure 6 (JANHCB, JANKCB 2N5664/2N5666).

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Radiation hardness assurance (RHA). Radiation hardness assurance requirements, PIN designators, and test levels shall be as defined in MIL-PRF-19500.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in 4.4.2, 4.4.3, and 4.4.4, herein.

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500. When applicable, the radiation hardened designator M, D, P, L, R, F, G or H shall immediately precede (or replace) the device “2N” identifier (depending upon the degree of abbreviation required).

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I, II, and III).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table IV tests, the tests specified in table IV herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (list applicable JAN levels). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
(1) 3c	Thermal impedance method 3131 of MIL-STD-750, see 4.3.3.	Thermal impedance method 3131 of MIL-STD-750, see 4.3.3. (2)
9	I_{CES1} and h_{FE2}	I_{CES1}
11	I_{CES1} and $h_{FE2;}$ ΔI_{CES1} = 100 percent of initial value or 10 nA dc, whichever is greater; Δh_{FE2} = ±15 percent.	I_{CES1} and $h_{FE2;}$ ΔI_{CES1} = 100 percent of initial value or 20 nA dc, whichever is greater.
12	See 4.3.1.	See 4.3.1.
13	Subgroups 2 and 3 of table I herein; ΔI_{CES1} = +100 percent of initial value or 10 nA dc, whichever is greater. Δh_{FE2} = ±15 percent.	Subgroup 2 of table I herein; ΔI_{CES1} = +100 percent of initial value or 20 nA dc, whichever is greater. Δh_{FE2} = ±25 percent.

(1) Thermal impedance limits shall not exceed figures 12, 13, 14, and 15.
(2) Shall be performed any time after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: T_J = +187.5 ±12.5°C, V_{CE} = 100 V dc, applied P_T minimum of P_{T1} = 75 percent, $T_A \leq$ +55°C. Burn-in duration for lot acceptance for the JANKC level follows JANS requirements. Burn-in duration for lot acceptance for the JANHC level follows JANTX requirements.

4.3.2 Screening (JANHC and JANKC). Screening of JANHC and JANKC die shall be in accordance with MIL-PRF-19500. As a minimum, die shall be 100 percent probed to insure the assembled chips will meet the requirements of table I, subgroup 2.

* 4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, (and V_C where appropriate). The thermal impedance limit used in screen 3c of 4.3 and the subgroup 2 of table I herein shall comply with the thermal impedance graph on figures 12, 13, 14, and 15 (less than or equal to the curve value at the same t_H time) and shall be less than the process determined statistical maximum limit as outlined in method 3131. See table III, group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein. If alternate screening is being performed in accordance with E.5.3.1d of MIL-PRF-19500 a sample of screened devices shall be submitted to and pass the requirements of group A1 and A2 inspection only (table VIb, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and table I herein. End-point electrical measurements shall be in accordance with table I, subgroup 2.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and 4.4.2.1 and 4.4.2.2 herein. Delta measurements shall be in accordance with the steps in table II herein as specified in the notes for table II.

4.4.2.1 Group B inspection, table E-VIA (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
B4	1037	V_{CB} = 30 V dc minimum, T_A = +25°C ±3°C; t_{on} = t_{off} = 3 minutes minimum. No heat sink or forced-air cooling on the heating cycle shall be permitted.
B5	1027	See 4.5.3 herein.

4.4.2.2 Group B inspection, table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

Subgroup	Method	Condition
B3	1027	T_J = +187.5°C ±12.5°C, V_{CE} = 100 ±5 V dc; T_A = ≤ +55°C. The applied P_T minimum of P_{T1} = 75 percent.
B5	3131	Not applicable.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and herein. Delta measurements shall be in accordance with the steps in table II herein and as specified in the notes for table II.

Subgroup	Method	Condition
C2	2036	Terminal strength (tension) 2N5664 and 2N5665 only: Test condition A, weight = 10 pounds, application time = 15 seconds. Terminal strength (lead fatigue) 2N5666, 2N5666S, 2N5667, and 2N5667S only: Test condition E (not applicable to 2N5666U3).
C5	3131	See 1.3 and 4.3.3 herein.
C6	1026	T_J = +187.5°C ±12.5°C, V_{CE} = 100 ±5 V dc; T_A = ≤ +55°C. The applied P_T minimum of P_{T1} = 75 percent.

4.4.4 Group D inspection. Conformance Inspection for hardness assured JANTXV, JANS, and JANKC types shall include the group D tests specified in table III herein. These tests shall be performed as required in accordance with MIL-PRF-19500 and method 1019 of MIL-STD-750, for total ionizing dose, or method 1017 of MIL-STD-750 for neutron fluence, as applicable (see 6.2.e herein), except group D subgroup 2 may be performed separately from other subgroups. Alternate package options may also be substituted for the testing provided there is no adverse effect to the fluence profile.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table IV herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein; delta measurements shall be in accordance with the applicable steps of table II.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Inspection conditions. Unless otherwise specified herein, all inspections shall be conducted at a case temperature (T_C) of +25°C.

4.5.3 Group B accelerated life test. This test shall be conducted using one of the four options listed herein (a, b, c, or d) with the following conditions applying to all options: V_{CB} = 30 V dc.

a. T_A = +150°C, maximum, t = 96 hours minimum, T_J = +275°C.

b. P_T = 2.5 W (TO-66); P_T = 1.2 W (TO-5, U3 suffix), T_A = +112°C or P_T adjusted to give a lot average of T_J = +275°C, t = 96 hours minimum, T_J = +275°C.

c. T_A = +25°C +3 °C with P_T adjusted to give a lot average of T_J = +275°C, t = 96 hours minimum, T_J = +275°C.

d. Adjust T_A or P_D to achieve a T_J = +225°C minimum. t = 216 hours, n = 45, c = 0.

TABLE I. Group A inspection.

	Inspection 1/ 2/	MIL-STD-750		Symbol	Limits		Unit
		Method	Conditions		Min	Max	
	Subgroup 1						
	Visual and mechanical inspection	2071					
	Subgroup 2						
*	Thermal impedance 3/	3131	See 4.3.3	$Z_{\theta JX}$			°C/W
	Breakdown voltage collector to emitter	3011	Bias condition B; I_C = 10 mA dc, pulsed (see 4.5.1), R_1 = 100 Ω	$V_{(BR)CER}$			
	2N5664, 2N5666, 2N5666S				250		V dc
	2N5665, 2N5667, 2N5667S				400		V dc
	Breakdown voltage emitter to base	3026	Bias condition D, I_E = 10 µA dc, pulsed (see 4.5.1)	$V_{(BR)EBO}$	6		V dc
	Collector to emitter cutoff current	3041	Bias condition C	I_{CES1}		0.2	µA dc
	2N5664, 2N5666, 2N5666S		V_{CE} = 200 V dc				
	2N5665, 2N5667, 2N5667S		V_{CE} = 300 V dc				
	Collector to base cutoff current	3036	Bias condition D	I_{CBO}			
	2N5664, 2N5666, 2N5666S		V_{CB} = 200 V dc			0.1	µA dc
	2N5664, 2N5666, 2N5666S		V_{CB} = 250 V dc			1.0	mA dc
	2N5665, 2N5667, 2N5667S		V_{CB} = 300 V dc			0.1	µA dc
	2N5665, 2N5667, 2N5667S		V_{CB} = 400 V dc			1.0	mA dc
	Forward-current transfer ratio	3076	V_{CE} = 2 V dc, I_C = 0.5 A dc pulsed (see 4.5.1)	h_{FE1}			
	2N5664, 2N5666, 2N5666S				40		
	2N5665, 2N5667, 2N5667S				25		
	Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 1.0 A dc pulsed (see 4.5.1)	h_{FE2}			
	2N5664, 2N5666, 2N5666S				40	120	
	2N5665, 2N5667, 2N5667S				25	75	
	Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 3.0 A dc pulsed (see 4.5.1)	h_{FE3}			
	2N5664, 2N5666, 2N5666S				15		
	2N5665, 2N5667, 2N5667S				10		

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/ 2/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued						
Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 5 A dc, pulsed (see 4.5.1)	h_{FE4}	5		
Collector-emitter saturation voltage	3071	I_C = 3.0 A dc,	$V_{CE(sat)1}$		0.4	V dc
2N5664, 2N5666, 2N5666S		I_B = 0.3 A dc, pulsed (see 4.5.1)				
2N5665, 2N5667, 2N5667S		I_B = 0.6 A dc, pulsed (see 4.5.1)				
Collector-emitter saturation voltage	3071	I_C = 5 A dc, I_B = 1 A dc, pulsed (see 4.5.1)	$V_{CE(sat)2}$ 4/		1.0	V dc
Base-emitter saturation voltage	3066	Test condition A, I_C = 3.0 A dc,	$V_{BE(sat)1}$ 4/		1.2	V dc
2N5664, 2N5666, 2N5666S		I_B = 0.3 A dc, pulsed (see 4.5.1)				
2N5665, 2N5667, 2N5667S		I_B = 0.6 A dc, pulsed (see 4.5.1)				
Base-emitter saturation voltage	3066	Test condition A, I_C = 5 A dc, I_B = 1 A dc, pulsed (see 4.5.1)	$V_{BE(sat)2}$		1.5	V dc
Subgroup 3						
High-temperature operation:		T_A = + 150°C				
Collector to emitter cutoff current	3041	Bias condition C	I_{CES2}		100	µA dc
2N5664, 2N5666, 2N5666S		V_{CE} = 200 V dc				
2N5665, 2N5667, 2N5667S		V_{CE} = 300 V dc				
Low-temperature operation:		T_A = -55°C				
Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 1.0 A dc, pulsed (see 4.5.1)	h_{FE5}			
2N5664, 2N5666, 2N5666S				15		
2N5665, 2N5667, 2N5667S				10		

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/ 2/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 4						
Magnitude of common-emitter, small-signal short-circuit, forward-current, transfer ratio	3306	V_{CE} = 5 V dc, I_C = 0.5 A dc, f = 10 MHz	$\lvert h_{fe} \rvert$	2.0	7.0	
Open-circuit output capacitance	3236	V_{CB} = 10 V dc, 100 kHz ≤ f ≤ 1 MHz	C_{obo}		120	pF
Pulse response						
Turn-on time	3251	Test condition A; I_C = 1.0 A dc, V_{CC} = 100 V dc	t_{on}		0.25	µs
2N5664, 2N5666, 2N5666S		See figure 16				
2N5665, 2N5667, 2N5667S		See figure 17				
Turn-off time	3251	Test condition A; I_C = 1.0 A dc, V_{CC} = 100 V dc	t_{off}			
2N5664, 2N5666, 2N5666S		See figure 16			1.5	µs
2N5665, 2N5667, 2N5667S		See figure 17			2.0	µs
Subgroup 5						
Safe operating area (continuous dc) (for types 2N5664 and 2N5665 only)	3051	T_C = + 100°C, t ≥ 1 s, 1 cycle; $t_r + t_f$ = 10 µs (see figure 18)				
Test #1 2N5664 and 2N5665		V_{CE} = 6 V dc, I_C = 5 A dc				
Test #2						
2N5664		V_{CE} = 32 V dc, I_C = 0.75 A dc				
2N5665		V_{CE} = 40 V dc, I_C = 0.75 A dc				
Test #3						
2N5664		V_{CE} = 200 V dc, I_C = 29 mA dc				
2N5665		V_{CE} = 300 V dc, I_C = 21 mA dc				

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/ 2/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 5 - Continued						
Safe operating area (continuous dc) (for types 2N5666, 2N5666S, 2N5667, and 2N5667S	3051	T_C = +100°C, t ≥ 1 s, 1 cycle; $t_r + t_f$ = 10 μs (see figure 19)				
Test #1 2N5666, 2N5666S, 2N5667, and 2N5667S		V_{CE} = 3.0 V dc, I_C = 5 A dc				
Test #2 2N5666 and 2N5666S 2N5667 and 2N5667S		V_{CE} = 29 V dc, I_C = 0.4 A dc V_{CE} = 37.5 V dc, I_C = 0.4 A dc				
Test #3 2N5666 and 2N5666S 2N5667 and 2N5667S		V_{CE} = 200 V dc, I_C = 19 mA dc V_{CE} = 300 V dc, I_C = 14 mA dc				
Safe operating area (switching)	3053	Load condition B (clamped inductive load) (see figure 20); T_C = + 100°C, $t_r + t_f \leq 10$ μs, duty cycle ≤ 2 percent; t_p = 4 ms; R_S = 0.5 Ω, R_{BB1} = 50 Ω, V_{BB1} = 50 V dc, R_{BB2} = 50 Ω, V_{BB2} = -4 V dc, I_C = 5 A dc, V_{CC} = 50 V dc, $R_L \leq 2.5$ Ω, L = 40 mH (Triad C-48U or equivalent)				
2N5664, 2N5666, and 2N5666S		Clamp voltage = 200 +0, -5 V dc				
2N5665, 2N5667, and 2N5667S		Clamp voltage = 300 +0, -5 V dc				
End-point electrical measurements		See table I, group A, subgroup 2 herein				
Subgroups 6 and 7						
Not applicable						

1/ For sampling plan, see MIL-PRF-19500.
2/ Electrical characteristics for 2N5666U3 are identical to 2N5666 unless otherwise noted.
3/ This test required for the following end-point measurements only:
Group B, subgroups 3, 4 and 5 (JANS).
Group B, subgroups 2 and 3 (JAN, JANTX, JANTXV).
Group C, subgroups 2 and 6.
Group E, subgroup 1.
4/ Measured at less than .125 inch (3.175 mm) from case.

TABLE II. Groups B, C, and E delta measurements. 1/ 2/ 3/ 4/

Steps	Inspection	MIL-STD-750		Symbol	Limits		Unit
		Method	Conditions		Min	Max	
1.	Collector to emitter cutoff current	3041	Base condition C	ΔI_{CES1}	100 percent of initial value or 20 nA dc, whichever is greater.		
	2N5664, 2N5666, 2N5666S, and 2N5666U3		V_{CE} = 200 V dc				
	2N5665, 2N5667, 2N5667S		V_{CE} = 300 V dc				
2.	Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 1.0 A dc pulsed (see 4.5.1)	Δh_{FE2} 5/	±25 percent change from initial reading.		

1/ The delta measurements for table E-VIA (JANS) of MIL-PRF-19500 are after subgroups 4 and 5, and consist of steps 1 and 2 of table II herein.
2/ The delta measurements for table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500 are as follows: Subgroups 3 and 6, see table II herein, steps 1 and 2.
3/ The delta measurements for table E-VII of MIL-PRF-19500 are as follows: Subgroup 6, see table II herein, steps 1 and 2.
4/ The delta measurements for table E-IX of MIL-PRF-19500 are as follows: Subgroups 1 and 2, see table II herein, steps 1 and 2.
5/ Measured at less than .125 inch (3.175 mm) from case.

TABLE III. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1 4/						
Neutron irradiation	1017	Neutron exposure, Vces = 0 V				
Breakdown voltage collector to emitter	3011	Bias condition B; I_C = 10 mA dc, pulsed (see 4.5.1), R_1 = 100 Ω	$V_{(BR)CER}$			
2N5664, 2N5666, 2N5666S				250		V dc
2N5665, 2N5667, 2N5667S				400		V dc
Breakdown voltage emitter to base	3026	Bias condition D, I_E = 10 μA dc, pulsed (see 4.5.1)	$V_{(BR)EBO}$	6		V dc
Collector to emitter cutoff current	3041	Bias condition C	I_{CES1}		0.4	μA dc
2N5664, 2N5666, 2N5666S		V_{CE} = 200 V dc				
2N5665, 2N5667, 2N5667S		V_{CE} = 300 V dc				
Collector to base cutoff current	3036	Bias condition D	I_{CBO}			
2N5664, 2N5666, 2N5666S		V_{CB} = 200 V dc			0.2	μA dc
2N5664, 2N5666, 2N5666S		V_{CB} = 250 V dc			2.0	mA dc
2N5665, 2N5667, 2N5667S		V_{CB} = 300 V dc			0.2	μA dc
2N5665, 2N5667, 2N5667S		V_{CB} = 400 V dc			2.0	mA dc
Forward-current transfer ratio	3076	V_{CE} = 2 V dc, I_C = 0.5 A dc pulsed (see 4.5.1)	$[h_{FE1}]$ 5/			
2N5664, 2N5666, 2N5666S				[20]		
2N5665, 2N5667, 2N5667S				[12.5]		
Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 1.0 A dc pulsed (see 4.5.1)	$[h_{FE2}]$ 5/			
2N5664, 2N5666, 2N5666S				[20]	120	
2N5665, 2N5667, 2N5667S				[12.5]	75	
Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 3.0 A dc pulsed (see 4.5.1)	$[h_{FE3}]$ 5/			
2N5664, 2N5666, 2N5666S				[7.5]		
2N5665, 2N5667, 2N5667S				[5]		
Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 5 A dc, pulsed (see 4.5.1)	$[h_{FE4}]$ 5/	2.5		
Collector-emitter saturation voltage	3071	I_C = 3.0 A dc,	$V_{CE(sat)1}$		0.46	V dc
2N5664, 2N5666, 2N5666S		I_B = 0.3 A dc, pulsed (see 4.5.1)				
2N5665, 2N5667, 2N5667S		I_B = 0.6 A dc, pulsed (see 4.5.1)				

See footnotes at end of table.

TABLE III. Group D inspection - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1 - Continued 4/						
Collector-emitter saturation voltage	3071	I_C = 5 A dc, I_B = 1 A dc, pulsed (see 4.5.1)	$V_{CE(sat)2}$		1.15	V dc
Base-emitter saturation voltage 2N5664, 2N5666, 2N5666S 2N5665, 2N5667, 2N5667S	3066	Test condition A, I_C = 3.0 A dc, pulsed (see 4.5.1) I_B = 0.3 A dc I_B = 0.6 A dc	$V_{BE(sat)1}$		1.38	V dc
Base-emitter saturation voltage	3066	Test condition A, I_C = 5 A dc, I_B = 1 A dc, pulsed (see 4.5.1)	$V_{BE(sat)2}$		1.73	V dc
Subgroup 2		Gamma exposure				
Total dose irradiation	1019	Vces = 160 V for 2N5664, 2N5666, 2N5666S Vces = 240 V for 2N5665, 2N5667, 2N5667S				
Breakdown voltage collector to emitter 2N5664, 2N5666, 2N5666S 2N5665, 2N5667, 2N5667S	3011	Bias condition B; I_C = 10 mA dc, pulsed (see 4.5.1), R_1 = 100 Ω	$V_{(BR)CER}$	 250 400		 V dc V dc
Breakdown voltage emitter to base	3026	Bias condition D, I_E = 10 μA dc, pulsed (see 4.5.1)	$V_{(BR)EBO}$	6		V dc
Collector to emitter cutoff current 2N5664, 2N5666, 2N5666S 2N5665, 2N5667, 2N5667S	3041	Bias condition C V_{CE} = 200 V dc V_{CE} = 300 V dc	I_{CES1}		0.4	μA dc
Collector to base cutoff current 2N5664, 2N5666, 2N5666S 2N5664, 2N5666, 2N5666S 2N5665, 2N5667, 2N5667S 2N5665, 2N5667, 2N5667S	3036	Bias condition D V_{CB} = 200 V dc V_{CB} = 250 V dc V_{CB} = 300 V dc V_{CB} = 400 V dc	I_{CBO}		 0.2 2.0 0.2 2.0	 μA dc mA dc μA dc mA dc
Forward-current transfer ratio 2N5664, 2N5666, 2N5666S 2N5665, 2N5667, 2N5667S	3076	V_{CE} = 2 V dc, I_C = 0.5 A dc pulsed (see 4.5.1)	$[h_{FE1}]$ 5/	 [20] [12.5]		

See footnotes at end of table.

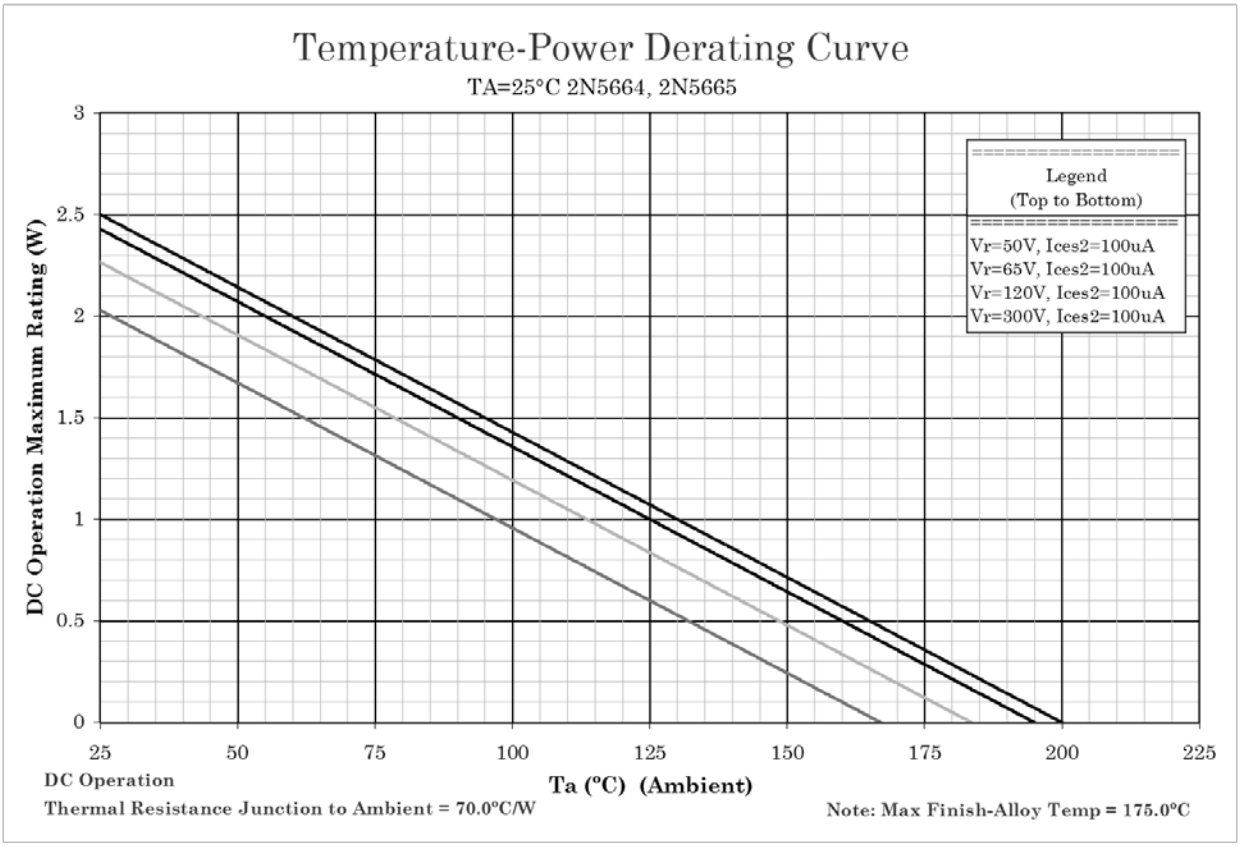
TABLE III. Group D inspection - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued.						
Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 1.0 A dc pulsed (see 4.5.1)	[h_{FE2}] 5/			
2N5664, 2N5666, 2N5666S				[20]	120	
2N5665, 2N5667, 2N5667S				[12.5]	75	
Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 3.0 A dc pulsed (see 4.5.1)	[h_{FE3}] 5/			
2N5664, 2N5666, 2N5666S				[7.5]		
2N5665, 2N5667, 2N5667S				[5]		
Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 5 A dc, pulsed (see 4.5.1)	[h_{FE4}] 5/	[2.5]		
Collector-emitter saturation voltage	3071	I_C = 3.0 A dc, pulsed (see 4.5.1)	$V_{CE(sat)1}$		0.46	V dc
2N5664, 2N5666, 2N5666S		I_B = 0.3 A dc				
2N5665, 2N5667, 2N5667S		I_B = 0.6 A dc				
Collector-emitter saturation voltage	3071	I_C = 5 A dc, I_B = 1 A dc, pulsed (see 4.5.1)	$V_{CE(sat)2}$		1.15	V dc
Base-emitter saturation voltage	3066	Test condition A, I_C = 3.0 A dc, pulsed (see 4.5.1)	$V_{BE(sat)1}$		1.38	V dc
2N5664, 2N5666, 2N5666S		I_B = 0.3 A dc				
2N5665, 2N5667, 2N5667S		I_B = 0.6 A dc				
Base-emitter saturation voltage	3066	Test condition A, I_C = 5 A dc, I_B = 1 A dc, pulsed (see 4.5.1)	$V_{BE(sat)2}$		1.73	V dc

1/ Tests to be performed on all devices receiving radiation exposure.
2/ For sampling plan, see MIL-PRF-19500.
3/ Electrical characteristics apply to all device types unless otherwise noted.
4/ Subgroup 1 is an optional test and shall be specified on the contract or order when required.
5/ See method 1019 of MIL-STD-750 for how to determine [h_{FE}] by first calculating the delta($1/h_{FE}$) from the pre- and post-radiation h_{FE}. Notice that [h_{FE}] is not the same as h_{FE} and cannot be measured directly. The [h_{FE}] value can never exceed the pre-radiation minimum h_{FE} that it is based upon.

TABLE IV. Group E inspection (all quality levels) - for qualification only.

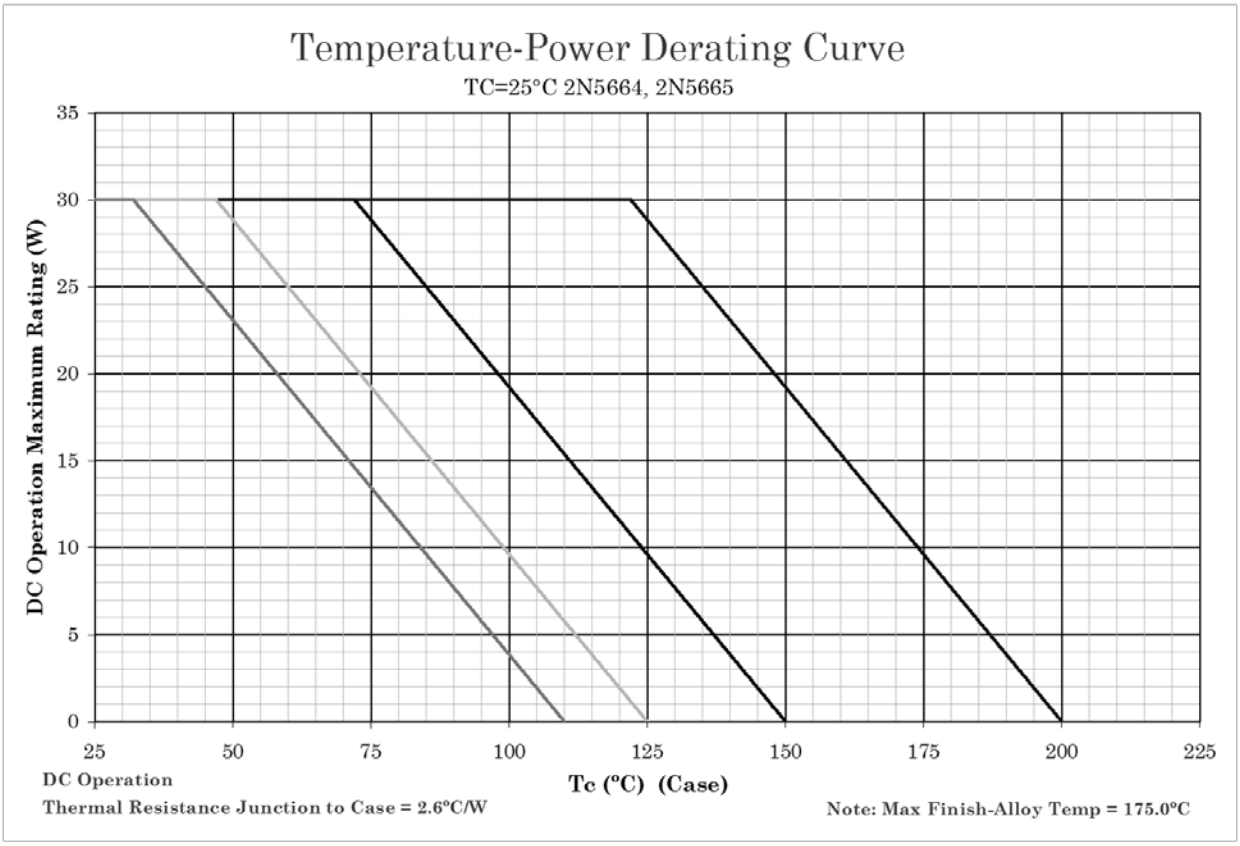
Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles.	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2 and table II, step 1 and 2.	
Subgroup 2			45 devices c = 0
Intermittent life	1037	V_{CB} = 10 V dc, 6,000 cycles.	
Electrical measurements		See table I, subgroup 2 and table II, step 1 and 2 herein.	
Subgroup 4			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 5			3 devices, c = 0
Barometric pressure (reduced)	1001	Normal mounting pressure = 8 mm Hg ±2 mm Hg for 60 s (minimum) Unless otherwise specified, the device shall be subjected to the maximum voltage it would be subjected to under rated operating conditions.	
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition A for devices ≥ 400 V, Condition B for devices < 400 V.	



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Top derate design curve constrained by the maximum junction temperature ($T_J \leq +200°C$) and power rating specified and a maximum dc voltage of 50 V. (See 1.3 herein.)
3. Second derate design curve chosen for a maximum dc voltage of 65 V.
4. Third derate design curve chosen for a maximum dc voltage of 120 V.
5. Fourth and bottom derate design curve chosen for the maximum rated dc voltage of 300 V.
6. All four curves show the predicted effects of high voltage dc operation for devices with leakage running at the Ices2 maximum rated limited with free air cooling to prevent thermal runaway. Improved cooling or lower duty cycles will, increase the maximum voltage to be used as illustrated in the other case mounted derating curve sets.

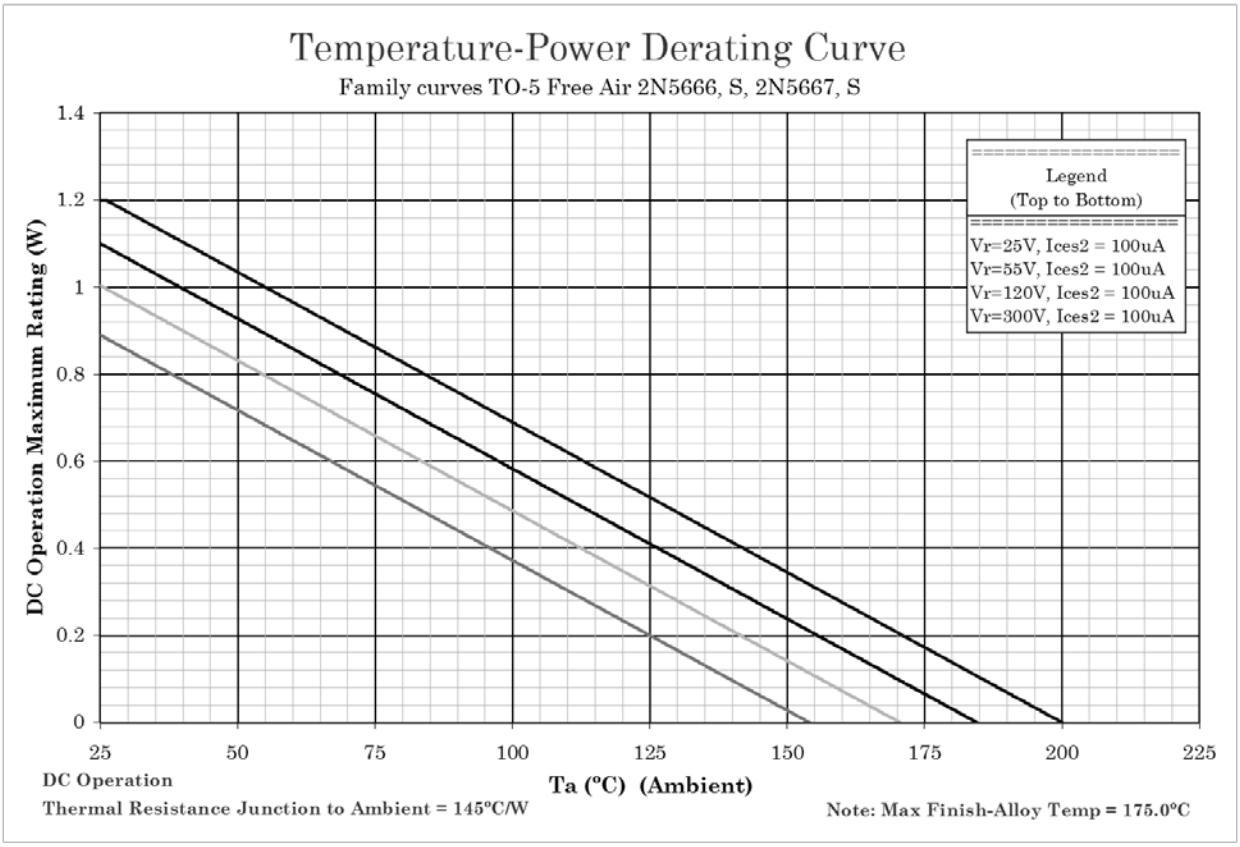
FIGURE 7. Temperature-power derating for 2N5664 and 2N5665.



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ +200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ +150°C where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ +125°C and +110°C to show power rating where most users want to limit T_J in their application.

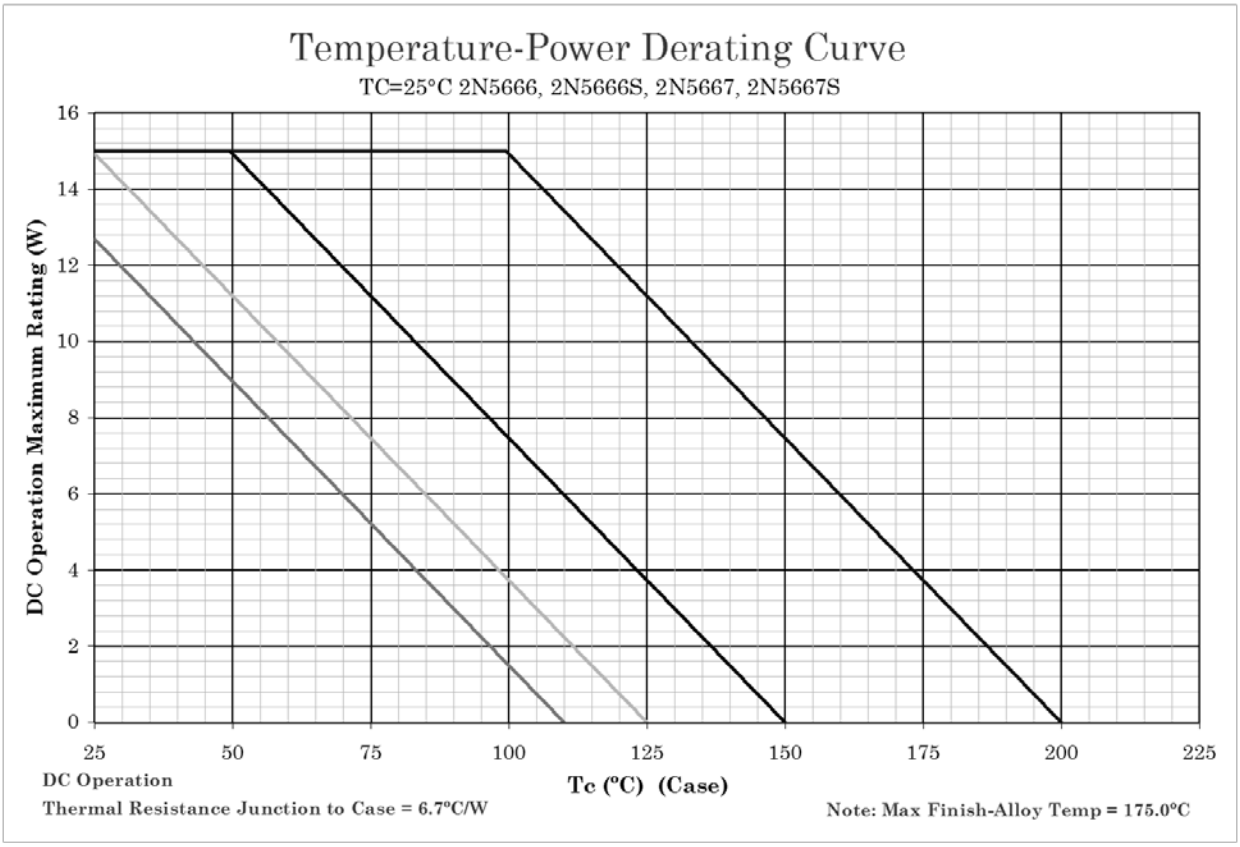
FIGURE 8. Temperature-power derating for 2N5664 and 2N5665.



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Top derate design curve constrained by the maximum junction temperature ($T_J \leq +200°C$) and power rating specified and a maximum dc voltage of 25 V. (See 1.3 herein.)
3. Second derate design curve chosen for a maximum dc voltage of 55 V.
4. Third derate design curve chosen for a maximum dc voltage of 120 V.
5. Fourth and bottom derate design curve chosen for the maximum rated dc voltage of 300 V.
6. All four curves show the predicted effects of high voltage dc operation for devices with leakage running at the Ices2 maximum rated limited with free air cooling to prevent thermal runaway. Improved cooling or lower duty cycles will, increase the maximum voltage to be used as illustrated in the other case mounted derating curve sets.

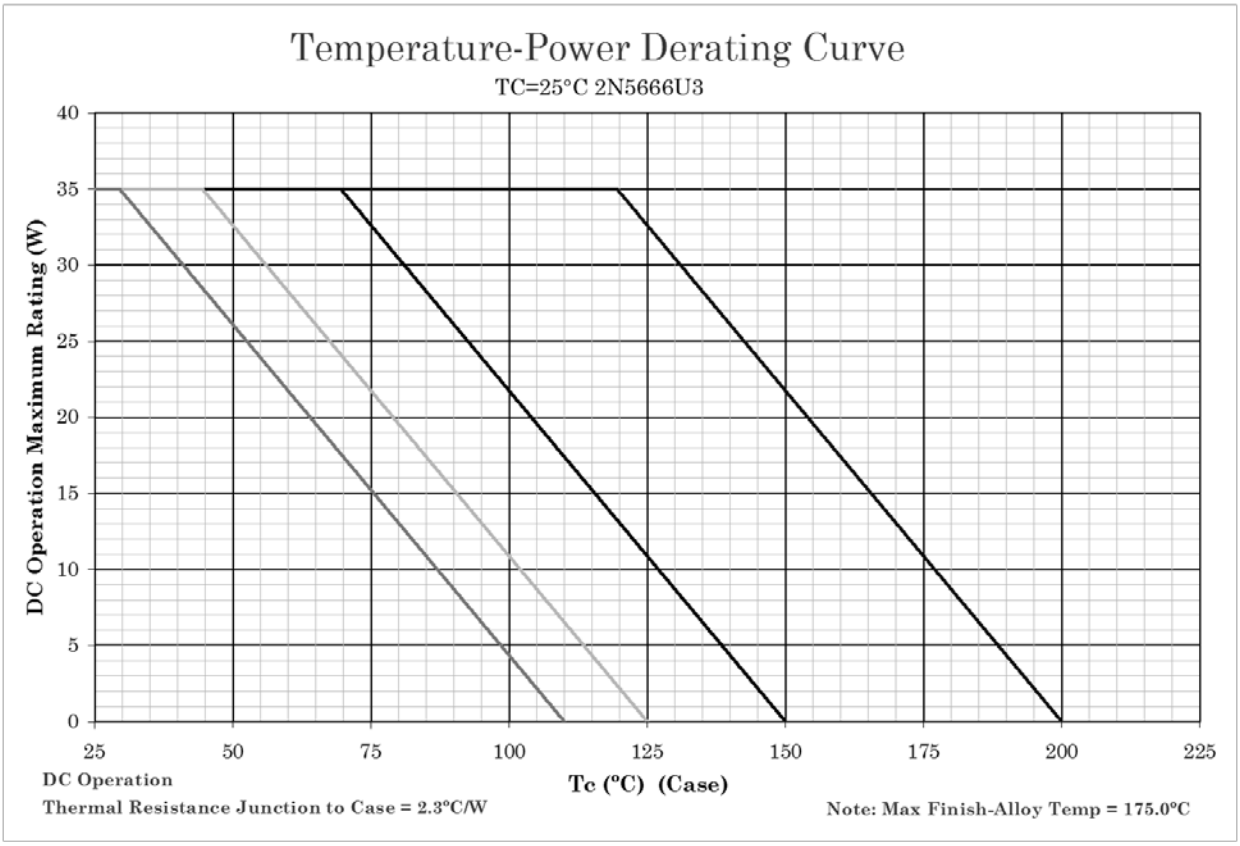
FIGURE 9. Temperature-power derating for 2N5666, 2N5666S, 2N5667, and 2N5667S.



NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq +200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150°C$ where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq +125°C$ and +110°C to show power rating where most users want to limit T_J in their application.

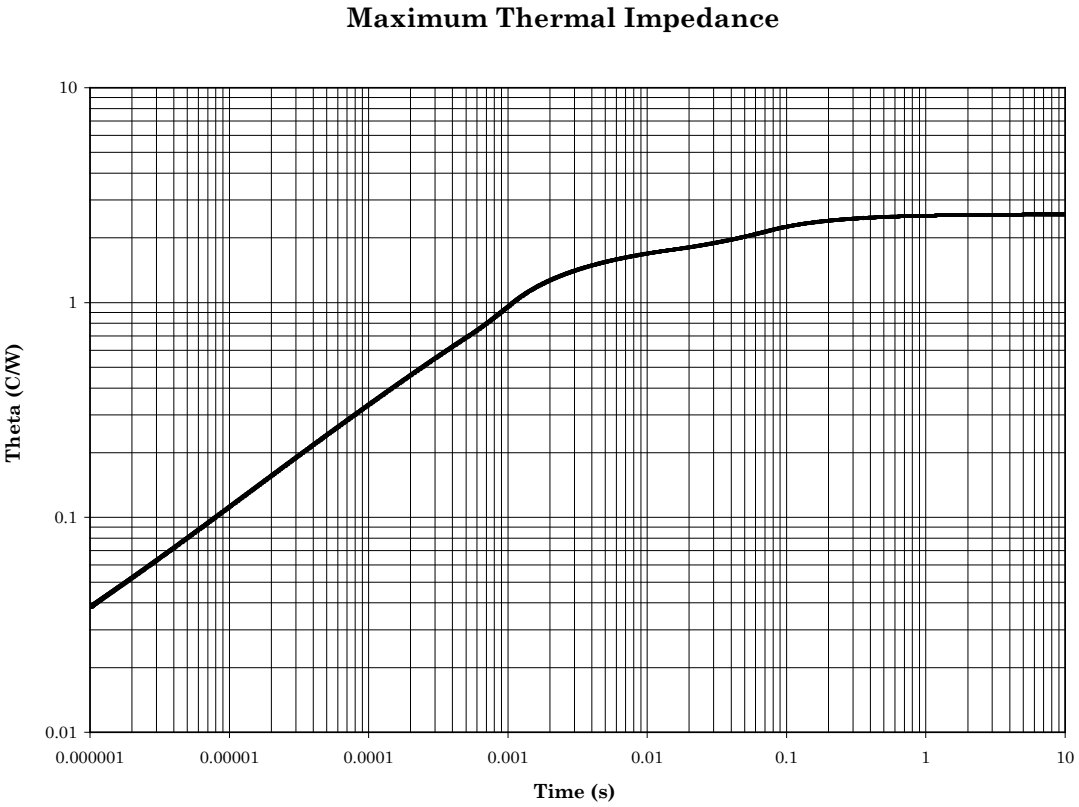
FIGURE 10. Temperature-power derating for 2N5666, 2N5666S, 2N5667, and 2N5667S.



NOTES:

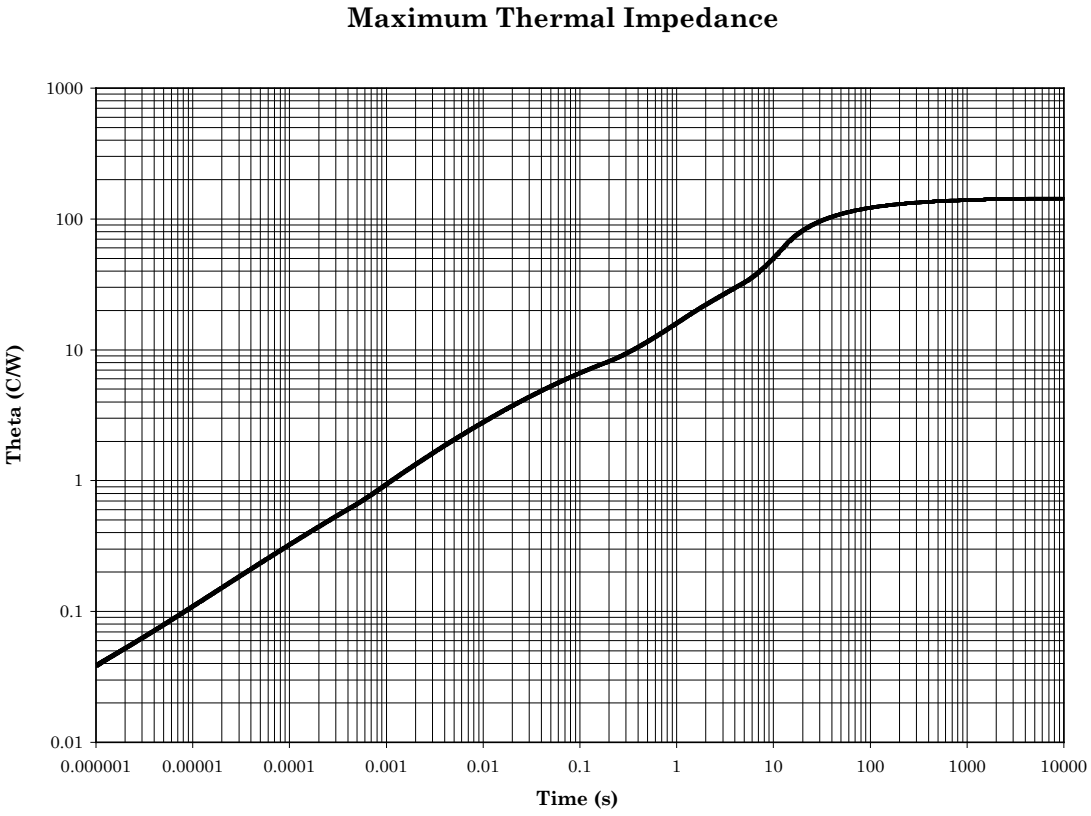
1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq +200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150°C$ where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq +125°C$ and +110°C to show power rating where most users want to limit T_J in their application.

FIGURE 11. Temperature-power derating for 2N5666U3.



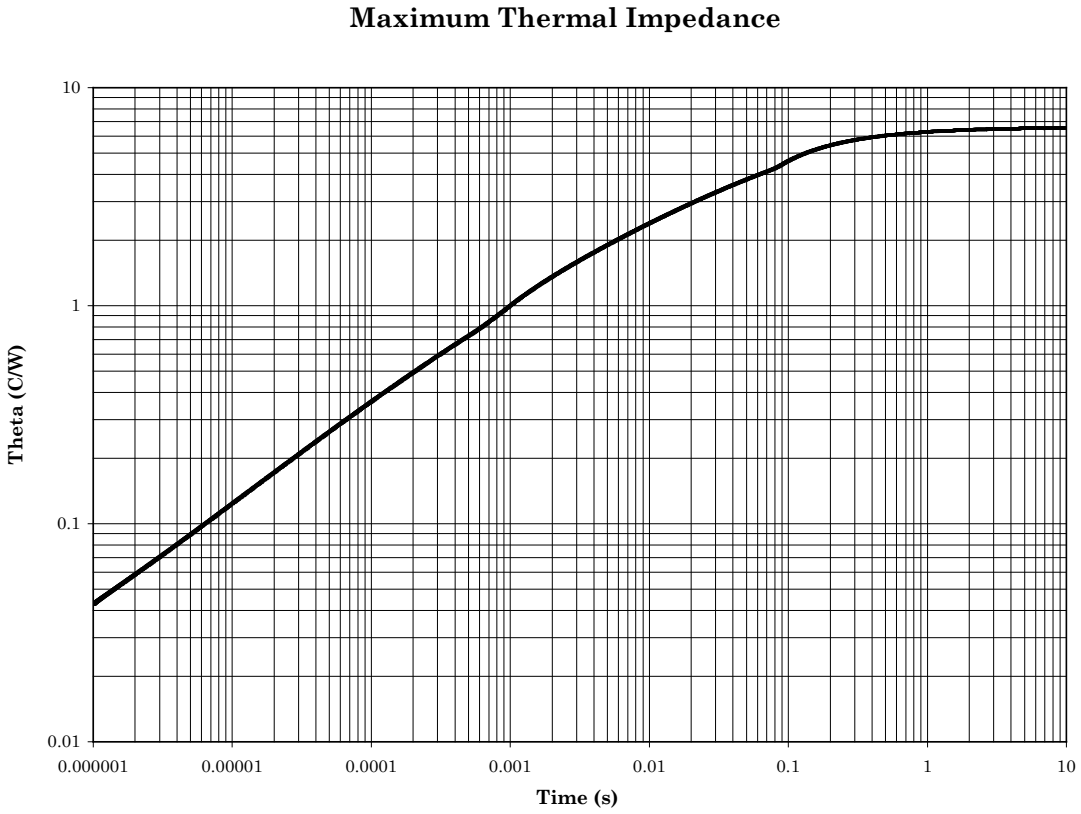
Solder mounted to copper heatsink at T_C = +25°C, thermal resistance = 2.6°C/W.

FIGURE 12. Thermal impedance graph ($R_{\theta JC}$) for 2N5664 and 2N5665 (TO-66).



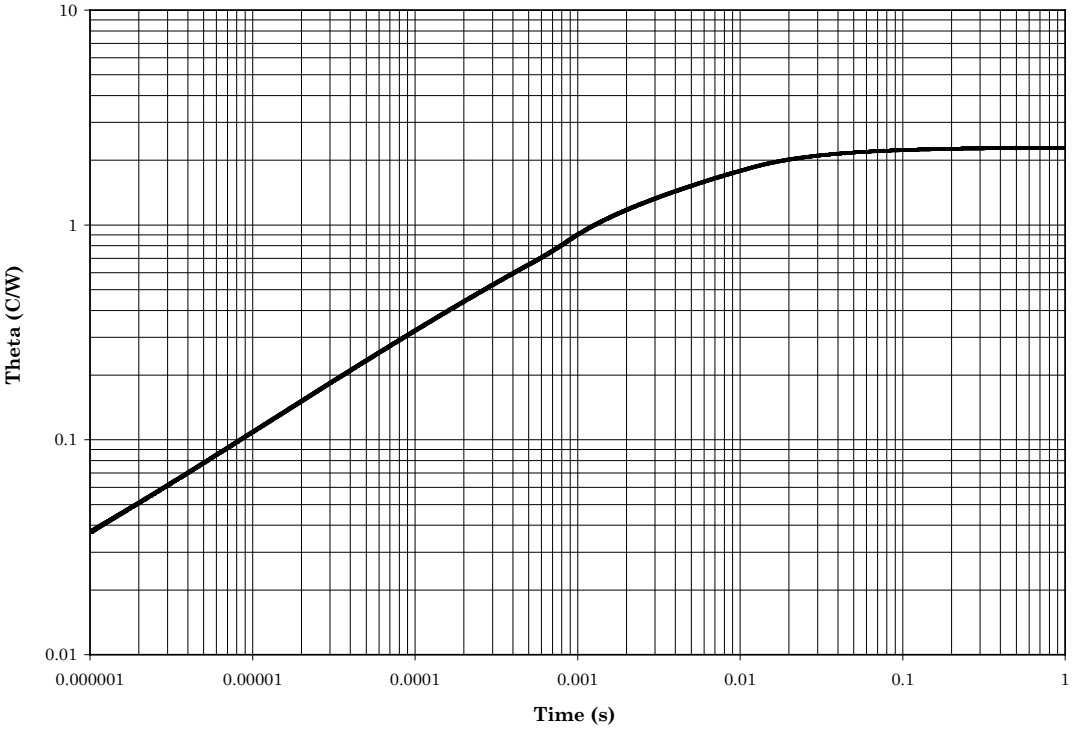
T_A = +25°C, thermal resistance $R_{\theta JA}$ = 145°C/W (ambient thermal resistance varies with power).

FIGURE 13. Thermal impedance graph ($R_{\theta JA}$) for 2N5666, 2N5666S, 2N5667, and 2N5667S (TO-5 and TO-39).



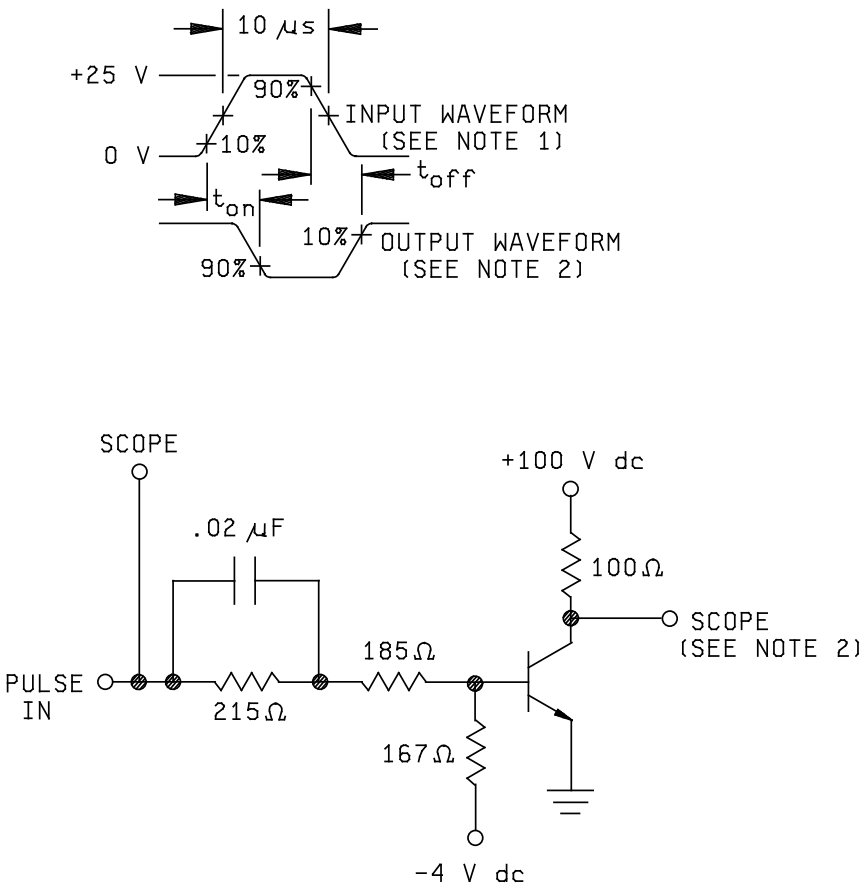
Solder mounted to copper heatsink at Tc = +25˚C, thermal resistance $R_{\theta JC}$ = 6.7 ˚C/W.

FIGURE 14. Thermal impedance graph ($R_{\theta JC}$) for 2N5666, 2N5666S, 2N5667, and 2N5667S.



Solder mounted to copper heatsink at T_C = +25°C, thermal resistance $R_{\theta JC}$ = 2.3°C/W.

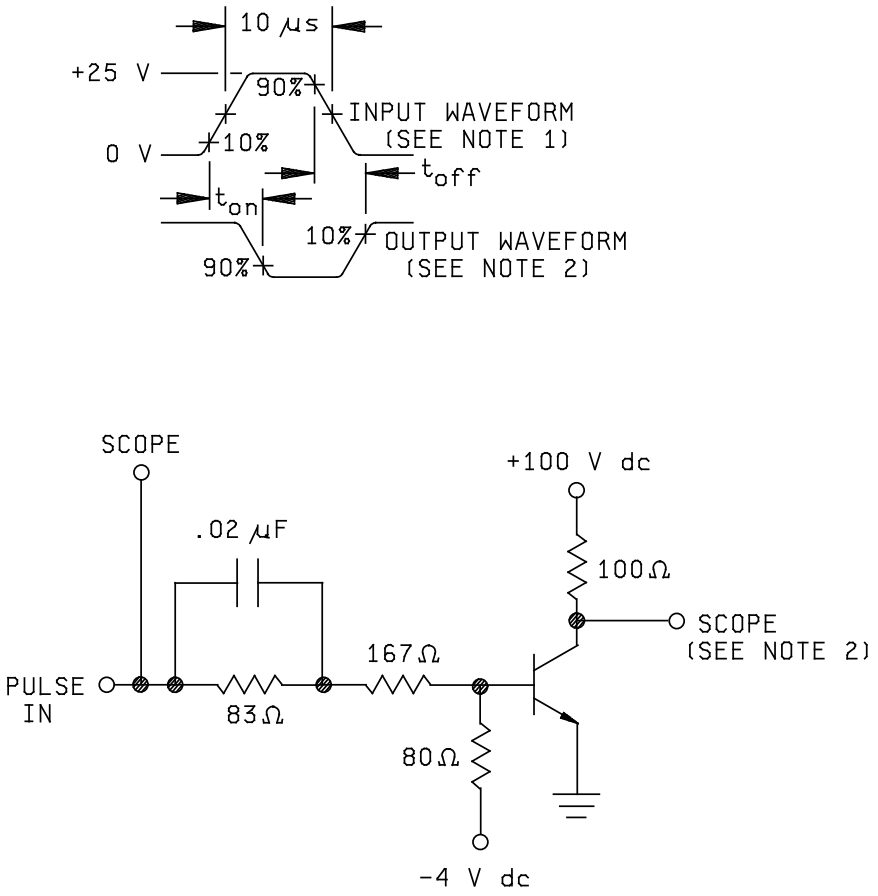
FIGURE 15. Thermal impedance graph ($R_{\theta JC}$) for 2N5666U3.



NOTES:

1. The input waveform is supplied by a pulse generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{out} = 50$ ohm, PW = 10 µs, duty cycle ≤ 2 percent.
2. Output waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $Z_{in} \geq 10$ M Ω, $C_{in} \leq 11.5$ pF.
3. Resistors shall be noninductive types.
4. The dc power supplies may require additional bypassing in order to minimize ringing.
5. The input pulse voltages and supply voltages (-4 V dc and +100 V dc) are nominal and shall be adjusted to obtain $I_{B1} = - I_{B2} = 30$ mA and $I_C = 1$ A.
6. An equivalent circuit may be used.
7. 0.02 µF capacitor may be removed during voltage adjustments.

FIGURE 16. Pulse response test circuit for types 2N5664, 2N5666, 2N5666S, and 2N5666U3.



NOTES:

1. The input waveform is supplied by a pulse generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{out} = 50$ ohm, PW = 10 µs, duty cycle ≤ 2 percent.
2. Output waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $Z_{in} \geq 10$ MΩ, $C_{in} \leq 11.5$ pF.
3. Resistors shall be noninductive types.
4. The dc power supplies may require additional bypassing in order to minimize ringing.
5. The input pulse voltages and supply voltages (-4 V dc and +100 V dc) are nominal and shall be adjusted to obtain $I_{B1} = - I_{B2} = 50$ mA and $I_C = 1$ A.
6. An equivalent circuit may be used.
7. 0.02 µF capacitor may be removed during voltage adjustments.

FIGURE 17. Pulse response test circuit for types 2N5665, 2N5667, and 2N5667S.

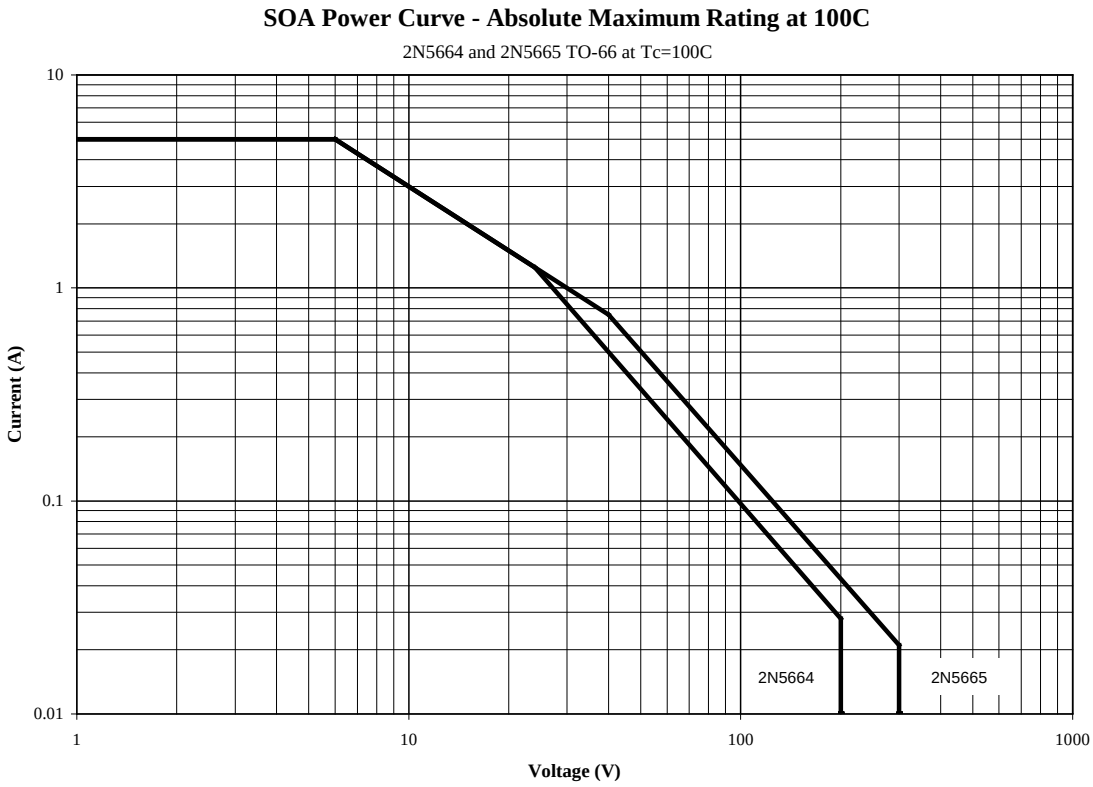
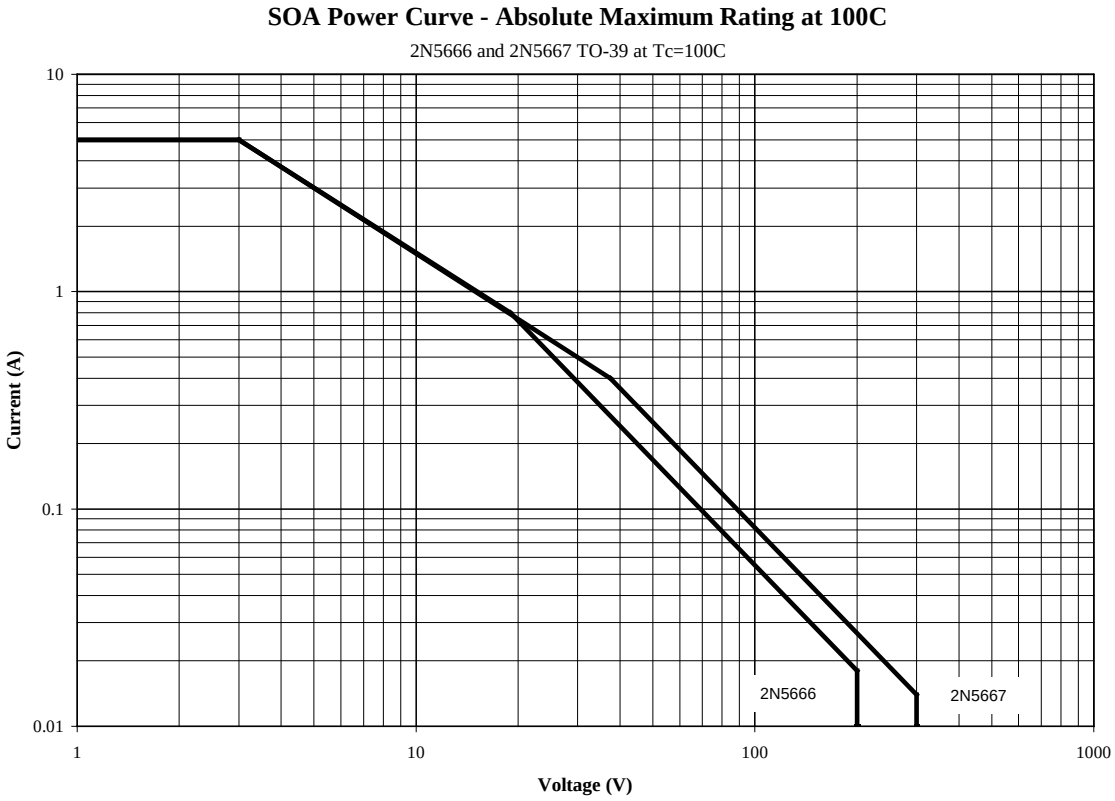
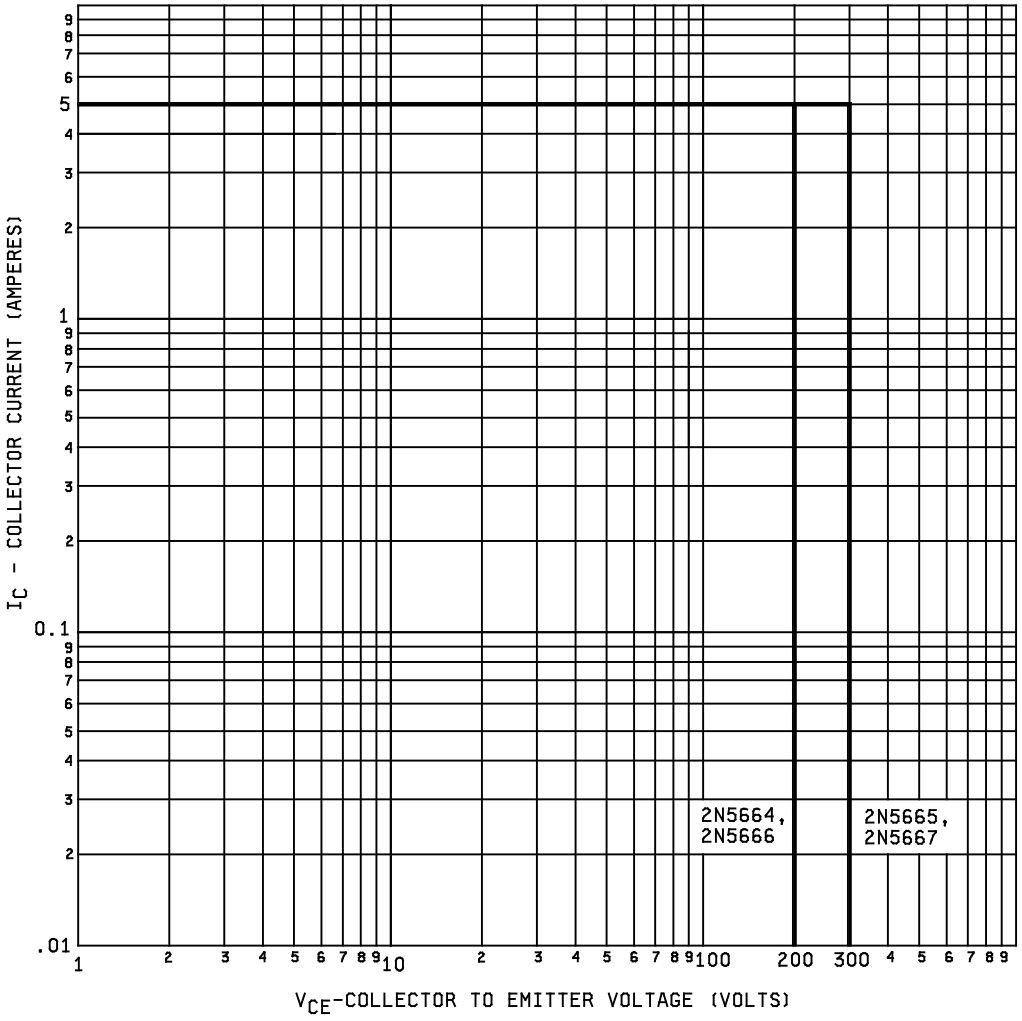


FIGURE 18. Maximum safe operating graph (continuous dc) for types 2N5664 and 2N5665.



NOTE: Electrical characteristics for "S" and "U3" suffix devices are identical to their corresponding devices without the suffix.

FIGURE 19. Maximum safe operating graph (continuous dc) for types 2N5666, 2N5666S, 2N5666U3, 2N5667, and 2N5667S.



NOTE: Electrical characteristics for "S" and "U3" suffix devices are identical to their corresponding devices without the suffix.

FIGURE 20. Safe operating area for switching between saturation and cutoff (clamped inductive load).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

* 6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

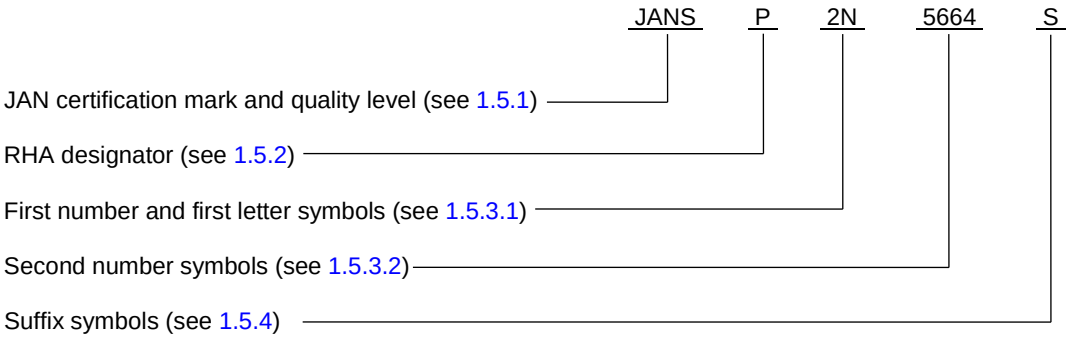
* d. The complete Part or Identifying Number (PIN), see 1.5 and 6.4.

e. For acquisition of RHA designated devices, table III, subgroup 1 testing of group D is optional. If subgroup 1 testing is desired, it must be specified in the contract.

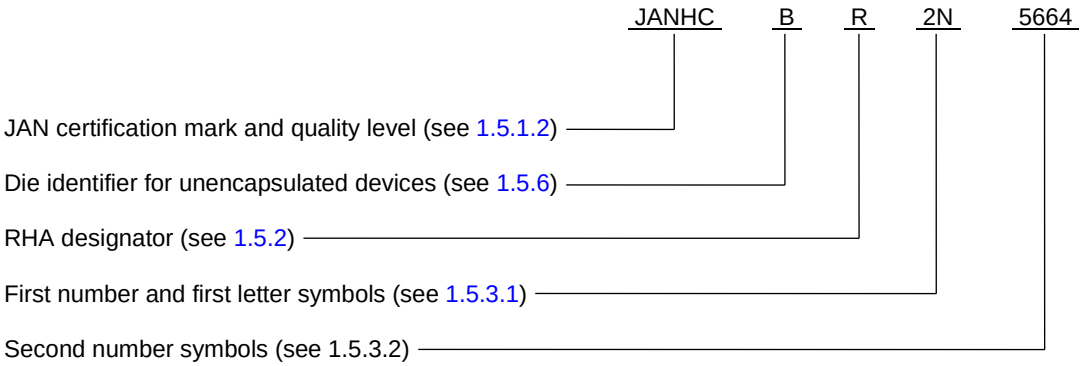
6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil .

6.4 PIN construction example.

6.4.1 Encapsulated devices. The PINs for encapsulated devices are constructed using the following form.



6.4.2 Un-encapsulated devices. The PINs for un-encapsulated devices are constructed using the following form.



* 6.5 Suppliers of JANHC and JANKC die. The qualified JANHC and JANKC suppliers with the applicable letter version (example JANHCA2N5664) will be identified on the QML.

Die ordering information (1)		
PIN	Manufacturer	
	43611	34156
2N5664	JANHCA2N5664	JANHCB2N5664
2N5665	JANHCA2N5665	
2N5666	JANHCA2N5666	JANHCB2N5666
2N5667	JANHCA2N5667	

(1) For JANKC level, replace JANHC with JANKC.

6.6 List of PINs.

6.6.1 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices in a TO-66 package (1)		PINs for devices in a TO-5 package (standard lead lengths) (1)		PINs for devices in a TO-39 package (short lead lengths) (1)	
JAN2N5664	JAN2N5665	JAN2N5666	JAN2N5667	JAN2N5666S	JAN2N5667S
JANTX2N5664	JANTX2N5665	JANTX2N5666	JANTX2N5667	JANTX2N5666S	JANTX2N5667S
JANTXV2N5664	JANTXV2N5665	JANTXV2N5666	JANTXV2N5667	JANTXV2N5666S	JANTXV2N5667S
JANTXVR2N5664	JANTXVR2N5665	JANTXVR2N5666	JANTXVR2N5667	JANTXVR2N5666S	JANTXVR2N5667S
JANTXVF2N5664	JANTXVF2N5665	JANTXVF2N5666	JANTXVF2N5667	JANTXVF2N5666S	JANTXVF2N5667S
JANS2N5664	JANS2N5665	JANS2N5666	JANS2N5667	JANS2N5666S	JANS2N5667S
JANS#2N5664	JANS#2N5665	JANS#2N5666	JANS#2N5667	JANS#2N5666S	JANS#2N5667S

PINs for devices in a U3 package (1)	
JAN2N5666U3	JANTXVR2N5666U3
JANTX2N5666U3	JANTXVF2N5666U3
JANTXV2N5666U3	JANS#2N5666U3
JANS2N5666U3	

(1) The number sign (#) represents one of eight RHA designators available (M, D, P, L, R, F, G, or H).

6.6.2 PINs for unencapsulated devices (die). The following is a list of possible PINs for unencapsulated devices available on this specification sheet.

Quality level HC	Quality level HC w/ RHA	Quality level KC	Quality level KC w/ RHA
JANHCA2N5664	JANHCA#2N5664	JANKCA2N5664	JANKCA#2N5664
JANHCA2N5665	JANHCA#2N5665	JANKCA2N5665	JANKCA#2N5665
JANHCA2N5666	JANHCA#2N5666	JANKCA2N5666	JANKCA#2N5666
JANHCA2N5667	JANHCA#2N5667	JANKCA2N5667	JANKCA#2N5667
JANHCB2N5664	JANHCB#2N5664	JANKCB2N5664	JANKCB#2N5664
JANHCB2N5666	JANHCB#2N5666	JANKCB2N5666	JANKCB#2N5666

(1) The number sign (#) represents one of eight RHA designators available for the KC quality level (M, D, P, L, R, F, G, or H), and one of two RHA designators available for the HC quality level (R or F).

* 6.7 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@.dla.mil or by facsimile (614) 693-1642 or DSN 850-6939.

* 6.8 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

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