DELKIN DEVICES®

SLC Industrial microSD Memory Card

Engineering Specification

Document Number: L500707

Revision: A

Overview

- **Capacity**
  - SLC 512MB up to 16GB
- **Bus Speed Mode**
  - 512MB – 2GB: Non-UHS
  - 4GB – 16GB: UHS-I
- **Power Consumption**
  - Idle Current <1.05mA
  - Read Current <50mA
  - Write Current <60mA
- **Performance**
  - Read: Up to 27 MB/s
  - Write: Up to 20 MB/s
- **Advanced Flash Management & Features**
  - Static and Global Wear Leveling
  - Bad Block Management
  - SMART Monitoring
  - Near-miss ECC Refresh
  - SMART Functionality
  - Firmware Redundancy
  - Power Fail Robustness
  - AES Encryption Engine
- **Operating Temperature Range**
  - -40°C ~ 85°C
- **Storage Temperature Range**
  - -50°C ~ 100°C
- **RoHS compliant**

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1. INTRODUCTION

1.1. General Description

Delkin Devices' latest generation of SLC industrial microSD cards deliver the endurance of SLC, full industrial operating temperature range and total compliance with SD Association Part 1 Physical Layer Specification Version 3.01 standard. In addition to advanced flash management features, the integrated robust industrial controller manages sudden power interruptions, provides SMART functionality and offers AES encryption.

microSD cards are the fastest growing form factor in the industrial storage market, due to their small size, robust mechanical design and low power consumption. Delkin has been a leader in this market for years and continues to innovate, providing our customers with new tools to ensure reliable performance.

1.2. Flash Management & Key Features

1.2.1. Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, the controller in Delkin's SLC industrial microSD cards applies an advanced BCH ECC algorithm, which can detect and correct errors occur during read processes, ensuring data been read correctly, as well as protecting data from corruption. The Delkin SLC Industrial microSD's also employ "near-miss" ECC, such that all blocks which reach a certain error threshold are automatically refreshed immediately upon detection. The threshold is determined by the specific flash and ECC configuration in the card.

1.2.2. Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some blocks are updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling techniques are applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

The controller in Delkin's newest SLC industrial microSD cards utilizes an advanced Wear Leveling algorithm, which optimizes life and performance, through a combination of static and global wear leveling. Static wear leveling is utilized until one flash reaches 90% of the rated P/E cycles, which is more efficient from a performance standpoint. Once a flash reaches 90%, wear leveling switches to a global scheme, and all flash blocks participate in wear leveling as one large pool, which enables the card to maximize lifetime.

1.2.3. Bad Block Management

Bad blocks are blocks that include one or more invalid bits and therefore, their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as "Initial Bad Blocks". Blocks that develop invalid bits during the lifespan of the flash are named "Later Bad Blocks". The controller in Delkin's Industrial SLC microSD cards implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manage any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves data reliability.

1.2.4. Smart Function

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is a special function that allows a memory device to automatically monitor its health. While there is not an industry standard for SD/microSD card SMART functionality, as there is for SATA & PATA devices, Delkin can provide either an off-line program or commands that can be issued via the host to collect data from the card. Refer to Section 7 for the direct command details and the information that can be extracted from the card.

1.2.5. Read Disturb Management

Delkin's SLC Industrial microSD's have advanced Read Disturb Management to prevent uncorrectable errors in heavy read applications. As flash geometries shrink, the likelihood of disturbances when adjacent pages are frequently read is increased, and typically wear leveling is triggered by writing and erasing. However, the advanced read disturb management system actually counts all reads on a block level, and compares them to a configurable threshold. Once the threshold has been reached, a read wear level is triggered and the block is refreshed, sending it to the back of the line. This ensures that errors will not accumulate to the point that they will be uncorrectable.

1.2.6. Firmware Redundancy

Since microSD cards are often used in applications with unstable sources of power, protecting the firmware is critical. Delkin's SLC industrial microSD cards maintain two copies of firmware within the flash, so that if the primary copy of the firmware is damaged, the back-up copy can be used, the back-up copy is used, and then the original copy is repaired.

1.2.7. Dynamic Data Refresh

Typically, when a drive is new and less than 10% of the program/erase cycles have been consumed, the data retention time of the flash is 5 or 10 years, depending on the type of flash. At end of life, however, when 100% of the program/erase cycles have been consumed, typically, the retention time is 1 year. To extend long term data retention over the life of a card, Delkin's SLC Industrial microSD will automatically refresh data that is not accessed for a long time, which can be triggered based on a configurable power-on count threshold and operate in the background.

1.2.8. Power Fail Robustness

With the goal of preventing data corruption and card failure, Delkin's SLC Industrial microSD's have been developed to survive unscheduled power interruptions with minimal effect. In the event of a power loss, the controller will reset and flash is immediately write-protected. A log is kept of recent flash transactions, and if the last data in the log is corrupt, then the controller will recover the latest valid entry. If a write operation was in process at the time of the power loss, but not committed to flash, or the tables had not yet been updated, then this data might be lost. Since the original data is always kept in a "twin" of the active block, we can always revert back to the last known valid state of the card.

2. PRODUCT SPECIFICATIONS

- **Capacity**
  - SLC: 512MB ~ 16GB
- **Operation Temp. Range**
  - -40 ~ +85°C
- **Storage Temp. Range**
  - -50 ~ +100°C
- **Support SD system specification version 3.0**
- **Card capacity of non-secure area and secure area support [Part 3 Security Specification Ver3.0 Final] Specifications**
- **Support SD & SPI mode**
- **Designed for read-only and read/write cards**
- **Bus Speed Mode (using 4 parallel data lines)**
  - **Non-UHS mode**
    - Default Speed mode: 3.3V signaling, Frequency up to 25 MHz, up to 12.5 MB/sec
    - High Speed mode: 3.3V signaling, Frequency up to 50 MHz, up to 25 MB/sec

    Note: SDSC card (capacity ≤ 2GB) only supports non-UHS mode.
  - **UHS-I mode**
    - SDR12 - SDR up to 25MHz 1.8V signaling, up to 12.5MB/sec
    - SDR25 - SDR up to 50MHz 1.8V signaling, up to 25MB/sec
    - SDR50: 1.8V signaling, Frequency up to 100 MHz, up to 50MB/sec
    - SDR104: 1.8V signaling, Frequency up to 208MHz, up to 104MB/sec
    - DDR50: 1.8V signaling, Frequency up to 50 MHz, sampled on both clock edges, up to 50MB/sec

    Notes: Timing in 1.8V signaling is different from that of 3.3V signaling.
- **The command list supports [Part 1 Physical Layer Specification Ver3.1 Final] definitions**
- **Card removal during read operation will never harm the content**
- **Password Protection of cards (optional)**
- **Write Protect feature using mechanical switch on SD adapter**
- **Built-in write protection features (permanent and temporary)**
- **AES encryption engine supporting 128 & 256 bit, ECB, CBC and XTS modes supported, for high performance on-the-fly encryption/decryption**
- **+4KV/-4KV ESD protection in contact pads**
- **Operation voltage range: 2.7 ~ 3.6V**

2.1. Part Numbers and Performance

Capacity	Temperature Range	Part Number	Sequential	
			Read (MB/s)	Write (MB/s)
512MB	-40 to +85°C	S351MMUU8-C1000-4	23.5 MB/s	18.3 MB/s
1GB	-40 to +85°C	S30GMMUU8-C1000-4	23.5 MB/s	18.1 MB/s
2GB	-40 to +85°C	S302MMZU8-C1000-4	23.3 MB/s	20.3 MB/s
4GB	-40 to +85°C	S304MMZU8-U1000-4	23.8 MB/s	20.3 MB/s
8GB	-40 to +85°C	S308MMZU8-U1000-4	27.4 MB/s	19.6 MB/s
16GB	-40 to +85°C	S316MMZU8-U1000-4	27.1 MB/s	17.5 MB/s

NOTES:

1. Performance benchmarks measured with CrystalDiskMark.
2. Actual performance in host system may vary depending on computer configuration, application, workload, etc.
3. All capacities below 4GB are non-UHS enabled.
4. 4GB – 16GB are UHS-I enabled. Not compatible with UHS-II hosts or card readers.
5. SD adapters are not included and are sold separately.
   Reference Part # PAK CAS MICROSD ADAPTER BV1

3. ENVIRONMENTAL SPECIFICATIONS

3.1. Environmental Conditions

Parameter	Conditions / Specifications
Temperature Operating Storage	 -40 to 85°C -50 to 100°C
Moisture & Corrosion Relative Humidity – Operating Relative Humidity – Storage Salt Spray	 25°C / 95% Relative Humidity 40°C / 93% Relative Humidity/500h 3% NaCl / 35°C; 24 hours, according to MIL-STD Method 1009
Shock & Vibration Shock Vibration	 1500G, 0.5msec duration 20 – 80Hz / 1.52mm displacement, 80Hz – 2000Hz, 20G acceleration, X, Y & Z axes; 30 min each
Bending, Torque, Drop Bending Torque Drop	 10N 0.15Nm, ± 25°C Max 1.5M free fall
Durability	10,000 mating cycles
Electro Static Discharge (ESD)	Human Body Model: ± 4KV 100pF / 1.5KΩ Machine Model: ± 0.25 KV 200pF / 0Ω Contact Pads: 4 KV , Non-Contact Pad Area: ± 8 KV (coupling plane discharge) ± 15 KV (air discharge) Testing in accordance with IEC 61000-4-2

4. MECHANICAL SPECIFICATIONS

4.1. microSD Memory Card Package – Dimensions

Item	Value
Dimensions	
Length	15mm ± 0.1mm
Width	11mm ± 0.1mm
Thickness	0.95mm Max
Interconnect Area	0.7mm ± 0.1mm
Pull Area	1.0mm ± 0.1mm
	Testing in accordance with MIL STD 883, Method 2016

4.2. External Signal Contacts

Item	Value
Number of ESC	8 Minimum
Distance from Front Edge	1.1 mm
ESC Grid	1.1mm
Contact Dimensions	0.8mm x 2.9mm
Electrical Resistance	30mΩ (Worst case: 100mΩ)
Contact Plating	
Nickel base	5.0µm (196.8 microinches) minimum
Gold	0.8µm (31.5 microinches) minimum

5. ELECTRICAL SPECIFICATIONS

5.1. Power Consumption

The table below shows the power consumption of Delkin's microSD cards by configuration.

Table 5-1 Power Consumption

Flash Mode	Idle Current (mA)	Max. Read Current (mA)	Max. Write Current (mA)
512MB	1.00	40	45
1GB	0.75	40	45
2GB	0.75	40	55
4GB	0.75	40	55
8GB	0.75	40	55
16GB	1.05	45	60

5.2. Electrical Specifications

Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit
1	V_{DD}-V_{SS}	DC Power Supply	-0.3	+3.3	V
2	V_{IN}	Input Voltage	V_{SS}-0.3	V_{DD}+0.3	V
4	Ta	Operating Temperature (Diamond)	-40	+85	°C
5	Tst	Storage Temperature	-50	+100	°C
6	V_{DD}	V_{DD} Voltage	2.7	3.6	V

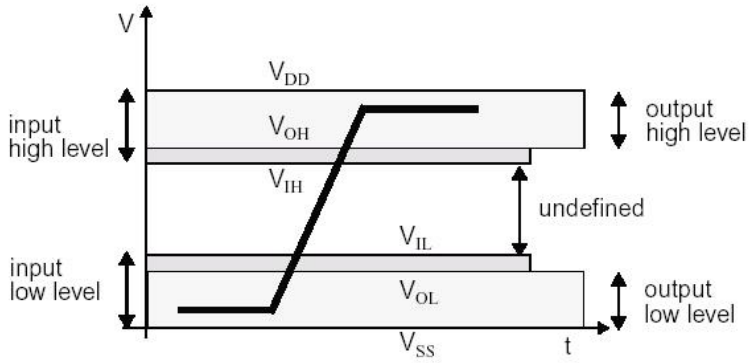
5.3. DC Characteristic

5.3.1. Bus Operation Conditions for 3.3V Signaling

Table 5-2 Threshold Level for High Voltage Range

Parameter	Symbol	Min	Max	Unit	Remarks
Supply voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	VOH	0.75*VDD		V	IOH=-100uA V_{DD}Min.
Output Low Voltage	VOL		0.125*VDD	V	IOL = 100uA VDD min
Input High Voltage	VIH	0.625*VDD	VDD+0.3	V	
Input Low Voltage	VIL	VSS-0.3	0.25 *VDD	V	
Power up time			250	ms	from 0v to VDD min.

Bus Signal Levels



Bus signal levels

Table 5-3 Peak Voltage and Leakage Current

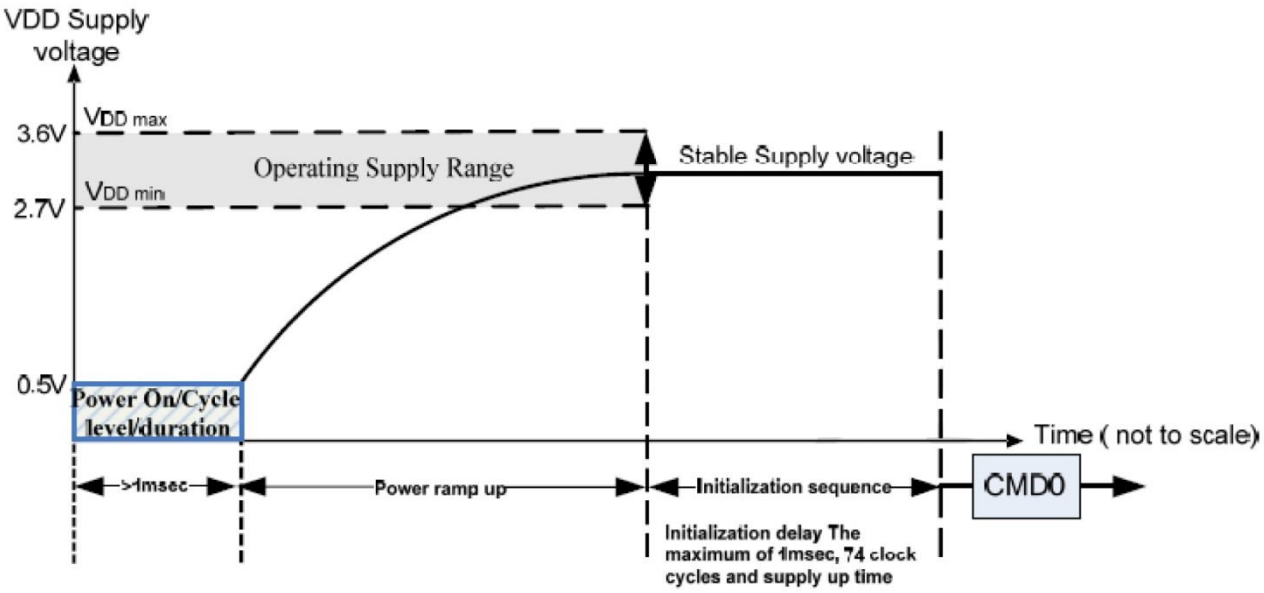
Parameter	Symbol	Min	Max.	Unit	Remarks
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

5.3.2. Bus Signal Line Levels

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card CHOST+CBUS shall not exceed 30 pF
Capacitance of the card for each signal pin	CCARD		10	pF	
Maximum signal line inductance			16	nH	f_{pp}<20 MHz
Pull-up resistance inside card (pin1)	RDAT3	10	90	kΩ	May be used for card detection

5.3.3. Power Up Time

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.



Power On or Power Cycle

Followings are requirements for Power on and Power cycle to assure a reliable SD Card hard reset.

(1) Voltage level shall be below 0.5V

(2) Duration shall be at least 1ms.

Power Supply Ramp Up

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD (min.) and VDD (max.) and host can supply SDCLK.

The followings are recommendations for Power ramp up:

(1) Voltage of power ramp up should be monotonic as much as possible.

(2) The minimum ramp up time should be 0.1ms.

(3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.

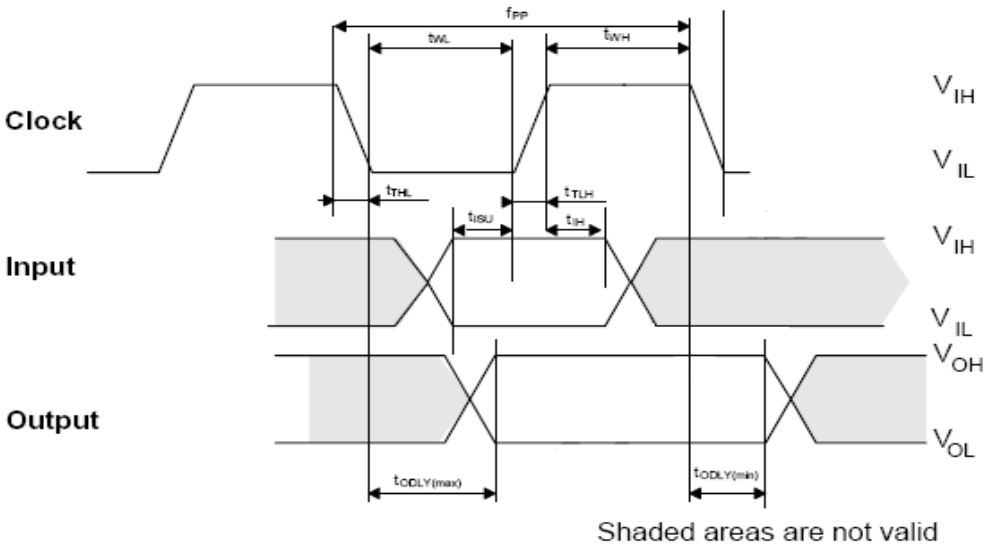
Power Down and Power Cycle

• When the host shuts down the power, the card VDD shall be reduced to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.

• If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in *Inactive State.* To create a power cycle, the host shall follow the power down description before power up the card (i.e. the card VDD shall be once reduced to less than 0.5Volt for a minimum period of 1ms).

5.4. AC Characteristic

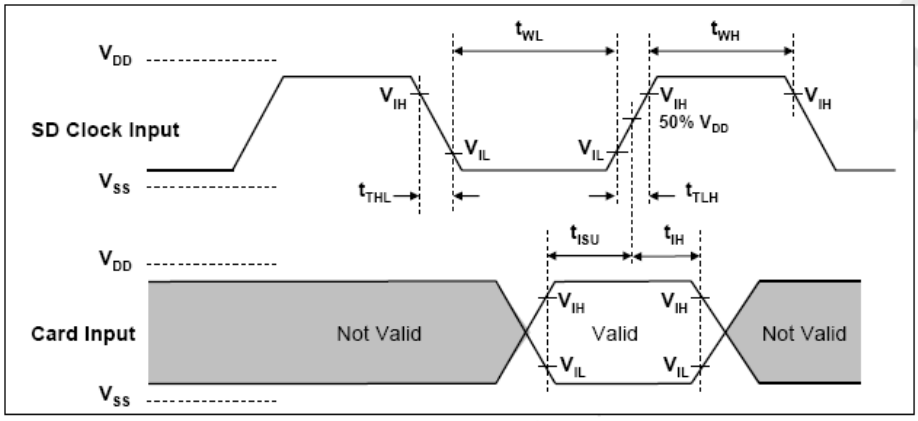
5.4.1. microSD Interface timing (Default)



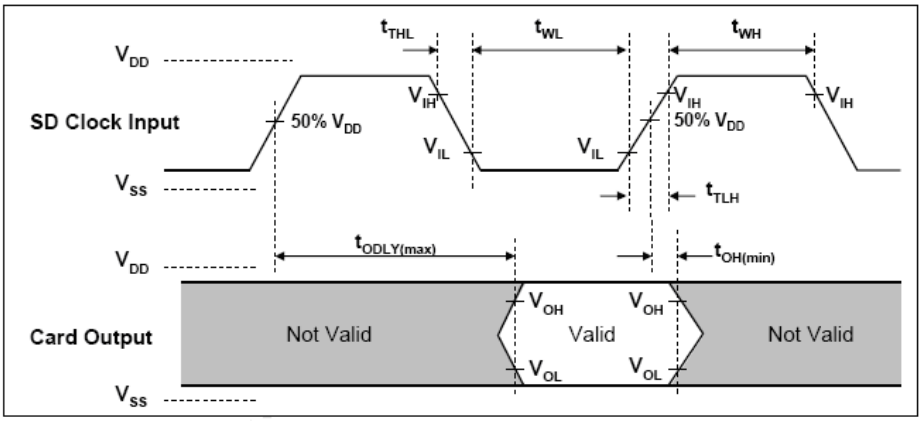
Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{card}≤□10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	$0_{(1)}$/100	400	kHz	C_{card}≤□10 pF (1 card)
Clock low time	t_{WL}	10		ns	C_{card}≤□10 pF (1 card)
Clock high time	t_{WH}	10		ns	C_{card}≤□10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{card}≤□10 pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{card}≤□10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{card}≤□10 pF (1 card)
Input hold time	t_{IH}	5		ns	C_{card}≤□10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L≤40 pF (1 card)
Output Delay time during Identification Mode	tODLY	0	50	ns	C_L≤40 pF (1 card)

(1) 0Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

5.4.2. microSD Interface Timing (High-Speed Mode)



Card Input Timing (High Speed Card)



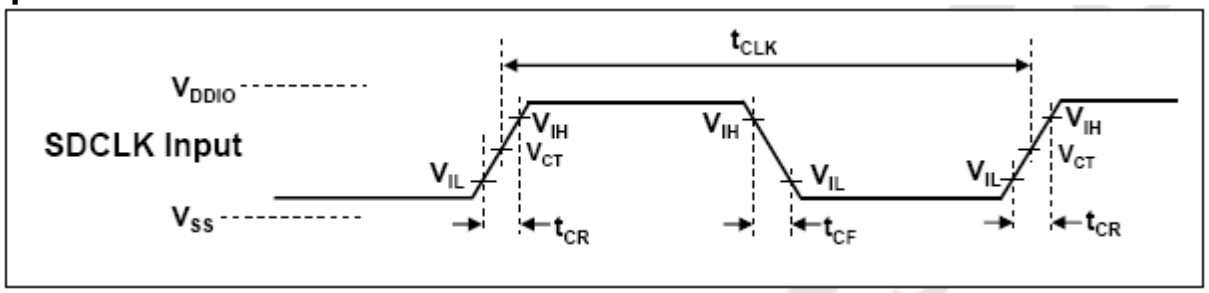
Card Output Timing (High Speed Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{card} ≤ 10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{card} ≤ 10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{card} ≤ 10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{card} ≤ 10 pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{card} ≤ 10 pF (1 card)
Input hold time	t_{IH}	2		ns	C_{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	C_L ≤ 40 pF (1 card)
Output Hold time	T_{OH}	2.5		ns	C_L ≤ 15 pF (1 card)
Total System capacitance of each line[1]	C_L		40	pF	CL ≤ 15 pF (1 card)

(1) In order to satisfy severe timing, the host shall drive only one card.

5.4.3. microSD Interface timing (SDR12, SDR25, SDR50 & SDR104 Modes)

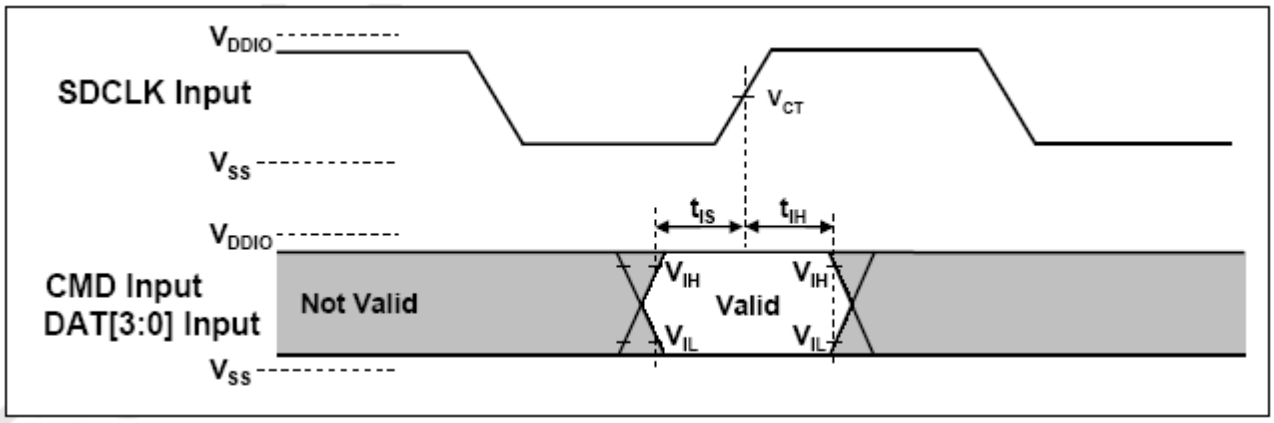
Input:



Symbol	Min	Max	Unit	Remark
tCLK	4.80	-	ns	208MHz (Max.), Between rising edge, VCT= 0.975V
tCR, tCF	-	0.2* tCLK	ns	tCR, tCF < 2.00ns (max.) at 100MHz, CCARD=10pF
Clock Duty	30	70	%	

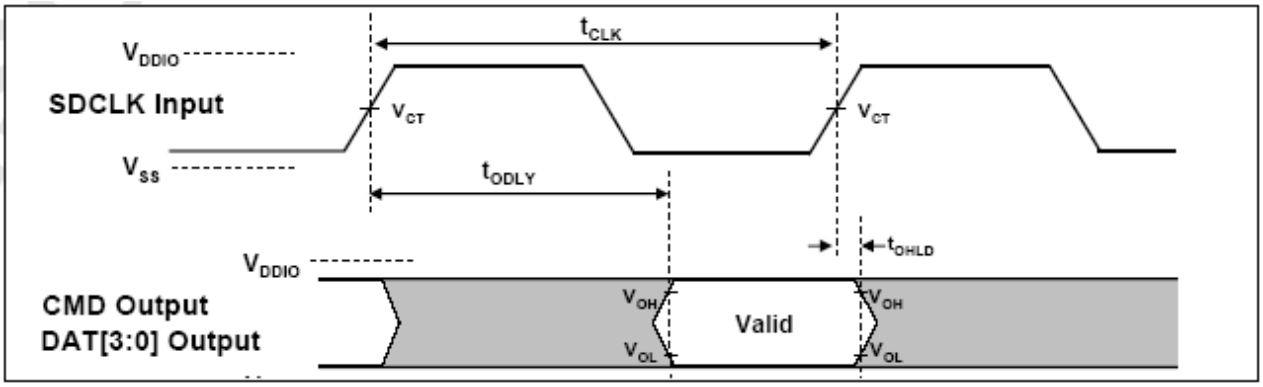
Clock Signal Timing

SDR50 and SDR104 Input Timing:



Symbol	Min	Max	Unit	SDR104 Mode
tIs	1.40	-	ns	CCARD =10pF, VCT= 0.975V
tIH	0.80	-	ns	CCARD =5pF, VCT= 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR50 Mode**
tIs	3.00	-	ns	CCARD =10pF, VCT= 0.975V
tIH	0.80	-	ns	CCARD =5pF, VCT= 0.975V

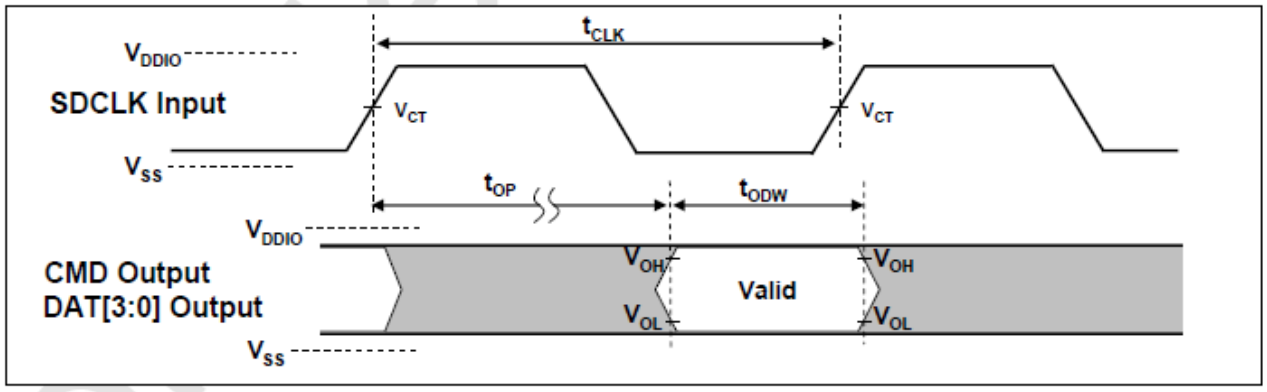
Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50):



Symbol	Min	Max	Unit	Remark
tODLY	-	7.5	ns	tCLK>=10.0ns, CL=30pF, using driver Type B, for SDR50
tODLY	-	14	ns	tCLK>=20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12,
TOH	1.5	-	ns	Hold time at the tODLY (min.), CL=15pF

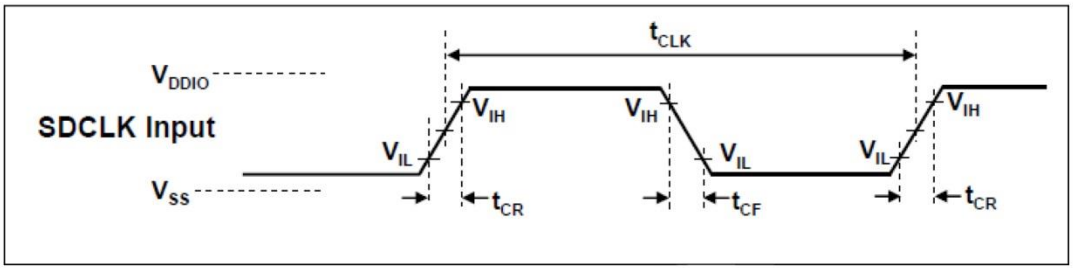
Output Timing of Fixed Data Window

Output Timing of Variable Window (SDR104):



Symbol	Min	Max	Unit	Remark
tOP	0	2	UI	Card Output Phase
ΔtOP	-350	+1550	ps	Delay variable due to temperature change after tuning
tODW	0.60	-	UI	tODW=2.88ns at 208MHz

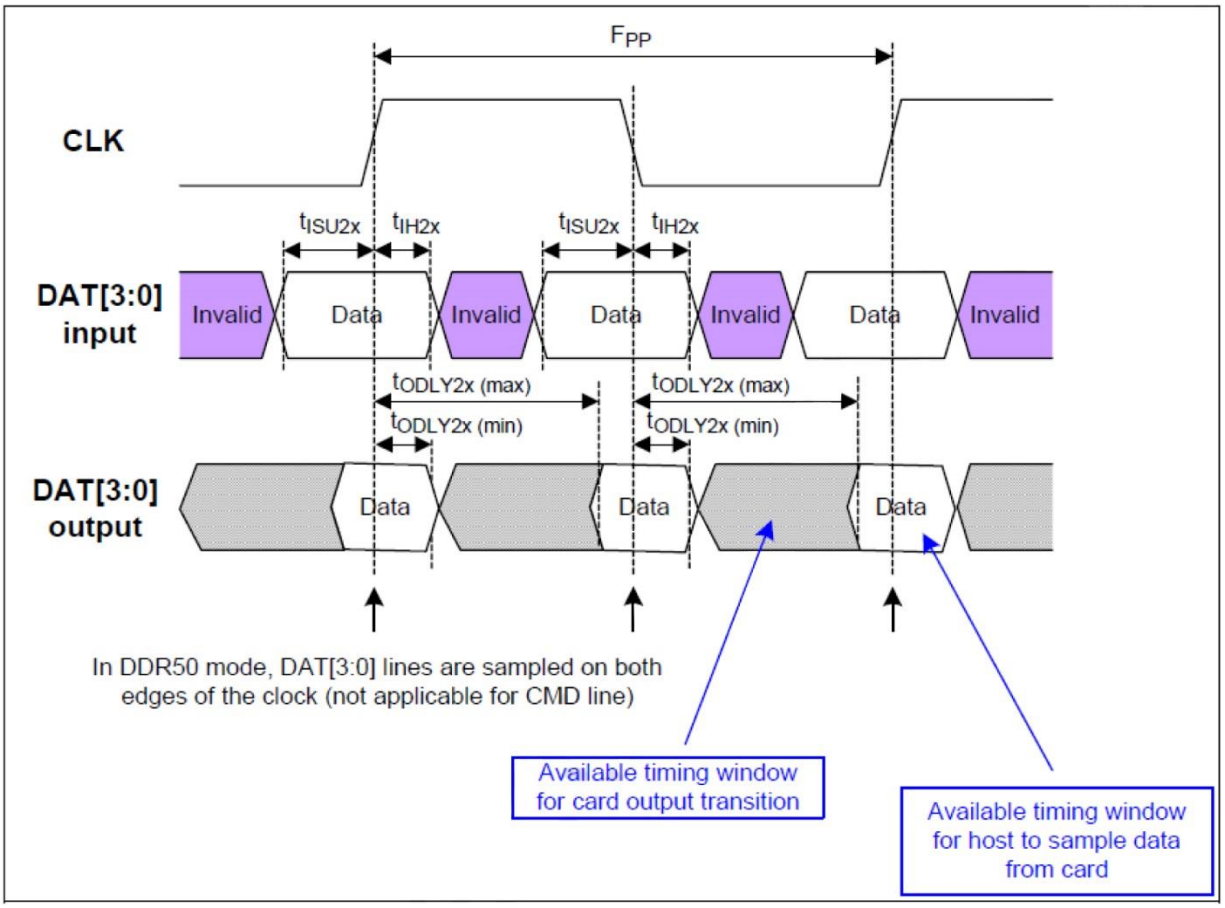
5.4.4. microSD Interface timing (DDR50 Modes)



Clock Signal Timing

Symbol	Min	Max	Unit	Remark
tCLK	20	-	ns	50MHz (Max.), Between rising edge
tCR, tCF	-	0.2* tCLK	ns	tCR, tCF < 4.00ns (max.) at 50MHz, CCARD=10pF
Clock Duty	45	55	%	

Clock Signal Timing



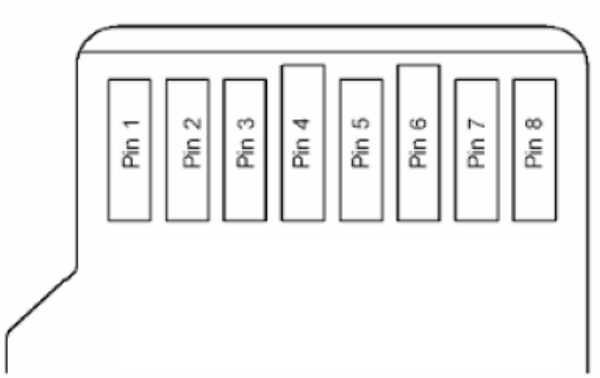
Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	6	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	C_L≤30 pF (1 card)
Output Hold time	T_{OH}	1.5	-	ns	C_L≥15 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	C_L≤25 pF (1 card)
Output Hold time	T_{OH2x}	1.5	-	ns	C_L≥15 pF (1 card)

Bus Timings – Parameters Values (DDR50 mode)

6. INTERFACE

6.1. Pad Assignment and Descriptions



pin	SD Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type	Description
1	DAT2	I/O/PP	Data Line[bit2]	RSV		
2	CD/DAT3[2]	I/O/PP[3]	Card Detect/ Data Line[bit3]	CS	I[3]	Chip Select (neg true)
3	CMD	PP	Command/Response	DI	I	Data In
4	V_{DD}	S	Supply voltage	V_{DD}	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS}	S	Supply voltage ground	V_{SS}	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line[bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line[bit1]	RSV		

(1) S: power supply, I: input; O: output using push-pull drivers; PP:I/O using push-pull drivers

(2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMedia Cards.

(3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions - Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer period, with SET_CLR_CARD_DETECT (ACMD42) command.

7. SMART

7.1. Direct Host Access to SMART Data via SD General Command (CMD56)

In order to directly access Delkin SLC Industrial microSD SMART data through host commands, including details about the card status and life, follow the protocol below:

SD Command number:	56
Command argument:	CS=3, CC=0, R/W=1
Input:	N/A
Returns:	One 512 Byte sector
Description:	Execution delivers information about the life and status of the card.

The data layout is as follows:

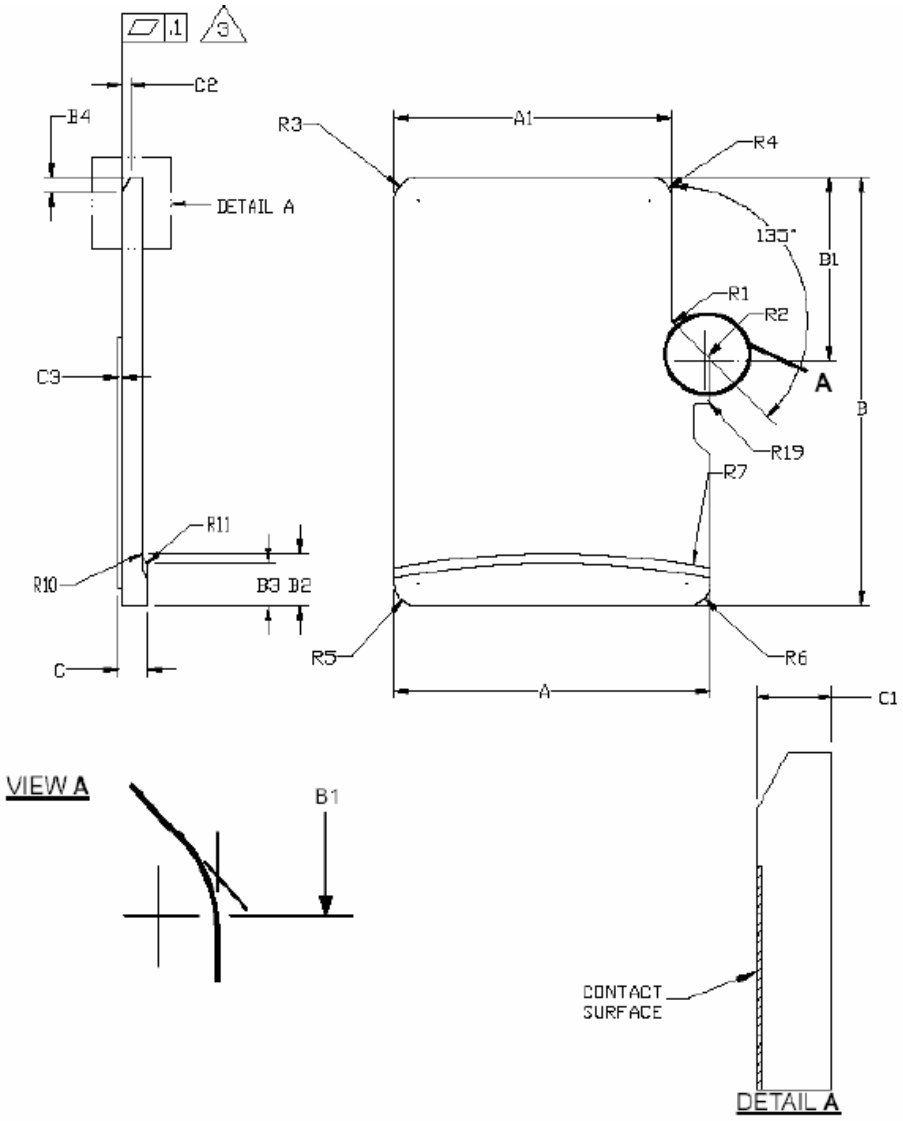
Offset	Description
0	Extended Card Life Time Information data structure version (currently 1)
1	Read disturb management enable status (0: off; 1: on)
2	Global wear level status (0: local wear leveling; 1: global wear leveling)
3	Global remap status (0: local remap; 1: global remap)
4…7	Host transfer CRC errors
8…15	Total LBAs read
16…23	Total LBAs written
24	ECC correction capability (correctable number of bit errors per 1KB unit)
25	Data structure version identifier, currently 1
26…27	Number of manufacturer marked defect blocks
28…29	Number of initial spare blocks (worst flash chip)
30…31	Number of initial spare blocks (sum over all flash chips)
32	Percentage of remaining spare blocks (worst flash chip)
33	Percentage of remaining spare blocks (sum over all flash chips)
34…35	Number of uncorrectable ECC errors (not including startup ECC errors)
36…39	Number of correctable ECC errors (not including startup ECC errors)
40…41	Lowest wear level class
42…43	Highest wear level class
44…45	Wear level threshold
46…51	Total number of block erases
52…53	Number of flash blocks, in units of 256 blocks
54…55	Maximum flash block erase count target, in wear level class units
56…59	Power on count
60…63	Firmware version
64…71	Total number of reads
72…75	Number of uncorrectable ECC errors during startup
76…79	Number of correctable ECC errors during startup
80…83	Minimum block erase count
84…87	Maximum block erase count
88…91	Anchor block write count
92…95	Initial read disturb threshold
96…99	Current read disturb threshold
100…103	RDM Block refresh count (number of block refreshes triggered by read disturb management)
104…111	Extended number of correctable ECC errors (not including startup)
112…115	Warm reboot count
116…119	Commit count
120…123	Flush count
124…127	Firmware update count
128…131	Total number of read retries (not including startup)
132…135	Total number of read retries during startup
136…511	----

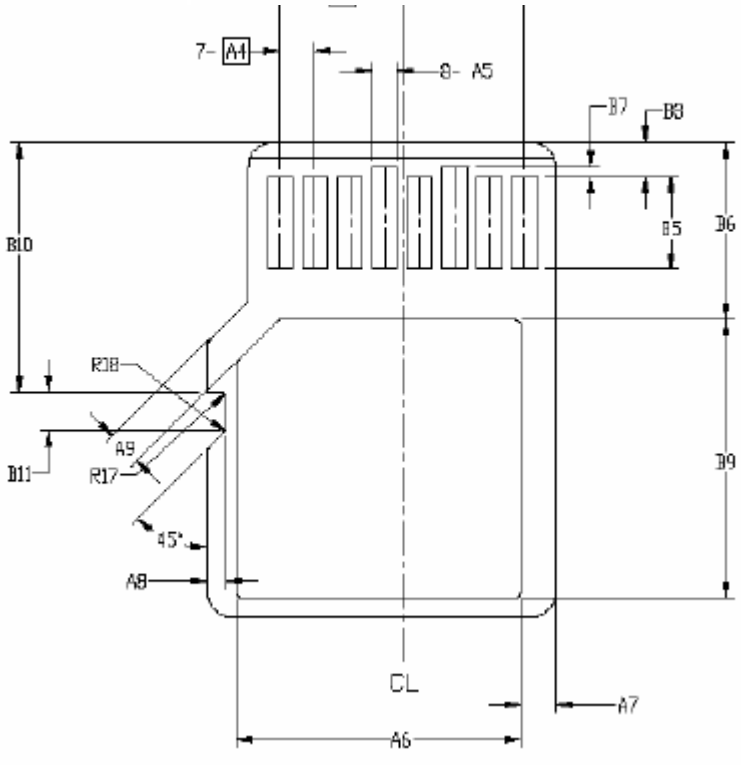
7.2. Access to SMART Data via CMD56 Emulation

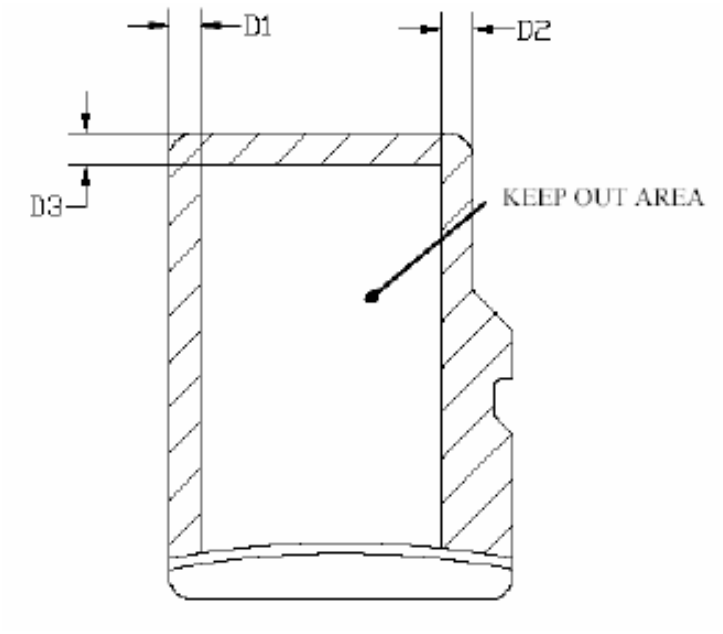
If unable to directly pass CMD56 from the host to the card, for

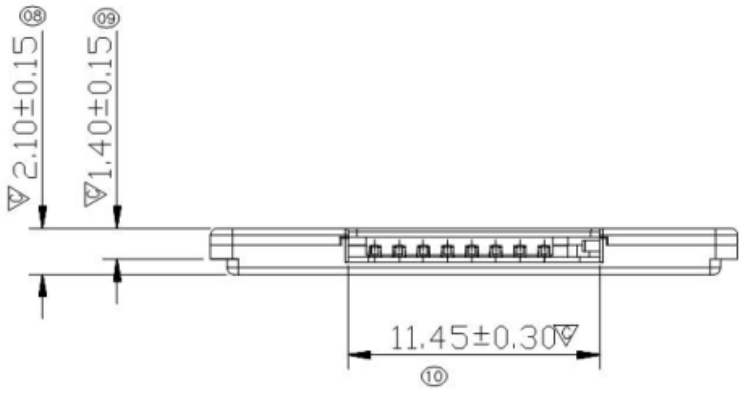
example, to access through a USB card reader, a CMD56 Emulation process is necessary. Contact Delkin for instructions.

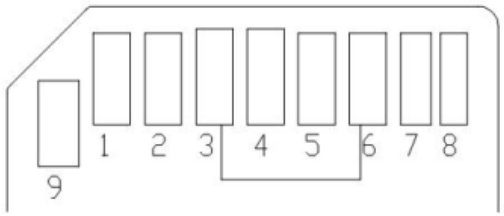
8. PHYSICAL DIMENSIONS


.1
3
C2
B4
DETAIL A
R3
A1
R4
135°
B1
R1
R2
A
B
C3
R19
R7
R11
R10
B3 B2
C
R5
R6
A
C1
VIEW A
B1
CONTACT
SURFACE
DETAIL A

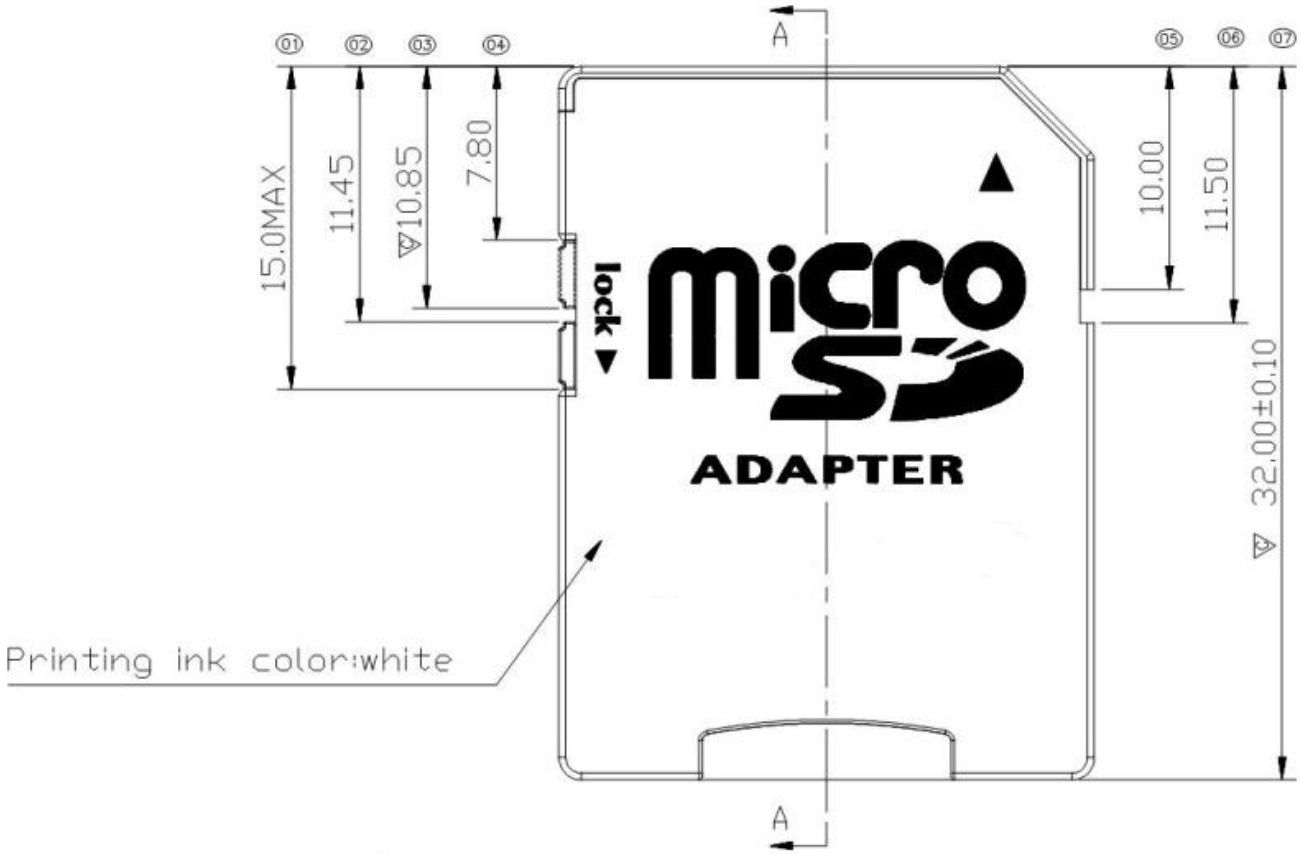

7- A4
8- A5
B7
B3
B10
B5
B6
R18
A9
B11
R17
B9
45°
A8
CL
A7
A6

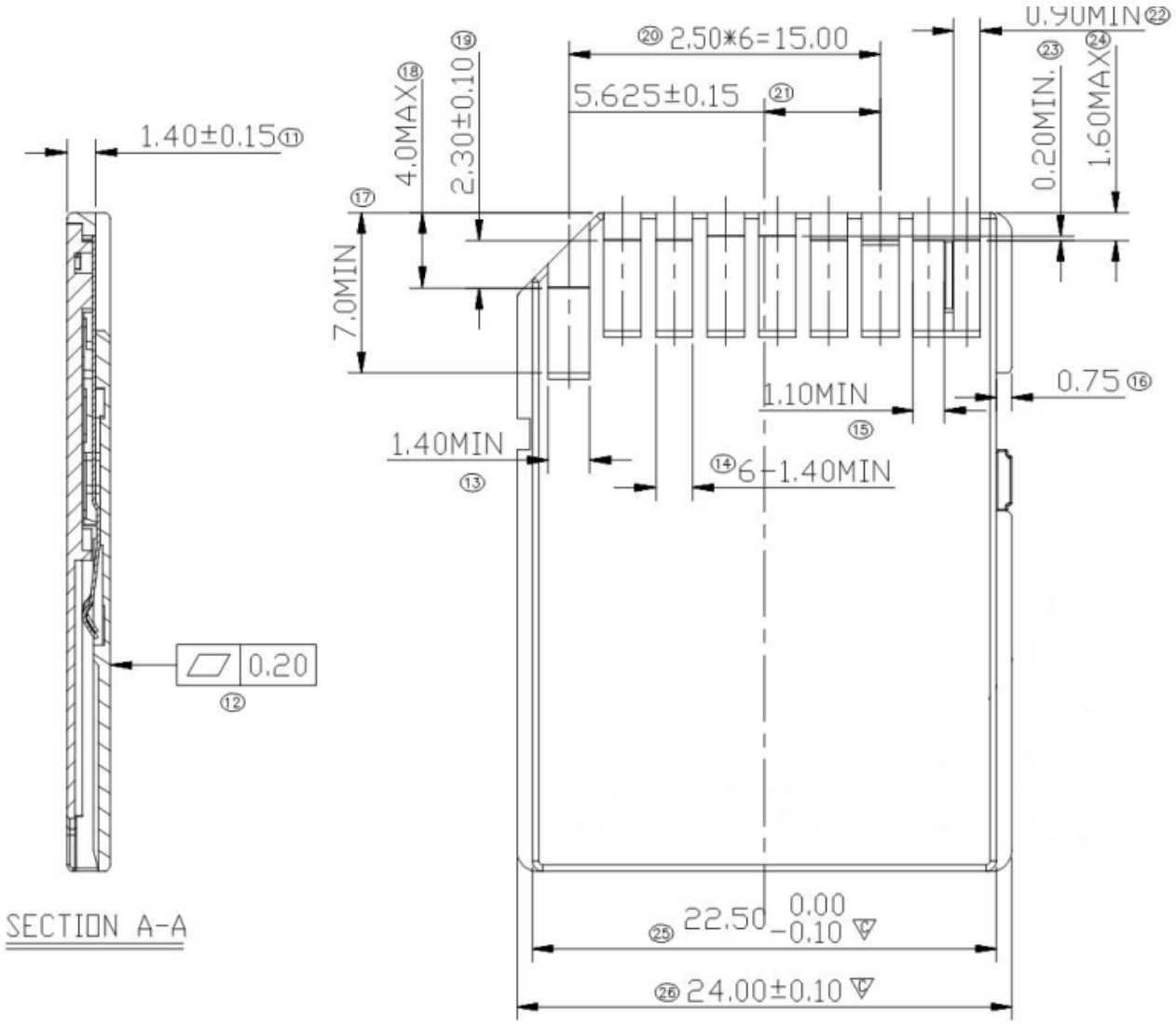






PIN 3 MUST BE CONNECTED TO PIN 6


01
02
03
04
05
06
07
A
15.0MAX
11.45
10.85
7.80
10.00
11.50
32.00±0.10
lock
ADAPTER
Printing ink color:white
A


1.40±0.15 11
0.20
12
SECTION A-A
19
4.0MAX 18
2.30±0.10
17
7.0MIN
20 2.50*6=15.00
5.625±0.15 21
0.90MIN 22
23
0.20MIN.
24
1.60MAX
1.10MIN 15
0.75 16
1.40MIN 13
14 6-1.40MIN
25 22.50 0.00 -0.10
26 24.00±0.10

SYMBOL	COMMON DIMENSIONS[1]			NOTE
	MIN[2]	NOM[2]	MAX[2]	
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
C	0.90	1.00	1.10	
C1	0.603	0.703	0.803	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.70	0.80	0.90	
R6	0.70	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	

Notes:

1. Dimensions are in millimeters
2. Dimensioning and tolerances are per ASME Y14.5M-1994.
3. Coplanarity is additive to C1 max thickness.