



60V 175°C DUAL N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BVDSS	R _{DS(ON)} max	I _D max T _C = +25°C
60V	$11m\Omega$ @ V _{GS} = $10V$	47.6A
607	$16m\Omega$ @ V _{GS} = 4.5V	39.5A

Description and Applications

This MOSFET is designed to meet the stringent requirements of automotive applications. It is qualified to AEC-Q101, supported by a PPAP and is ideal for use in:

- **Engine Management Systems**
- **Body Control Electronics**
- **DC-DC Converters**

Features and Benefits

- Rated to +175°C Ideal for High Ambient Temperature **Environments**
- 100% Unclamped Inductive Switching (UIS) Test in Production -Ensures More Reliable and Robust End Application
- High Conversion Efficiency
- Low Input Capacitance
- Fast Switching Speed
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- The DMTH6010LPDQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.

https://www.diodes.com/quality/product-definitions/

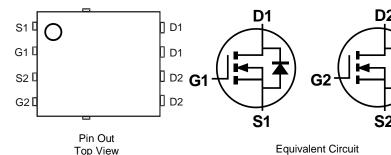
Mechanical Data

- Package: PowerDI®5060-8
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 @3
- Weight: 0.097 grams (Approximate)

Site1:



Top View **Bottom View**

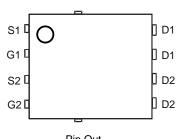


Site2:

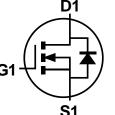
PowerDI5060-8/SWP (Type UXD)



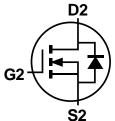
Top View **Bottom View**



Pin Out Top View



S1



Equivalent Circuit

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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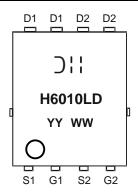
Ordering Information (Note 4)

Part Number	Packago	Packing		
Fait Number	Package	Qty.	Carrier	
DMTH6010LPDQ-13	PowerDI5060-8 (Type C)	2,500	Tape & Reel	
DMTH6010LPDQ-13	PowerDI5060-8/SWP (Type UXD)	2,500	Tape & Reel	

Notes:

4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



☐ = Manufacturer's Marking H6010LD = Product Type Marking Code YYWW or YYWW = Date Code Marking YY or YY = Year (ex: 21 = 2021) WW = Week (01 to 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V _{DSS}	60	V
Gate-Source Voltage			Vgss	±20	V
Continuous Drain Current (Note 6) $ T_C = +25^{\circ}C $ $T_C = +100^{\circ}C $			lo	47.6 33.7	А
Continuous Drain Current (Note 5)	Steady State	T _A = +25°C T _A = +70°C	lo	13.1 10.9	А
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I _{DM}	170	Α	
Maximum Continuous Body Diode Forward Current (Note 6)			Is	31	Α
Avalanche Current, L = 0.1mH			I _{AS}	20	Α
Avalanche Energy, L = 0.1mH			Eas	20	mJ

Thermal Characteristics

Characteristic	Symbol	Value	Unit	
Total Power Dissipation (Note 5)	$T_A = +25$ °C	PD	2.8	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	RөJA	53	°C/W
Total Power Dissipation (Note 6)	PD	37.5	W	
Thermal Resistance, Junction to Case (Note 6)	Rejc	4	°C/W	
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +175	°C	

5. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate. 6. Thermal resistance from junction to soldering point (on the exposed drain pad). Notes:



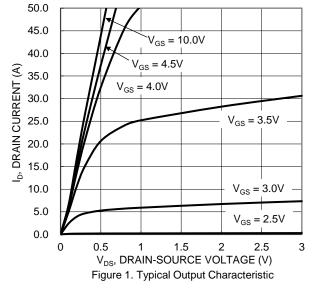
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BVDSS	60	_	_	V	$V_{GS} = 0V$, $I_D = 1mA$	
Zero Gate Voltage Drain Current	IDSS	_	_	1	μA	V _{DS} = 48V, V _{GS} = 0V	
Gate-Source Leakage	I _{GSS}	_	_	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	Vgs(th)	1	_	3	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	
Static Drain-Source On-Resistance	Descour	_	8.5	11	mΩ	VGS = 10V, ID = 20A	
Static Dialii-Source Off-Resistance	RDS(ON)	_	10.9	16		$V_{GS} = 4.5V, I_D = 20A$	
Diode Forward Voltage	VsD	_	0.9	1.2	V	V _G S = 0V, I _S = 20A	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	Ciss	_	2615	_	pF	.,	
Output Capacitance	Coss	_	1415	_	pF	V _{DS} = 30V, V _{GS} = 0V, f = 1MHz	
Reverse Transfer Capacitance	Crss	_	58	_	pF		
Gate Resistance	Rg	_	0.67	_	Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$	
Total Gate Charge (V _{GS} = 4.5V)	Qg	_	20.3	_	nC		
Total Gate Charge (V _{GS} = 10V)	Qg	_	40.2	_	nC	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	
Gate-Source Charge	Qgs	_	5.9	_	nC	$V_{DS} = 30V, I_{D} = 20A$	
Gate-Drain Charge	Qgd	_	9.3	_	nC		
Turn-On Delay Time	t _{D(ON)}	_	5.7	_	ns		
Turn-On Rise Time	t _R	_	8.8	_	ns	V _{DD} = 30V, V _{GS} = 10V,	
Turn-Off Delay Time	tD(OFF)	_	20.8	_	ns	$I_D = 20A$, $R_G = 3\Omega$	
Turn-Off Fall Time	tF	_	7.4	_	ns	1	
Body Diode Reverse Recovery Time	trr	_	34.5	_	ns	1 004 divis 4004/cc	
Body Diode Reverse Recovery Charge	Qrr	_	37.5	_	nC	I _F = 20A, di/dt = 100A/μs	

Notes:

^{7.} Short duration pulse test used to minimize self-heating effect. 8. Guaranteed by design. Not subject to product testing.





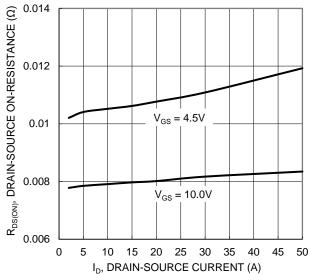


Figure 3. Typical On-Resistance vs. Drain Current

and Gate Voltage

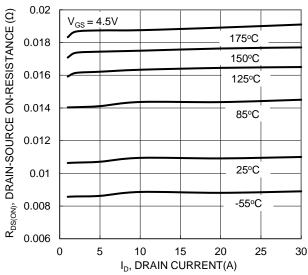


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

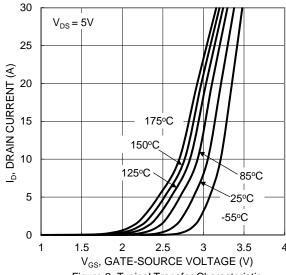


Figure 2. Typical Transfer Characteristic

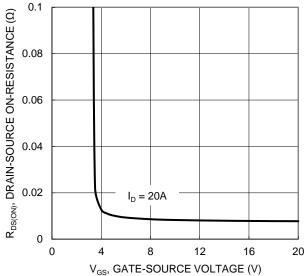


Figure 4. Typical Transfer Characteristic

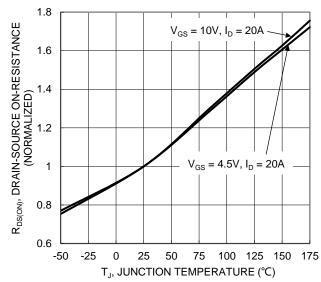


Figure 6. On-Resistance Variation with Junction Temperature



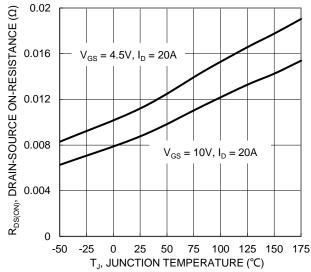


Figure 7. On-Resistance Variation with Junction Temperature

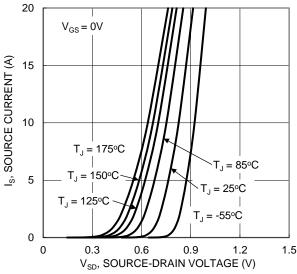


Figure 9. Diode Forward Voltage vs. Current

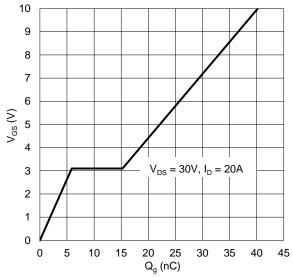


Figure 11. Gate Charge

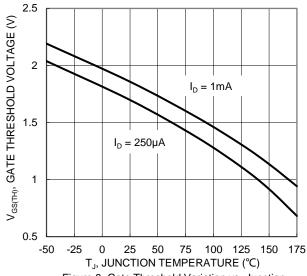
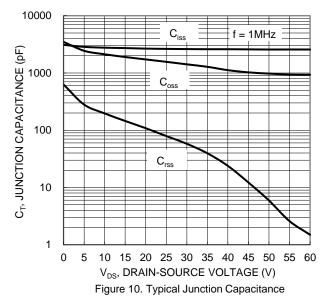


Figure 8. Gate Threshold Variation vs. Junction Temperature



100

R_{DS(ON)}

100

P_W = 1 μ s

P_W = 100 μ s

100

P_W = 100 μ s

100

P_W = 100 μ s

P_W = 100ms

P_W =



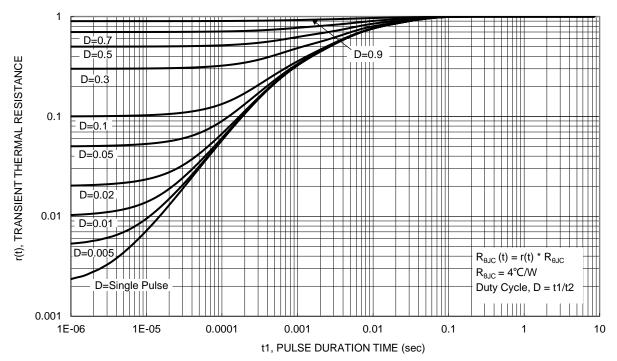


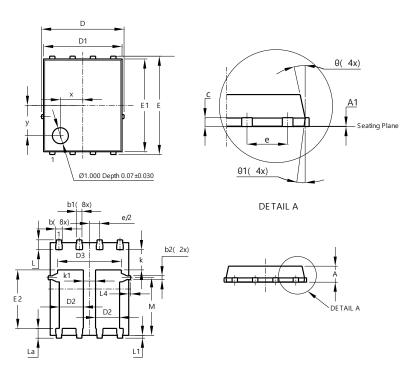
Figure 13. Transient Thermal Resistance



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version. **Site1:**

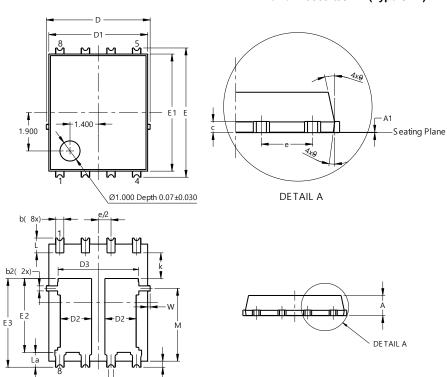
PowerDI5060-8 (Type C)



PowerDI5060-8 (Type C)				
Dim	Min	Max	Тур	
Α	0.90	1.10	1.00	
A 1	0	0.05	0.02	
b	0.33	0.51	0.41	
b1	0.300	0.366	0.333	
b2	0.20	0.35	0.25	
C	0.23	0.33	0.277	
D	;	5.15 BSC	;	
D1	4.85	4.95	4.90	
D2	1.40	1.60	1.50	
D3	1	1	3.98	
E	(6.15 BSC	;	
E1	5.75	5.85	5.80	
E2	3.56	3.76	3.66	
е		1.27BSC	;	
k	1	1	1.27	
k1	0.56	-	-	
L	0.51	0.71	0.61	
La	0.51	0.71	0.61	
L1	0.05	0.20	0.175	
L4	1	1	0.125	
М	3.50	3.71	3.605	
Х	-	-	1.400	
у	-	-	1.900	
θ	10°	12°	11°	
θ1	6°	8°	7°	
All Dimensions in mm				

Site2:

PowerDI5060-8/SWP (Type UXD)



Ро	PowerDI5060-8/SWP (Type UXD)				
Dim	Min	Max	Тур		
Α	0.90	1.10	1.00		
A1	0.00	0.05			
b	0.30	0.50	0.41		
b2	0.20	0.35	0.25		
b4).25REF			
С	0.230	0.330	0.277		
D	5	.15 BS(2		
D1	4.70	5.10	4.90		
D2	1.46	1.66	1.55		
D3	3.78	4.18	3.98		
Е	6	.40 BS	2		
E1	5.60	6.00	5.80		
E2	3.46	3.86	3.66		
E2a	4.195	4.595	4.395		
е	1	.27BS0)		
k	1.05				
L	0.635	0.835	0.735		
La	0.635	0.835	0.735		
L1	0.200	0.400	0.300		
М	3.205	4.005	3.605		
W	0.025	0.225	0.125		
θ	10°	12°	11°		
θ1	6°	8°	7°		
All Dimensions in mm					

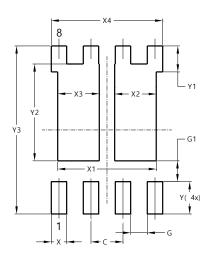


Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

Site1:

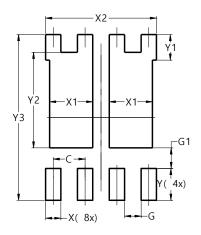
PowerDI5060-8 (Type C)



Dimensions	Value (in mm)
С	1.270
G	0.660
G1	0.820
Χ	0.610
X1	3.910
X2	1.650
Х3	1.650
X4	4.420
Υ	1.270
Y1	1.020
Y2	3.810
Y3	6.610

Site2:

PowerDI5060-8/SWP (Type UXD)



Dimensions	Value
Dilliensions	(in mm)
С	1.270
G	0.660
G1	0.820
Х	0.610
X1	1.720
X2	4.420
Υ	1.270
Y1	1.020
Y2	3.810
Y3	6.610



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