

Features

ReDriver™

- ➔ 10Gbps Serial Link with Linear Equalizer
- ➔ Full Compliancy to USB 3.1 Gen-2 and Gen-1 Super Speed Standard
- ➔ 1 to 2 DeMux from Host Tx to Device Rx
- ➔ 2 to 1 Mux from Device Tx to Host Rx
- ➔ Adjustable Output Linear Swing, Flat Gain, and Equalization via I2C or Pin Control
- ➔ 100Ω Differential CML I/Os
- ➔ Automatic Receiver Detect
- ➔ Auto Slumber Mode for Adaptive Power Management
- ➔ Supply Voltage 3.3V
- ➔ Temperature Range: -40°C to 70°C
- ➔ Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- ➔ Halogen and Antimony Free. "Green" Device (Note 3)
- ➔ Packaging (Pb-free & Green):
 - 40-contact, ZLC40 (TQFN)

Applications

- ➔ Notebooks
- ➔ Mobile Phones
- ➔ Tablets
- ➔ Docking Station

Description

PI3EQX10612 is a low-power, high-performance, 10Gbps 2-port USB 3.1 Gen-2/Gen-1 Mux/DeMux ReDriver.

The 2-Port Mux/DeMux ReDriver

The ReDriver provides programmable equalization, swing and flat gain to optimize performance over a variety of physical mediums by reducing intersymbol interference. The ReDriver supports two 100Ω differential CML data I/Os between the Protocol ASIC to a switch fabric, over cable, or to extend the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver. A low-level input signal detection and output squelch function is provided for each channel. Each channel operates fully independently. The channels' input signal level determines whether the output is active.

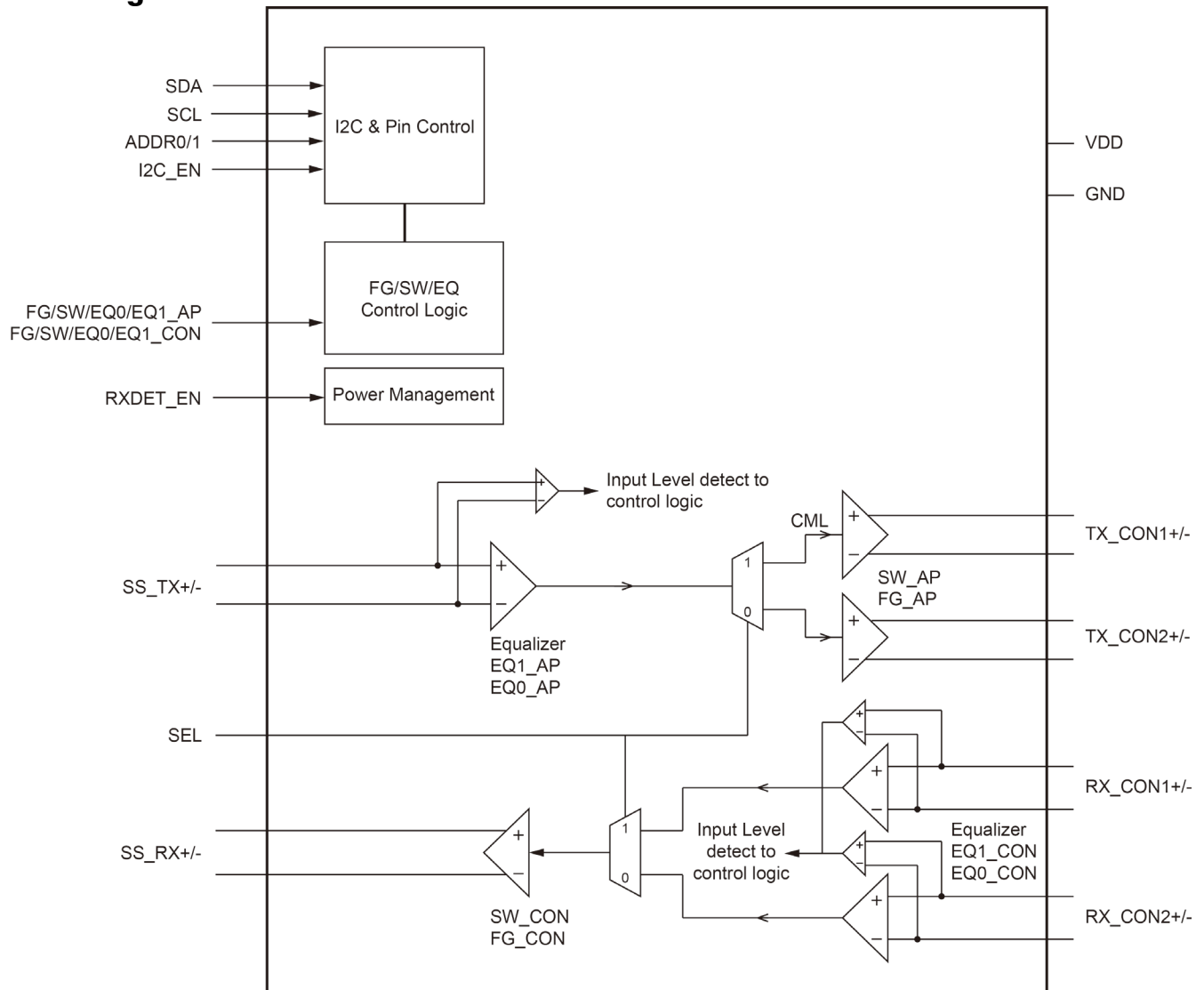
The ReDriver also includes an adaptive power management feature to maximize battery life for power sensitive consumer devices.

ReDriver is a trademark of Diodes Incorporated.

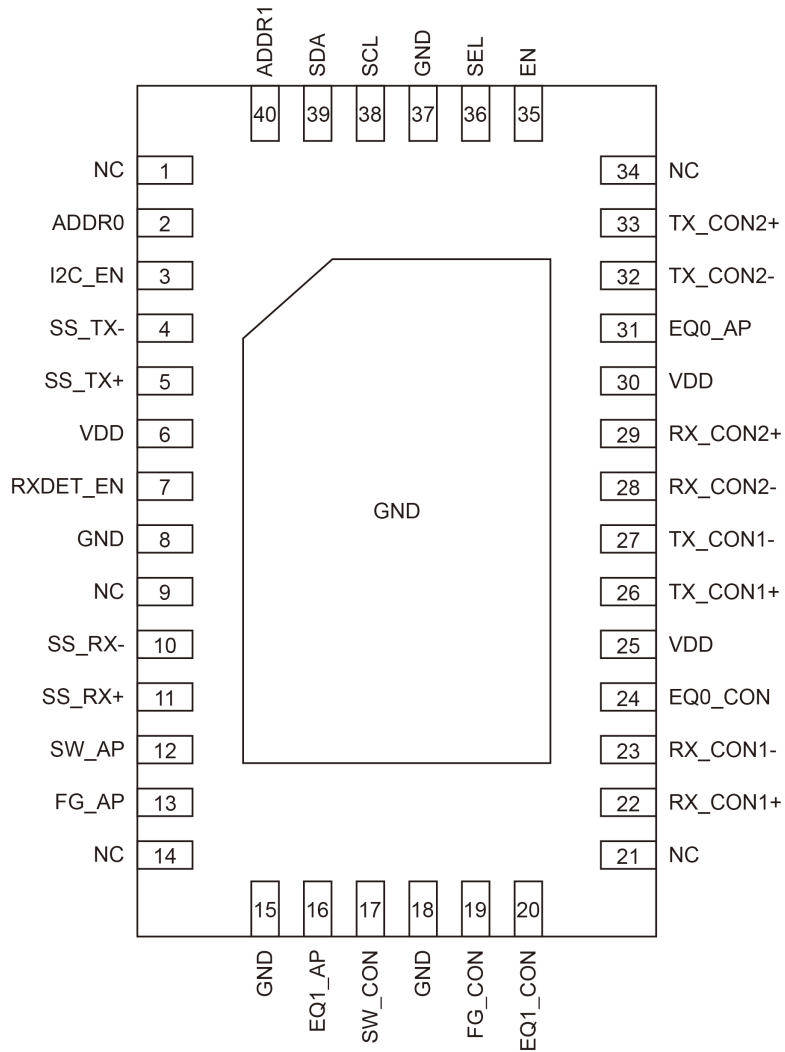
Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Block Diagram



Pin Configuration



Pin Descriptions

Pin #	Pin Name	I/O	Description
Thermal PAD, 8, 15,18,37	GND	Ground	Ground pin. Thermal pad.
2, 40	ADDR0, ADDR1	I	Input pins to indicate I2C address: Please refer to Table of I2C slave address
3	I2C_EN	I	Input pin to enable I2C mode (with internal 300kΩ pull-up resistor). HIGH: I2C mode LOW: Pin control mode
5,4 22,23 29,28	SS_TX+, SS_TX-, RX_CON1+, RX_CON1-, RX_CON2+, RX_CON2-	I	Input terminals. With selectable input termination between 50Ω to VDD, 75kΩ to VbiasRX, or 75kΩ to GND.
6,25,30	VDD	Power	Dedicated 3.3V Power Supply
7	RXDET_EN	I	ReDriver Loading Detection Enable Pin (with internal 300kΩ pull-up resistor). HIGH: ReDriver Loading Detection Enabled (Default Setting in Application) LOW: ReDriver Loading Detection Disabled
11,10 26,27 33,32	SS_RX+,SS_RX-, TX_CON1+,TX_CON1-, TX_CON2+, TX_CON2-	O	Output terminals. With selectable output termination between 50Ω to VbiasTx, 6kΩ to VbiasTx, 75kΩ to VbiasTx and 75kΩ to GND.
12,13,16,31	SW_AP FG_AP EQ1_AP, EQ0_AP	I	SW/FG/EQ setup for USB channels with receiver terminal is connected to AP Side. Please refer to truth table in Page 13.
17,19,20,24	SW_CON FG_CON EQ1_CON, EQ0_CON	I	SW/FG/EQ setup for USB channels with receiver terminal is connected to Connector Side. Please refer to truth table in Page 13.
35	EN	I	Active-high enable input pin (with internal 300kΩ pull-up resistor). HIGH: Enabled/Active State LOW: Disabled/Low Power State
36	SEL	I	Input Pin to select USB channel (with internal 300kΩ pull-up resistor). Please refer to truth table in Page 13.
38	SCL	I	I2C communication clk signal
39	SDA	I/O	I2C communication data signal
1,9,14,21,34	NC	—	No connection

Maximum Ratings

Storage Temperature	-65 to 150	°C
Supply Voltage	-0.5 to 3.8	V
Voltage of 3.3V IO pins (SCL, SDA, RXDET_EN, ADDR0/1, SEL, EN, SW_AP, FG_AP, EQ1_AP, EQ0_AP, SW_CON, FG_CON, EQ1_CON, EQ0_CON)	-0.5 to VDD+0.5	V
Voltage of SS_TX+/-, SS_RX+/-, TX_CON1/2 +/-, RX_CON1/2 +/-	-0.5 to VDD+0.5	V
Sink Current from SDA	10	mA
Continuous Input Current to SS_TX+/-, RX_CON1/2 +/-	±30	mA
ESD (HBM)	2KV	—

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Symbol	Parameter	Min.	Max.	Units
V _{DD}	Supply Voltage	3.0	3.6	V
V _{IO}	Voltage of IO pins (SCL, SDA, RXDET_EN, ADDR0/1, SEL, EN, SW_AP, FG_AP, EQ1_AP, EQ0_AP, SW_CON, FG_CON, EQ1_CON, EQ0_CON)	0	3.6	V
V _{TXRX}	Voltage of SS_TX+/-, SS_RX+/-, TX_CON1/2 +/-, RX_CON1/2 +/-	0	3.6	V
V _{NOISE}	Supply Noise up to 50MHz	—	100	mVpp
T _A	Operating Temperature	-40	70	°C

ReDriver AC/DC Electrical Characteristics

Power Consumption (VDD)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{PD}	Typical Pin Power Down Current	EN=0	—	26	100	μA
I_{DDQ_PD}	I2C Power Down Current	EN=1 I2C Byte4<7:4>=1111	—	—	340	μA
USB 3.1 Gen 2 Mode						
I_{U0}	Current in USB U0 Mode	EN=1, USB U0 mode	—	80	112	mA
I_{U1}	Current in USB U1 Mode	EN=1, USB U1 mode	—	16	20	mA
$I_{U2/U3}$	Current in USB U2/U3 Mode	EN=1, USB U2/U3 mode	—	0.5	0.6	mA
I_{RXDET}	Current RXDET Mode	EN=1, RXDET mode	—	0.5	0.6	mA
4-Level Control Pins (FG_AP, FG_CON, EQ1_AP, EQ0_AP, EQ1_CON, EQ0_CON, SW_AP, SW_CON)						
V_{IH}	DC Input Logic High	—	$0.92 \times VDD$	VDD	—	V
V_{IF}	DC Input Logic “Float”	—	$0.59 \times VDD$	$0.67 \times VDD$	$0.75 \times VDD$	V
V_{IR}	DC Input Logic with Rext to GND	—	$0.25 \times VDD$	$0.33 \times VDD$	$0.41 \times VDD$	V
V_{IL}	DC Input Logic Low	—	—	GND	$0.08 \times VDD$	V
I_{IH}	Input High Current	—	—	—	50	μA
I_{IL}	Input Low Current	—	-75	—	—	μA
Rext	External Resistance Connects to GND ($\pm 5\%$)	—	64.6	68	71.4	k Ω
2-Level Control Pins (EN, SEL, ADDR0/1, RXDET_EN)						
V_{IH}	DC Input Logic High	—	2.0	—	—	V
V_{IL}	DC Input Logic Low	—	—	—	0.8	V
I_{IH}	Input High Current	—	—	—	25	μA
I_{IL}	Input Low Current	—	-25	—	—	μA
I2C Interface Pins (SCL, SDA)						
V_{IH}	DC Input Logic High	—	1.1	—	—	V
V_{IL}	DC Input Logic Low	—	—	—	0.4	V

USB Differential Channel

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
USB Differential Input						
$C_{RXPARASITIC}$	The Parasitic Capacitor for RX	—	—	—	1.0	pF
$R_{RX-DIFF-DC}$	DC Differential Input Impedance	—	72	—	120	Ω
$R_{RX-SINGLE-DC}$	DC Single Ended Input Impedance	DC impedance limits are need to guarantee RxDet. Measured with respect to GND over a voltage of 500mV max	18	—	30	Ω
$Z_{RX-HIZ-DC-PD}$	DC Input CM Input Impedance for V>0 During Reset or Power Down	(Vcm=0 to 500mV)	25	—	—	k Ω
$C_{AC_COUPLING}$	AC Coupling Capacitance	—	75	—	265	nF
$V_{RX-CM-AC-P}$	Common Mode Peak Voltage	AV up to 5GHz	—	—	150	mVpeak
$V_{RX-CM-DC-Active-Idle-Delta-P}$	Common Mode Peak Voltage	Between U0 and U1, Ac up to 5GHz	—	—	200	mVpeak
USB Differential Output						
$V_{TX-DIFF-PP}$	Output Differential p-p Voltage Swing	Differential Swing $ V_{TX-D+} - V_{TX-D-} $	—	—	1.2	Vppd
$R_{TX-DIFF-DC}$	DC Differential TX Impedance	—	72	—	120	Ω
$V_{TX-RCV-DET}$	Amount of Voltage Change Allowed During RxDet	—	—	—	600	mV
$C_{ac\ coupling}$	AC Coupling Capacitance	—	75	—	265	nF
$T_{TX-EYE(10Gbps)}$	Transmitter Eye, Include all Jitter	At the silicon pad.	0.646	—	—	UI

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
		10Gbps				
T _{TX-EYE(5Gbps)}	Transmitter Eye, Include all Jitter	At the silicon pad. 5Gbps	0.625	—	—	UI
T _{TX-DJ-DD(10Gbps)}	Transmitter Deterministic Jitter	At the silicon pad. 10Gbps	—	—	0.17	UI
T _{TX-DJ-DD(5Gbps)}	Transmitter Deterministic Jitter	At the silicon pad. 5Gbps	—	—	0.205	UI
C _{TXPARASITIC}	The Parasitic Capacitor for TX	—	—	—	1.1	pF
R _{TX-DC-CM}	Common mode DC output Impedance	—	18	—	30	Ω
V _{TX-DC-CM}	Instantaneous Allowed DC Common Mode Voltage at the Connector Side of the AC Coupling Capacitors	V _{TX-D+} +V _{TX-D-} /2	0	—	2.2	V
V _{TX-C}	Common-Mode Voltage	V _{TX-D+} +V _{TX-D-} /2	VDD-2	—	VDD	V
V _{TX-CM-AC-PP-Active}	Active Mode TX AC Common Mode Voltage	V _{TX-D+} +V _{TX-D-} for both time and amplitude	—	—	100	mVpp
V _{TX-CM-DC-Active_Idle-Delta}	Common Mode Delta Voltage Avg _{uo} (V _{TEX-D+} + V _{TX-D-})/2 - Avg _{ul} (V _{TX-D+} + V _{TX-D-})/2	Between U0 to U1	—	—	200	mV-peak
V _{TX-Idle-Diff-AC-pp}	Idle Mode AC Common Mode Delta Voltage V _{TX-D+} -V _{TX-D-}	Between Tx+ and Tx- in idle mode. Use the HPF to remove DC components. =1/LPF. No AC and DC signals are applied to Rx terminals.	—	—	10	mVppd
V _{TX-Idle-Diff-DC}	Idle Mode DC Common Mode Delta Voltage V _{TX-D+} -V _{TX-D-}	Between Tx+ and Tx- in idle mode. Use the LPF to remove DC components. =1/HPF. No AC and DC signals are applied to Rx terminals.	—	—	10	mV
G _p	Peaking Gain (Compensation at 5GHz, Relative to 100MHz, 100mV _{p-p} Sine Wave Input)	EQ<3:0>=0000 EQ<3:0>=0101 EQ<3:0>=1010 EQ<3:0>=1111	—	6.42 9.5 11.77 13.54	—	dB
		Variation around typical	-3	—	+3	dB
G _F	Flat Gain (100MHz, EQ<3:0>=0000, SW<1:0>=01)	FG<1:0>=00 FG<1:0>=01 FG<1:0>=10 FG<1:0>=11	—	-2.07 -0.24 +0.62 +1.77	—	dB
		Variation around typical	-3	—	+3	dB
V _{SW_100M}	-1dB Compression Point Output Swing (at 100MHz)	SW<1:0>=00 SW<1:0>=01	—	900 1000	—	mVppd
V _{SW_5G}	-1dB Compression Point Output Swing (at 5GHz)	SW<1:0>=00 SW<1:0>=01	—	600 750	—	mVppd
DD _{NEXT} ^{Note3}	Differential Near-End Crosstalk	100MHz to 5GHz	—	-45	—	dB
DD _{FEXT} ^{Note3}	Differential Far-End Crosstalk	100MHz to 5GHz	—	-45	—	dB

V _{NOISE-INPUT}	Input-Referred Noise ⁽²⁾	100MHz to 5GHz, FG<1:0>=11, EQ<3:0>=0000, SW<1:0>=01	—	0.6	—	mV _{RMS}
		100MHz to 5GHz, FG<1:0>=11, EQ<3:0>=1111, SW<1:0>=01	—	0.5	—	
V _{NOISE-OUTPUT}	Output-Referred Noise ⁽²⁾	100MHz to 5GHz, FG<1:0>=11, EQ<3:0>=0000, SW<1:0>=01	—	0.8	—	mV _{RMS}
		100MHz to 5GHz, FG<1:0>=11, EQ<3:0>=1111, SW<1:0>=01	—	1	—	mV _{RMS}
S11	Input Return Loss	10 MHz to 4.1 GHz differential	—	-13.0	—	dB
		1 GHz to 4.1 GHz common mode	—	-5.0	—	dB
S22	Output Return Loss	10 MHz to 4.1 GHz differential	—	-15	—	dB
		1 GHz to 4.1 GHz common mode	—	-6.0	—	dB
Signal and Frequency Detectors						
V _{TH_UPM}	Unplug Mode Detector Threshold	Threshold of LFPS when the input impedance of the ReDriver is 67kohm to VbiasRx only. Used in the unplug mode.	200	—	800	mVppd
V _{TH_DSM}	Deep Slumber Mode Detector Threshold	LFPS signal threshold in Deep slumber mode	100	—	600	mVppd
V _{TH_AM}	Active Mode Detector Threshold	Signal threshold in Active and slumber mode	65	—	175	mVppd
F _{TH}	LFPS Frequency Detector	Detect the frequency of the input CLK pattern	100	—	400	MHz
T _{ON_UPM}	Turn on of Unplug Mode	TX pin to RX pin latency when input signal is LFPS	—	—	3	ms
T _{ON_DSM}	Turn on of Deep Slumber Mode		—	—	5	μs
T _{ON_SM}	Turn on of Slumber Mode		—	—	20	ns

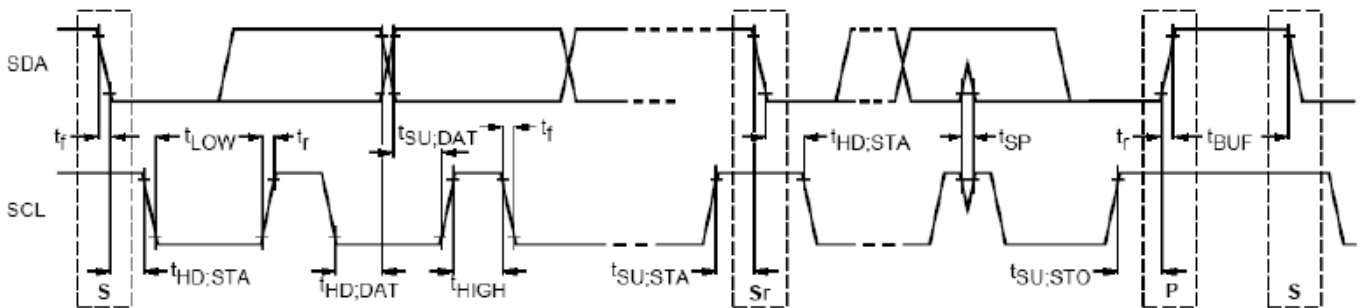
- Note:
1. Measured using a vector-network analyzer (VNA) with -15dBm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50 Ω .
 2. Guaranteed by design and characterization.
 3. Subtract the Channel Gain from the Total Gain to get the Actual Crosstalk

I²C AC Electrical Characteristics

Symbol	Parameter	Standard Mode I ² C		Fast Mode I ² C		Fast Mode Plus I ² C		Unit
		Min	Max	Min	Max	Min	Max	—
f _{SCL}	SCL Clock Frequency	0	100	0	400	0	1000	kHz
t _{BUF}	Bus Free Time Between a STOP and START Condition	4.7	—	1.3	—	0.5	—	μs
t _{HD;STA}	Hold Time (Repeated) START Condition	4.0	—	0.6	—	0.26	—	μs
t _{SU;STA}	Setup Time for a Repeated START Condition	4.7	—	0.6	—	0.26	—	μs
t _{SU;STO}	Setup Time for STOP Condition	4.0	—	0.6	—	0.26	—	μs
t _{VD;ACK} ^[1]	Data Valid Acknowledge Time	—	3.45	—	0.9	—	0.45	μs
t _{HD;DAT} ^[2]	Data Hold Time	0	—	0	—	0	—	ns
t _{VD;DAT}	Data Valid Time	—	3.45	—	0.9	—	0.45	ns
t _{SU;DAT}	Data Setup Time	250	—	100	—	50	—	ns
t _{LOW}	LOW Period of the SCL Clock	4.7	—	1.3	—	0.5	—	μs
t _{HIGH}	HIGH Period of the SCL Clock	4.0	—	0.6	—	0.26	—	μs
t _f	Fall Time of Both SDA and SCL Signals	—	300	—	300	—	120	ns
t _r	Rise Time of Both SDA and SCL Signals	—	1000	—	300	—	120	ns
t _{SP}	Pulse Width of Spikes that must be Suppressed by the Input Filter	—	50	—	50	—	50	ns

Notes:

1. A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement t_{SETDAT} ≥ 250ns must be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{r_max} + t_{SETDAT} = 1000 + 250 = 1250ns (according to the standard-mode I²C bus specification) before the SCL line is released.
2. C_b equals the total capacitance of one BUS line in pF. If mixed with high-speed devices, faster fall times are allowed according to the I²C specification.

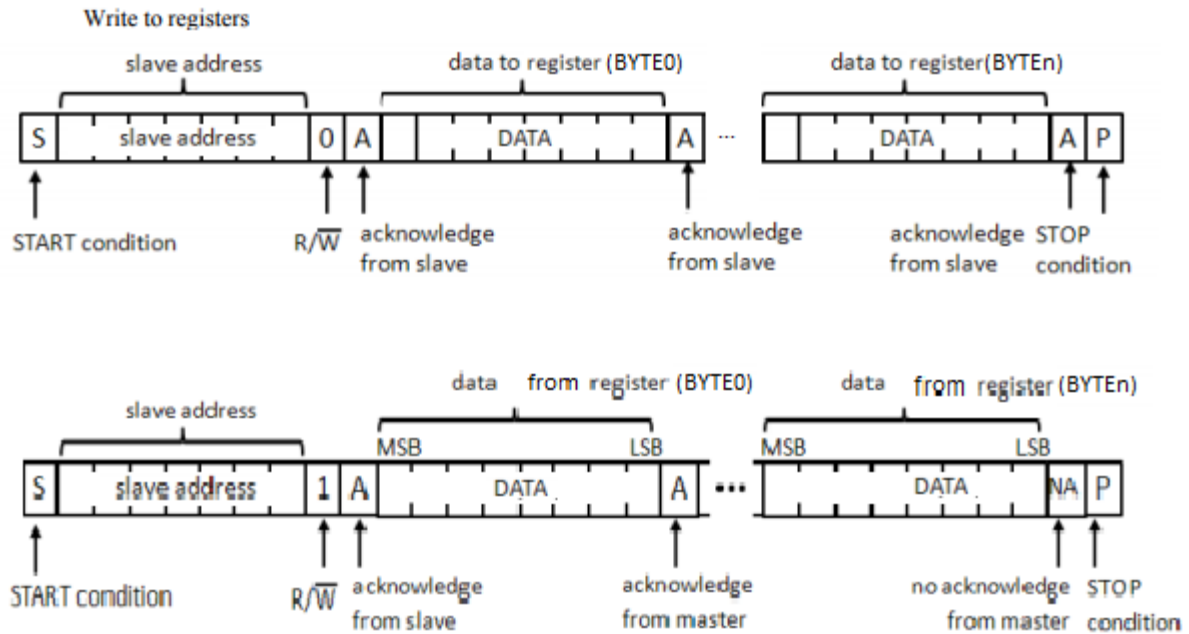


Definition of Timing for Full-Speed Mode Devices on the I²C Bus

I²C Slave Address

I2C_EN	ADDR1	ADDR0	ReDriverI2C Slave Address
VDD	GND	GND	A0h
VDD	GND	VDD	A2h
VDD	VDD	GND	A4h
VDD	VDD	VDD	A6h
GND	X	X	Pin Mode

I²C Data Transfer



***Registers of ReDriver can be Read/Written in Bulk Mode Only**

ReDriver Detailed Description

ReDriver Register Table

Register Assignment				
BYTE 0 (Revision and Vendor ID Register)				
Bit	Type	Power-up Condition	Control Affected	Comment
7	RO	0	Revision ID	Rev# = 0000
6	RO	0		
5	RO	0		
4	RO	0		
3	RO	0	Vendor ID	Pericom ID = 0011
2	RO	0		
1	RO	1		
0	RO	1		
BYTE 1 (Device Type/Device ID Register)				
Bit	Type	Power-up Condition	Control Affected	Comment
7	RO	0	Device Type	Device Type 0000 = Passive MUX 0001 = Active MUX
6	RO	0		
5	RO	0		
4	RO	1		
3	RO	0	Device ID	Device ID = 0001
2	RO	0		
1	RO	0		
0	RO	1		
BYTE 2 (Byte Count Register 32 Bytes)				
Bit	Type	Power-up Condition	Control Affected	Comment
7	RO	0	Register Byte count	I2C byte count = 32 bytes
6	RO	0		
5	RO	1		
4	RO	0		
3	RO	0		
2	RO	0		
1	RO	0		
0	RO	0		
BYTE 3 (Channel Assignment and Receiver Detection Enable Control)				
Bit	Type	Power-up Condition	Control Affected	Comment
7	R/W	0	—	Reserved
6	R/W	1	CONF<2>	Channel Assignment
5	R/W	0	CONF<1>	
4	R/W	1	CONF<0>	
3	R/W	0	—	Reserved
2	R/W	0 if RXDET_EN pin=1; 1 if RXDET_EN pin=0	RXDET_EN#	Far-end receiver detection enable/disable 0 = Enable 1 = Disable
1	R/W	1	—	Reserved
0	R/W	0	—	Reserved
BYTE 4 (Power Down Control)				
Bit	Type	Power-up Condition	Control Affected	Comment
7	R/W	0	PD_CON_Rx1	CONx power override 0 – Normal operation 1 – Force the CONx to power down state
6	R/W	0	PD_CON_Tx1	
5	R/W	0	PD_CON_Tx2	
4	R/W	0	PD_CON_Rx2	
3	R/W	0	—	Reserved
2	R/W	0	—	Reserved
1	R/W	0	—	Reserved
0	R/W	0	—	Reserved

BYTE 5 (Equalization, Flat Gain, and -1dB Linear Swing Setting of CON_Rx2)				
Bit	Type	Power-up condition	Control Affected	Comment
7	R/W	0	EQ_CON<3>	CON_Rx2 setting configuration Equalizer Flat Gain Swing
6	R/W	0	EQ_CON<2>	
5	R/W	0	EQ_CON<1>	
4	R/W	0	EQ_CON<0>	
3	R/W	0	FG_CON<1>	
2	R/W	1	FG_CON<0>	
1	R/W	0	SW_CON<1>	
0	R/W	1	SW_CON<0>	
BYTE 6 (Equalization, Flat Gain, and -1dB Linear Swing Setting of AP_Tx2)				
Bit	Type	Power-up Condition	Control Affected	Comment
7	R/W	0	EQ_AP<3>	CON_Tx2 setting configuration Equalizer Flat Gain Swing
6	R/W	0	EQ_AP<2>	
5	R/W	0	EQ_AP<1>	
4	R/W	0	EQ_AP<0>	
3	R/W	0	FG_AP<1>	
2	R/W	1	FG_AP<0>	
1	R/W	0	SW_AP<1>	
0	R/W	1	SW_AP<0>	
BYTE 7 (Equalization, Flat Gain, and -1dB Linear Swing Setting of AP_Tx1)				
Bit	Type	Power-up Condition	Control Affected	Comment
7	R/W	0	EQ_AP<3>	CON_Tx1 setting configuration Equalizer Flat Gain Swing
6	R/W	0	EQ_AP<2>	
5	R/W	0	EQ_AP<1>	
4	R/W	0	EQ_AP<0>	
3	R/W	0	FG_AP<1>	
2	R/W	1	FG_AP<0>	
1	R/W	0	SW_AP<1>	
0	R/W	1	SW_AP<0>	
BYTE 8 (Equalization, Flat Gain, and -1dB Linear Swing Setting of CON_Rx1)				
Bit	Type	Power-up Condition	Control Affected	Comment
7	R/W	0	EQ_CON<3>	CON_Rx1 setting configuration Equalizer Flat Gain Swing
6	R/W	0	EQ_CON<2>	
5	R/W	0	EQ_CON<1>	
4	R/W	0	EQ_CON<0>	
3	R/W	0	FG_CON<1>	
2	R/W	1	FG_CON<0>	
1	R/W	0	SW_CON<1>	
0	R/W	1	SW_CON<0>	
BYTE 9-11 (Reserved)				
BYTE 12 (Threshold, Feature Enable/ Disable, and Timing Setting)				
Bit	Type	Power-up Condition	Control Affected	Comment
7	R/W	0	IDET_VTH<1>	High Speed channel signal detector threshold setting 00 50mVppd 01 65mVppd (Default) 10 80mVppd 11 95mVppd
6	R/W	1	IDET_VTH<0>	
5	R/W	1	Reserved	—
4	R/W	1	Reserved	—
3	R/W	0	Reserved	—
2	R/W	0	Reserved	—
1	R/W	0	Reserved	—
0	R/W	1	Reserved	—
BYTE 13-31 (Reserved)				

Equalization Setting (dB):

EQ1pin	EQ0pin	EQ3	EQ2	EQ1	EQ0	@ 2.5GHz	@ 3GHz	@ 4GHz	@ 5GHz	@ 6GHz	Note
0	F	0	0	0	0	3.57	4.22	5.44	6.42	7.27	Default
0	1	0	0	0	1	3.83	4.56	5.93	7.04	8.00	—
0	0	0	0	1	0	4.13	4.93	6.47	7.71	8.76	—
0	R	0	0	1	1	4.41	5.29	6.95	8.29	9.42	—
R	1	0	1	0	0	4.98	5.89	7.61	8.99	10.14	—
R	F	0	1	0	1	5.25	6.23	8.05	9.50	10.70	—
R	R	0	1	1	0	5.55	6.59	8.51	10.04	11.28	—
R	0	0	1	1	1	5.82	6.92	8.93	10.51	11.78	—
F	0	1	0	0	0	6.39	7.44	9.39	10.93	12.16	—
F	R	1	0	0	1	6.63	7.74	9.76	11.34	12.60	—
F	F	1	0	1	0	6.90	8.05	10.14	11.77	13.05	—
F	1	1	0	1	1	7.14	8.34	10.49	12.15	13.44	—
1	R	1	1	0	0	7.51	8.71	10.87	12.53	13.81	—
1	0	1	1	0	1	7.74	8.97	11.18	12.87	14.15	—
1	1	1	1	1	0	7.98	9.25	11.51	13.23	14.51	—
1	F	1	1	1	1	8.20	9.51	11.81	13.54	14.82	—

Flat Gain Setting:

FGpin is the selection pin for the DC gain.

FGpin	FG<1:0>	Flat Gain Setting (dB)
R	00	-2.07
F	01	-0.24 (Default)
0	10	0.62
1	11	1.77

Swing -1dB Compression Point Output Swing Setting:

SWpin is the selection pin for SW.

SWpin	SW<1:0>	Swing Setting
0	00	900 mVppd
1	01	1000 mVppd (Default)
F	10	1100 mVppd
R	11	1200 mVppd

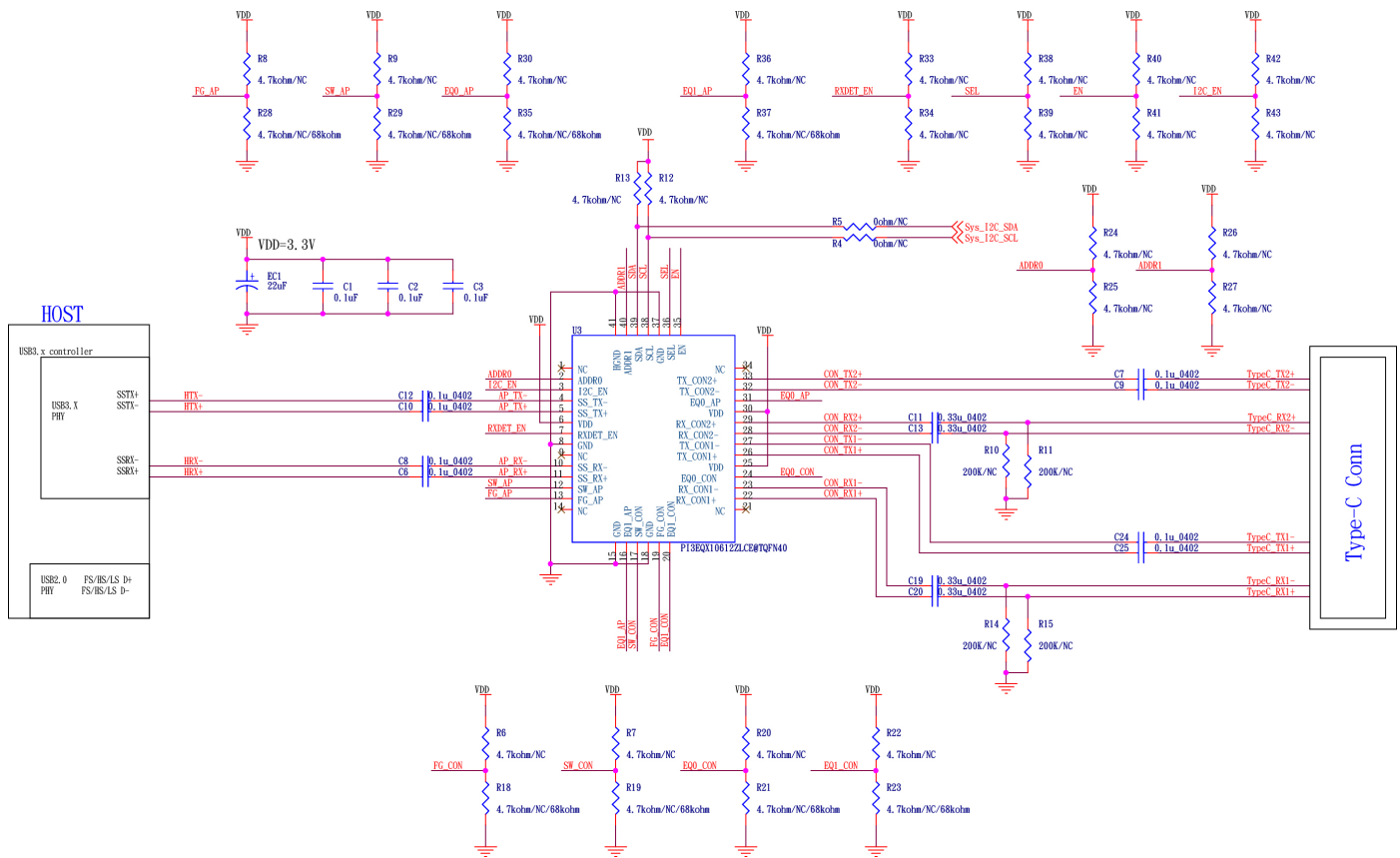
ReDriver Connection in Pin Mode

EN	SEL	ReDriver Status
0	X	Inactive
1	1	TX CON1/RX CON1 Active
1	0	TX CON2/RX CON2 Active

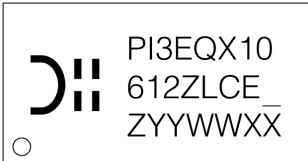
ReDriver Connection in I2C Mode

EN	BYTE3 CONF<2:0>	ReDriver Status
0	X	Inactive
1	100	TX CON1/RX CON1 Active
1	101 (default)	TX CON2/RX CON2 Active

Application Diagram



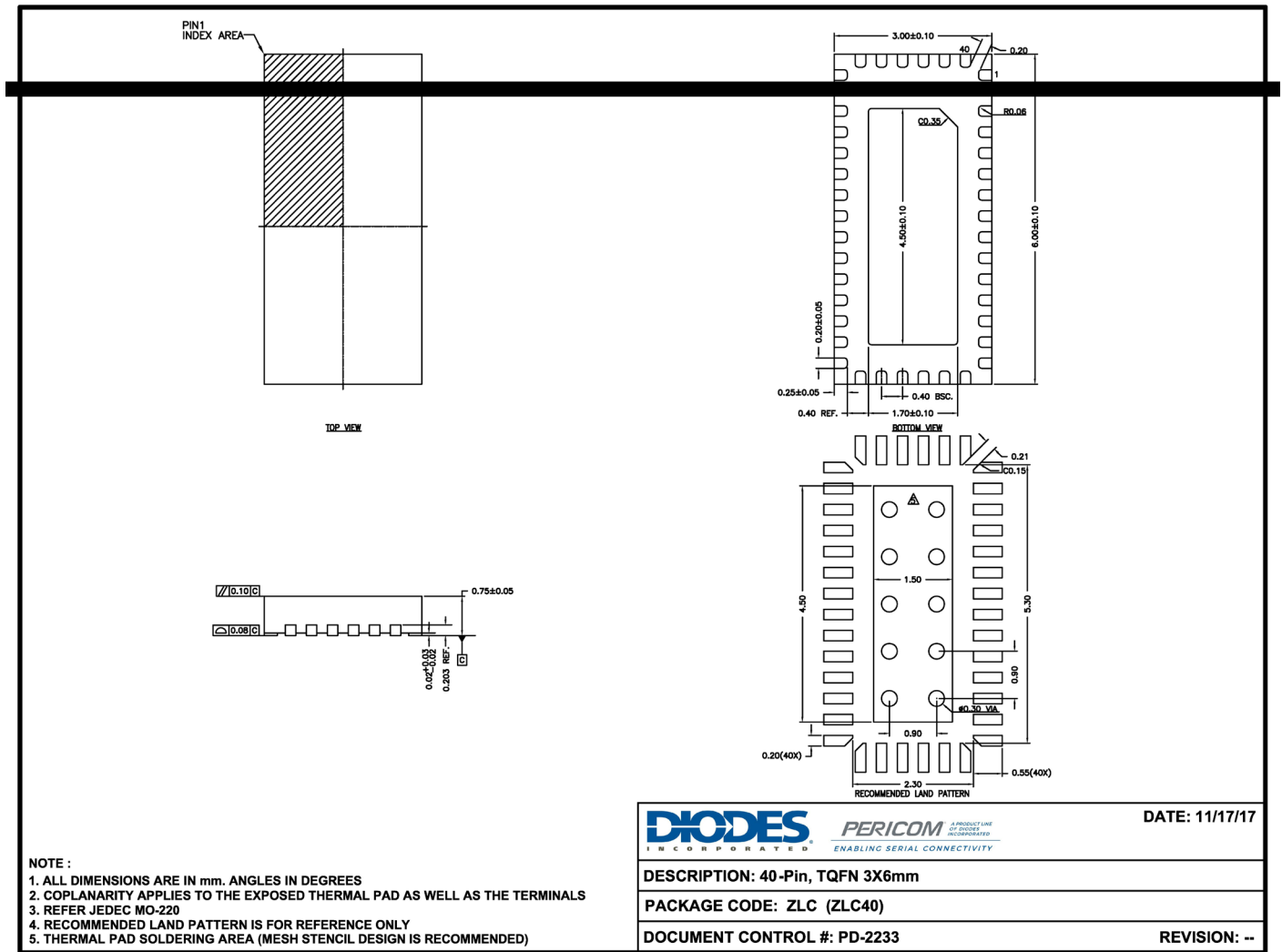
Part Marking



Z: Die Rev
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Packaging Mechanical

40-TQFN (ZLC)



For latest package information:

See <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>.

Ordering Information

Ordering Number	Package Code	Package Description
PI3EQX10612ZLCEX	ZLC	40-Pin, 3mm x 6mm (TQFN)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

IMPORTANT NOTICE

DIODES INCORPORATED MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Diodes Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Diodes Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on Diodes Incorporated website, harmless against all damages.

Diodes Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

Should Customers purchase or use Diodes Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Diodes Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

Products described herein may be covered by one or more United States, international or foreign patents pending. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks.

This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes Incorporated.

LIFE SUPPORT

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or
2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

Copyright © 2019, Diodes Incorporated
www.diodes.com