

**PI6C39X0202**

**Low Skew 1 to 2 Clock Buffer**

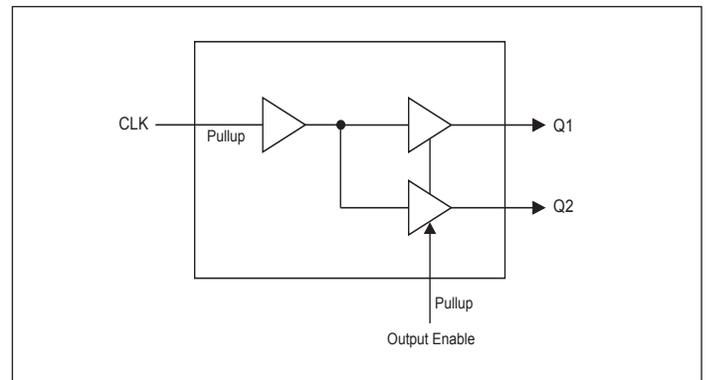
**Features**

- Low Skew Outputs (50 ps)
- Low Additive Jitter RMS: 50fs
- Input/Output Frequency up to 250MHz
- Operating Voltages of 1.5V to 3.3V
- Output Enable Pin tri-states outputs
- 3.3V Tolerant Input Clock
- Extended Temperature Range: -40°C to 105°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact@diodes.com) or your local Diodes representative.  
<https://www.diodes.com/quality/product-definitions/>
- Packaging (Pb-free & Green):
  - 8-pin, X1DFN (XEC)

**Description**

The PI6C39X0202 is a low skew, low additive jitter single input to two output clock buffer.

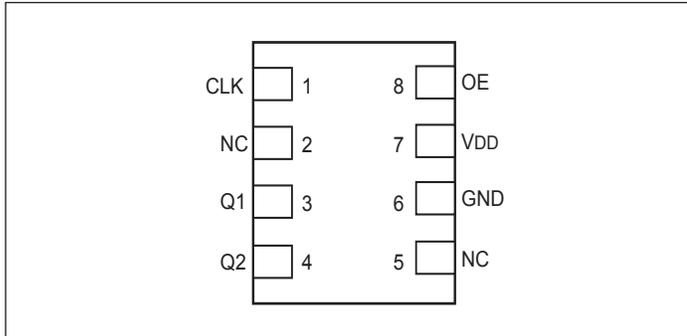
**Block Diagram**



Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, “Green” and Lead-free.
3. Halogen- and Antimony-free “Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Pin Configuration



## Pin Descriptions

Pin#	Pin Name	Pin Type	Pin Description
1	CLK	Input	Clock Input. 3.3V tolerant input. Internal pull-up resistor.
2	NC	NC	Not Connected.
3	Q1	Output	Clock Output 1.
4	Q2	Output	Clock Output 2.
5	NC	NC	Not Connected.
6	GND	Power	Connect to ground.
7	VDD	Power	Connect to 1.5V, 1.8V, 2.5V or 3.3V.
8	OE	Input	Output Enable. Tri-states outputs when low. Internal pull-up resistor.

## External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01  $\mu$ F should be connected between VDD on pin 7 and GND on pin 6, as close to the device as possible. A 33  $\Omega$  series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

## Maximum Ratings

Supply Voltage, VDD	4.6V
Output Enable and All Outputs	-0.5V to VDD+0.5V
CLK	-0.5V to 3.6V (VDD > 0V)
Storage Temperature	-65 to +150°C
Junction Temperature	125°C max
ESD Protection (HBM)	2000V

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (Extended)	-40		+105	°C
Power Supply Voltage (measured in respect to GND)	+1.425		+3.465	V

## DC Electrical Characteristics

**VDD = 1.5V ±5%**, Ambient temperature -40 to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage		1.425	1.5	1.575	V
V <sub>IH</sub>	Input High Voltage <sup>(1)</sup>	CLK, OE	0.7xVDD		VDD	V
V <sub>IL</sub>	Input Low Voltage <sup>(1)</sup>	CLK, OE			0.3xVDD	V
I <sub>IH</sub>	Input High Current	CLK, OE	-1		1	µA
I <sub>IL</sub>	Input Low Current	CLK, OE	-40			µA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -6mA	0.95			V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 6mA			0.45	V
IDD	Operating Supply Current	No load, 133 MHz		10	18	mA
Z <sub>O</sub>	Nominal Output Impedance			20		Ω
C <sub>IN</sub>	Input Capacitance	CLK, OE pin		5		pF

Notes: 1. Nominal switching threshold is VDD/2

### DC Electrical Characteristics Cont.

**VDD=1.8V ±5%**, Ambient temperature -40 to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage		1.7	1.8	1.89	V
V <sub>IH</sub>	Input High Voltage <sup>(1)</sup>	CLK, OE	0.7xVDD		VDD	V
V <sub>IL</sub>	Input Low Voltage <sup>(1)</sup>	CLK, OE			0.3xVDD	V
I <sub>IH</sub>	Input High Current	CLK, OE	-1		1	μA
I <sub>IL</sub>	Input Low Current	CLK, OE	-40			μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -10mA	1.4			V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 10mA			0.4	V
IDD	Operating Supply Current	No load, 133 MHz		13	21	mA
Z <sub>O</sub>	Nominal Output Impedance			20		Ω
C <sub>IN</sub>	Input Capacitance	CLK, OE pin		5		pF

Notes: 1. Nominal switching threshold is VDD/2

**VDD=2.5V ±5%**, Ambient temperature -40 to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage		2.375	2.5	2.625	V
V <sub>IH</sub>	Input High Voltage <sup>(1)</sup>	CLK, OE	0.7xVDD		VDD	V
V <sub>IL</sub>	Input Low Voltage <sup>(1)</sup>	CLK, OE			0.3xVDD	V
I <sub>IH</sub>	Input High Current	CLK, OE	-1		1	μA
I <sub>IL</sub>	Input Low Current	CLK, OE	-60			μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -16mA	1.8			V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 16mA			0.4	V
IDD	Operating Supply Current	No load, 133 MHz		18	26	mA
Z <sub>O</sub>	Nominal Output Impedance			20		Ω
C <sub>IN</sub>	Input Capacitance	CLK, OE pin		5		pF

Notes: 1. Nominal switching threshold is VDD/2

## DC Electrical Characteristics Cont.

**VDD=3.3V ±5%**, Ambient temperature -40 to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage		3.135	3.3	3.465	V
V <sub>IH</sub>	Input High Voltage <sup>(1)</sup>	CLK, OE	0.7xVDD		VDD	V
V <sub>IL</sub>	Input Low Voltage <sup>(1)</sup>	CLK, OE			0.3xVDD	V
I <sub>IH</sub>	Input High Current	CLK, OE	-1		1	μA
I <sub>IL</sub>	Input Low Current	CLK, OE	-70			μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -25mA	2.2			V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 25mA			0.7	V
IDD	Operating Supply Current	No load, 133 MHz		22	35	mA
Z <sub>O</sub>	Nominal Output Impedance			20		Ω
C <sub>IN</sub>	Input Capacitance	CLK, OE pin		5		pF

Notes: 1. Nominal switching threshold is VDD/2

## AC Electrical Characteristics

**VDD=1.5V ±5%**, Ambient temperature -40 to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F <sub>OUT</sub>	Output Frequency		0		200	MHz
t <sub>OR</sub>	Output Rise Time	0.3V to 1.2V		1	1.6	ns
t <sub>OF</sub>	Output Fall Time	1.2V to 0.3V		1	1.6	ns
T <sub>PD</sub>	Propagation Delay <sup>(1)</sup>		2	3	5	ns
T <sub>SK</sub>	Output to Output Skew <sup>(2)</sup>	Rising edges at VDD/2		50	65	ps
t <sub>START-UP</sub>	Start-up Time	Part start-up time for valid outputs after VDD ramp-up			2	ms
t <sub>EN</sub>	Output Enable Time	C <sub>L</sub> < 5pF			3	cycles
t <sub>DIS</sub>	Output Disable Time	C <sub>L</sub> < 5pF			3	cycles

Notes:

1. With rail to rail input clock
2. Between any 2 outputs with equal loading.

### AC Electrical Characteristics Cont.

**VDD = 1.8V ±5%**, Ambient temperature -40 to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F <sub>OUT</sub>	Output Frequency		0		250	MHz
t <sub>OR</sub>	Output Rise Time	0.36V to 1.44V		0.6	1	ns
t <sub>OF</sub>	Output Fall Time	1.44V to 0.36V		0.6	1	ns
T <sub>PD</sub>	Propagation Delay <sup>(1)</sup>		1.3	2	4	ns
T <sub>SK</sub>	Output to Output Skew <sup>(2)</sup>	Rising edges at VDD/2		50	65	ps
J <sub>ADD</sub>	Additive Jitter	@156.25MHz, 12k to 20MHz		0.03	0.05	ps
t <sub>START-UP</sub>	Start-up Time	Part start-up time for valid outputs after VDD ramp-up			2	ms
t <sub>EN</sub>	Output Enable Time	C <sub>L</sub> < 5pF			3	cycles
t <sub>DIS</sub>	Output Disable Time	C <sub>L</sub> < 5pF			3	cycles

Notes:

1. With rail to rail input clock
2. Between any 2 outputs with equal loading.

**VDD = 2.5V ±5%**, Ambient temperature -40 to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F <sub>OUT</sub>	Output Frequency		0		250	MHz
t <sub>OR</sub>	Output Rise Time	0.5V to 2V		0.6	1	ns
t <sub>OF</sub>	Output Fall Time	2V to 0.5V		0.6	1	ns
T <sub>PD</sub>	Propagation Delay <sup>(1)</sup>		0.8	1.5	3	ns
T <sub>SK</sub>	Output to Output Skew <sup>(1)</sup>	Rising edges at VDD/2		50	65	ps
J <sub>ADD</sub>	Additive Jitter	@156.25MHz, 12k to 20MHz		0.035	0.05	ps
t <sub>START-UP</sub>	Start-up Time	Part start-up time for valid outputs after VDD ramp-up			2	ms
t <sub>EN</sub>	Output Enable Time	C <sub>L</sub> < 5pF			3	cycles
t <sub>DIS</sub>	Output Disable Time	C <sub>L</sub> < 5pF			3	cycles

Notes:

1. With rail to rail input clock
2. Between any 2 outputs with equal loading.

### AC Electrical Characteristics Cont.

**VDD=3.3V ±5%**, Ambient temperature -40 to +105°C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F <sub>OUT</sub>	Output Frequency		0		250	MHz
t <sub>OR</sub>	Output Rise Time	0.66V to 2.64V		0.6	1	ns
t <sub>OF</sub>	Output Fall Time	2.64V to 0.66V		0.6	1	ns
T <sub>PD</sub>	Propagation Delay <sup>(1)</sup>		0.8	1.0	2.5	ns
T <sub>SK</sub>	Output to Output Skew <sup>(2)</sup>	Rising edges at VDD/2		50	65	ps
J <sub>ADD</sub>	Additive Jitter	@156.25MHz, 12k to 20MHz		0.037	0.05	ps
t <sub>START-UP</sub>	Start-up Time	Part start-up time for valid outputs after VDD ramp-up			2	ms
t <sub>EN</sub>	Output Enable Time	C <sub>L</sub> < 5pF			3	cycles
t <sub>DIS</sub>	Output Disable Time	C <sub>L</sub> < 5pF			3	cycles

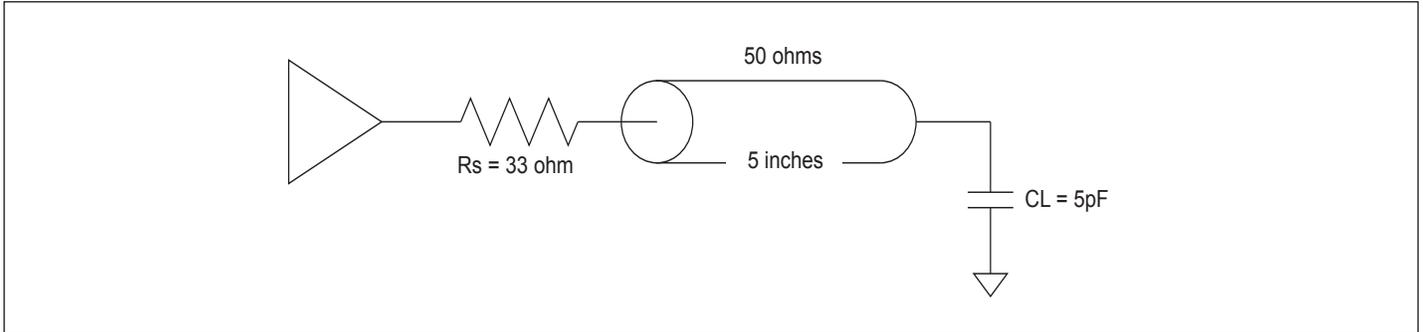
Notes:

1. With rail to rail input clock
2. Between any 2 outputs with equal loading.

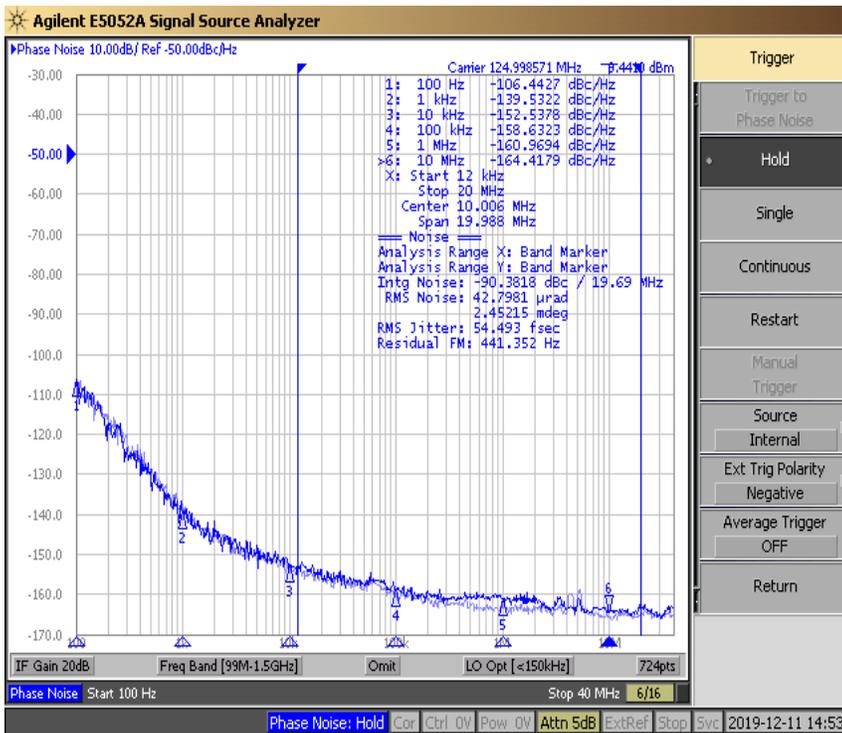
### Thermal Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
θ <sub>JA</sub>	Thermal Resistance Junction to Ambient	Still air		157		°C/W
θ <sub>JC</sub>	Thermal Resistance Junction to Case			42		°C/W

**Test Circuit**



**Additive Phase Noise Plot**



## Application Information

### Suggest for Unused Inputs and Outputs

#### LVC MOS Input Control Pins

It is suggested to add pull-up=4.7k and pull-down=1k for LVC MOS pins even though they have internal pull-up/down but with much higher value (>=50k) for higher design reliability.

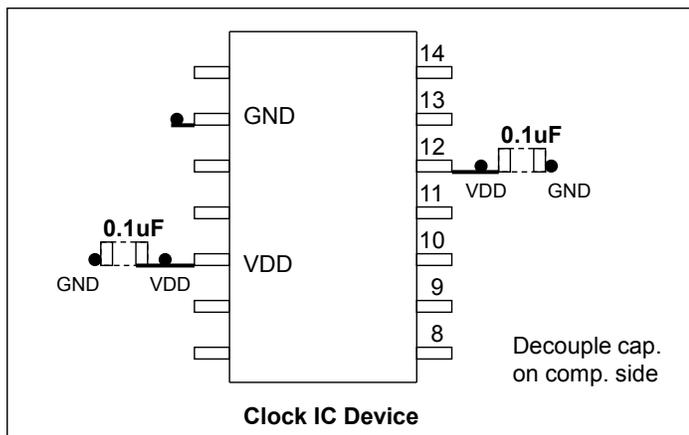
#### Outputs

All unused outputs are suggested to be left open and not connected to any trace. This can lower the IC power consumption.

### Power Decoupling & Routing

#### VDD Pin Decoupling

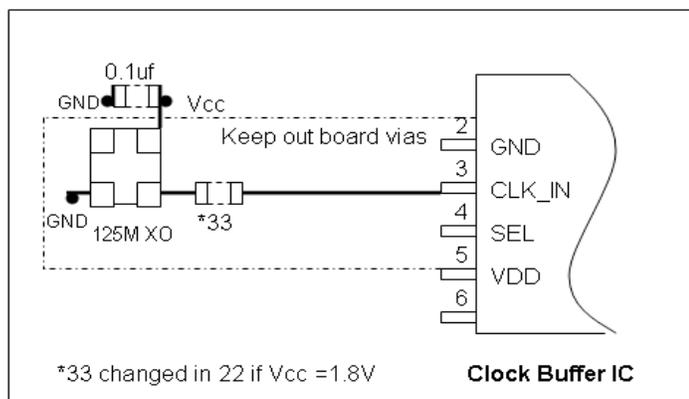
Each VDD pin must have a 0.1uF decoupling capacitor. For better decoupling, 1uF can be used. Locating the decoupling capacitor on the component side has better decoupling filter result as shown.



Placement of Decoupling Caps

### CMOS Clock Trace Routing

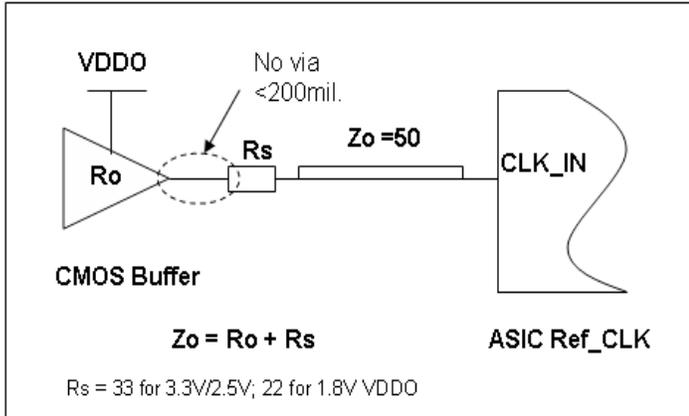
Please ensure that there is a sufficient keep-out area to the adjacent trace (>20mil.). In an example using a 125MHz XO driving a buffer IC, it is better to route the clock trace on the component side with a 33 ohm termination resistor.



## CMOS Output Termination

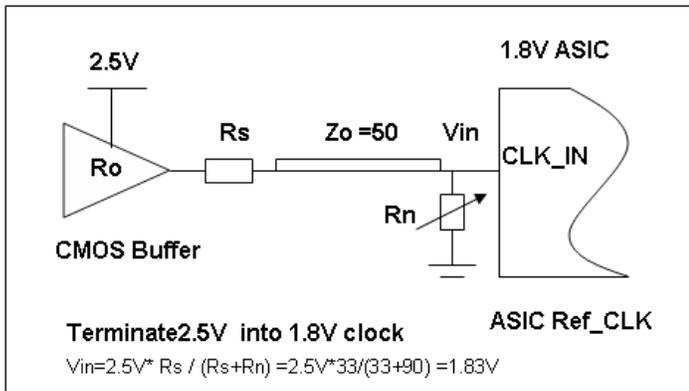
### Popular CMOS Output Termination

The most popular CMOS termination is a serial resistor close to the output pin ( $\leq 200\text{mil}$ ). It is simple and balances the drive strength. The resistor's value can be fine tuned for best performance during board bring-up based on VDDO voltage used.



### Combining Serial and Parallel Termination

Designers can also use a parallel termination for CMOS outputs. For example, a 50 ohm pull-down resistor can be used at the Rx side to reduce signal reflection, but it reduces the signals  $V_{\text{swing}}$  in half. This pull-down can be combined with a serial resistor to form a smaller clock voltage difference. The following diagram shows how to transition a 2.5V clock into 1.8V clock.



$R_s = 33$  ohm with  $R_n = 100$  ohm, to transition 3.3V CMOS to 2.5V

$R_s = 43$  ohm with  $R_n = 70$  ohm to transition 3.3V CMOS to 1.8V

## Clock Jitter Definitions

### Total Jitter = RJ + DJ

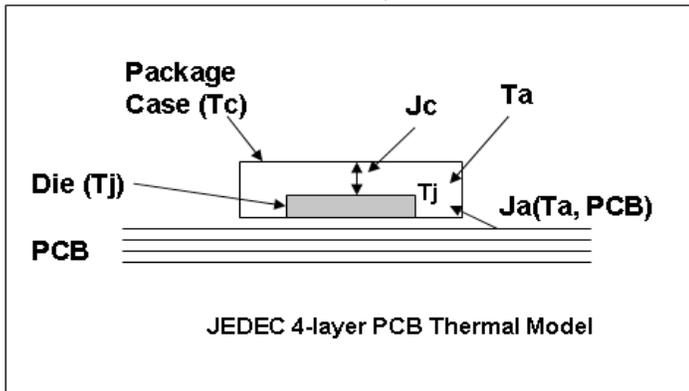
Random Jitter (RJ) is unpredictable and unbounded timing noise that can fit in a Gaussian math distribution in RMS. RJ test values are directly related with how long or how many test samples are available. Deterministic Jitter (DJ) is timing jitter that is predictable and periodic in fixed interference frequency. Total Jitter (TJ) is the combination of random jitter and deterministic jitter:  $TJ = \sqrt{RJ^2 + DJ^2}$ , where  $k$  is a factor based on total test sample count. JEDEC std. specifies digital clock TJ in 10k random samples.

### Phase Jitter

Phase noise is short-term random noise attached on the clock carrier and it is a function of the clock offset from the carrier, for example dBc/Hz@10kHz which is phase noise power in 1-Hz normalized bandwidth vs. the carrier power @10kHz offset. Integration of phase noise in plot over a given frequency band yields RMS phase jitter, for example, to specify phase jitter  $\leq 1$ ps at 12k to 20MHz offset band as SONET standard specification.

## Device Thermal Calculation

The JEDEC thermal model in a 4-layer PCB is shown below.



### JEDEC IC Thermal Model

Important factors to influence device operating temperature are:

- 1) The power dissipation from the chip ( $P_{chip}$ ) is after subtracting power dissipation from external loads. Generally it can be the no-load device  $I_{dd}$
- 2) Package type and PCB stack-up structure, for example, 1oz 4 layer board. PCB with more layers and are thicker has better heat dissipation
- 3) Chassis air flow and cooling mechanism. More air flow M/s and adding heat sink on device can reduce device final die junction temperature  $T_j$

The individual device thermal calculation formula:

$$T_j = T_a + P_{chip} \times J_a$$

$$T_c = T_j - P_{chip} \times J_c$$

$J_a$  \_\_\_ Package thermal resistance from die to the ambient air in C/W unit; This data is provided in JEDEC model simulation. An air flow of 1m/s will reduce  $J_a$  (still air) by 20~30%

$J_c$  \_\_\_ Package thermal resistance from die to the package case in C/W unit

$T_j$  \_\_\_ Die junction temperature in C (industry limit <125C max.)

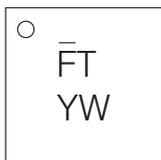
$T_a$  \_\_\_ Ambient air temperature in C

$T_c$  \_\_\_ Package case temperature in C

$P_{chip}$  \_\_\_ IC actually consumes power through  $I_{ee}/GND$  current

**PI6C39X0202**

**Part Marking**



FT: PI6C39X0202XECIE

Y: Year

W: Workweek

Line above first character denotes Lead-free and Green

**Packaging Mechanical: 8-X1DFN (XEC)**

**TOP VIEW**

**BOTTOM VIEW**

**RECOMMENDED LAND PATTERN**

SYMBOLS	MIN.	NOM.	MAX.
A	0.40	0.45	0.50
A1	0.00	0.02	0.05
A3	0.127 REF.		
b	0.20	0.25	0.30
D	1.95	2.00	2.05
E	1.95	2.00	2.05
e	0.50 BSC		
L	0.45	0.50	0.55

**NOTE :**  
 1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.  
 2. Ref JEDEC MO-287  
 3. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.

**DATE: 09/10/19**

**DESCRIPTION: 8-Contact, Extra Thin Dual Flat No-Lead (X1DFN)**

**PACKAGE CODE: XEC (XEC8)**

**DOCUMENT CONTROL #: PD-2242**

**REVISION: --**

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

**Ordering Information**

Ordering Code	Package Code	Package Description
PI6C39X0202XECIEX	XEC	8-contact, Extra Thin Dual Flat No-Lead (X1DFN)

**Notes:**

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. I = Industrial
5. E = Pb-free and Green
6. X suffix = Tape/Reel

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