PI3DPX8100

3.3V DisplayPort 1.4 8.1Gbps 4 Lane 2-to-1 Active Mux Switch with Linear Redriver

Features

- 2-to-1 mux switch configuration for 4-lane DisplayPort operation
- 8.1Gbps DP1.4 (RBR/HBR/HBR2/HBR3)
- LT-tunable capability for LTTPR redriver data path support
- Quad-level pin strap control through combinational logic table for equalizer gain value selection
- Quad-level pin strap control for flat gain and output swing linearity selection
- Input signal detection for automatic power saving mode
- Single power supply: 3.3v +/-0.3v
- Industrial temperature support: 0°C to +70°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 40-pin 3 x 6mm TQFN, (ZLD)

Description

The PI3DPX8100 is a 2-to-1 active mux switch for 4-lane DisplayPort link with data rate support for DP1.4. The maximum equalizer gain controls is +8.8dB (DP1.4@4.05GHz) to compensate the insertion loss along the channel connection.

The Link Training tunable linear Redriver™ design supports the LTTPR (Link Training Transparent PHY Repeater) redriver data path type. It ensures the differential signals conveying pre-shoot and de-emphasis equalization waveforms to be transmitted from source side to the receiver side to optimize the overall channel link adjustment conducted by the system transmitter and receiver. The CTLE equalizers are implemented at the inputs of the redriver to reduce the ISI jitters and compensate channel loss. The programmable flat gain and linearity adjustments support the eye diagram opening.

With the combinational logic control design, users can use pin strap method to select various EQ gains, flat gains and output swing linearity for flexible design tuning.

Applications

- Laptop and Desktop PCs
- Workstation and Server System
- Docking, KVM and PC Peripherals
- Display Monitors

Ordering Information

Ordering Number	Package Code	Description
PI3DPX8100ZLDEX	ZLD	40-Pin, 3 x 6mm (TQFN)

Notes:

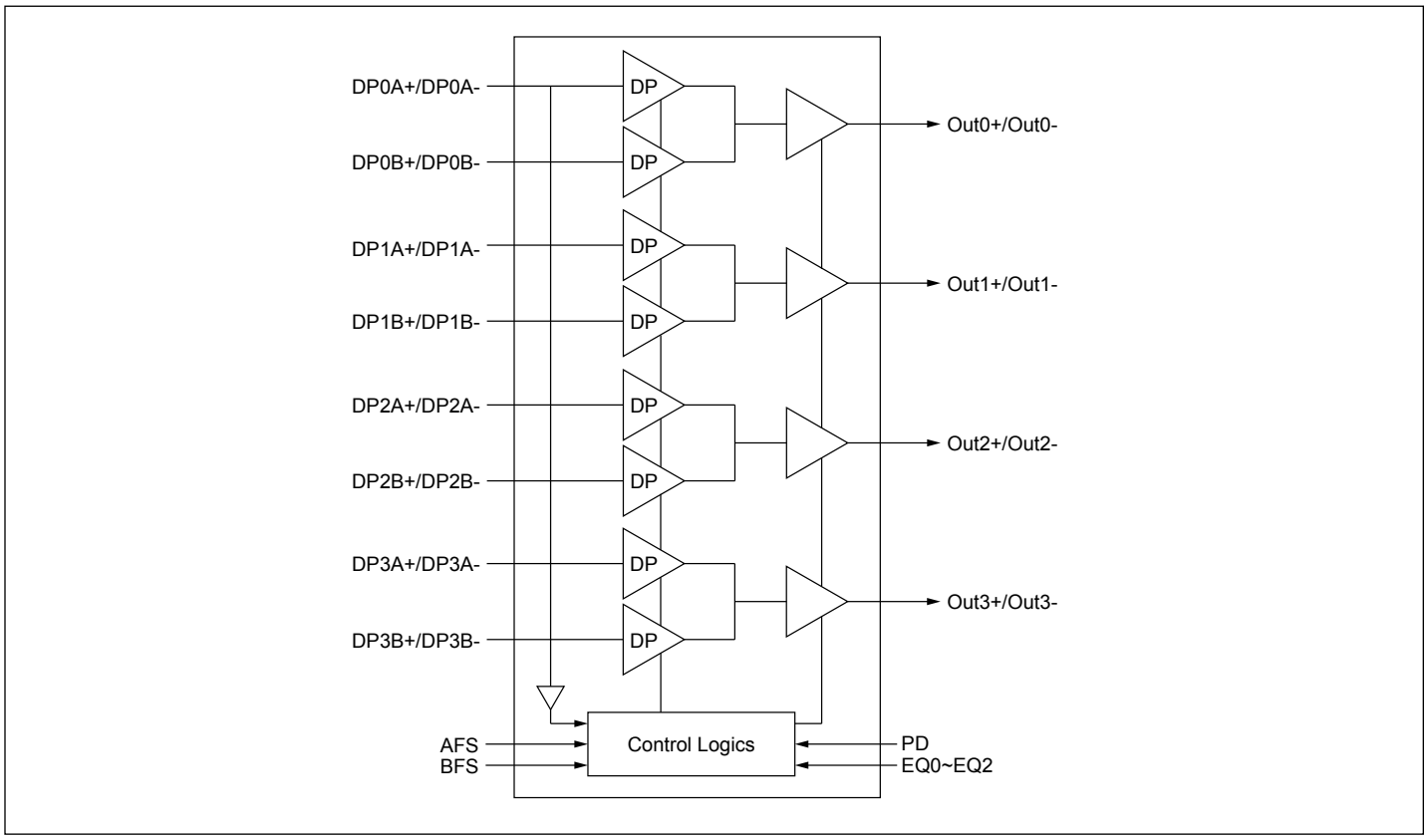
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

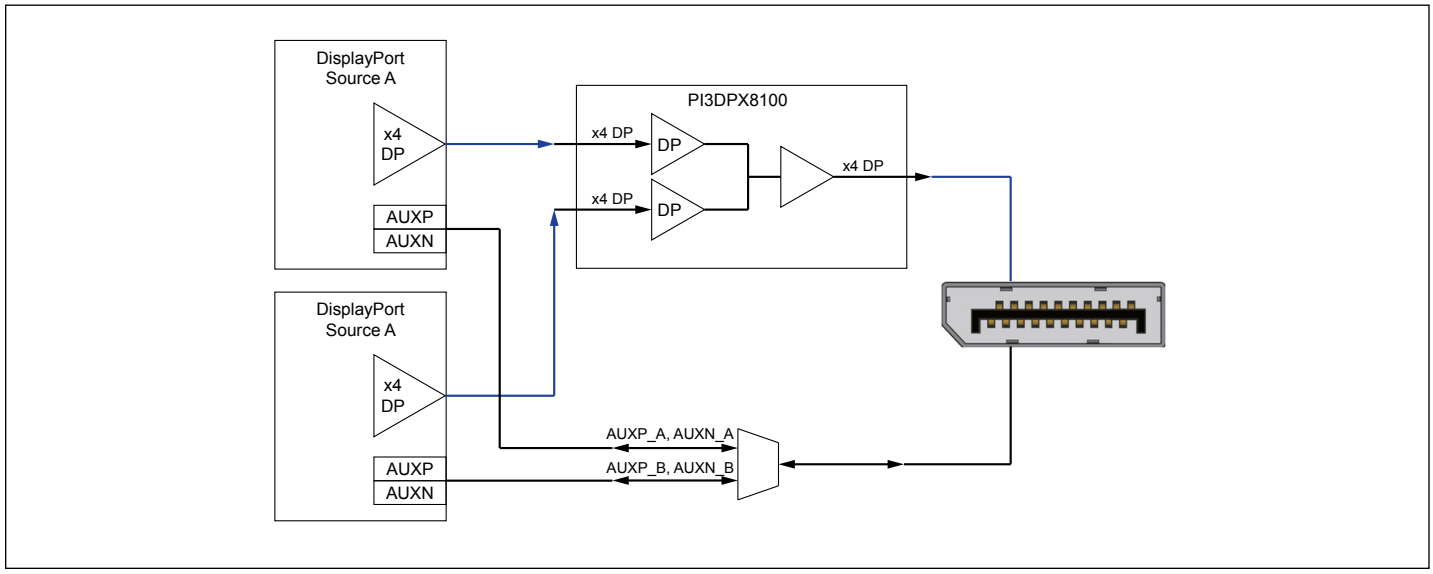
Revision History

Date	Revision	Description
May 2020	1	Datasheet

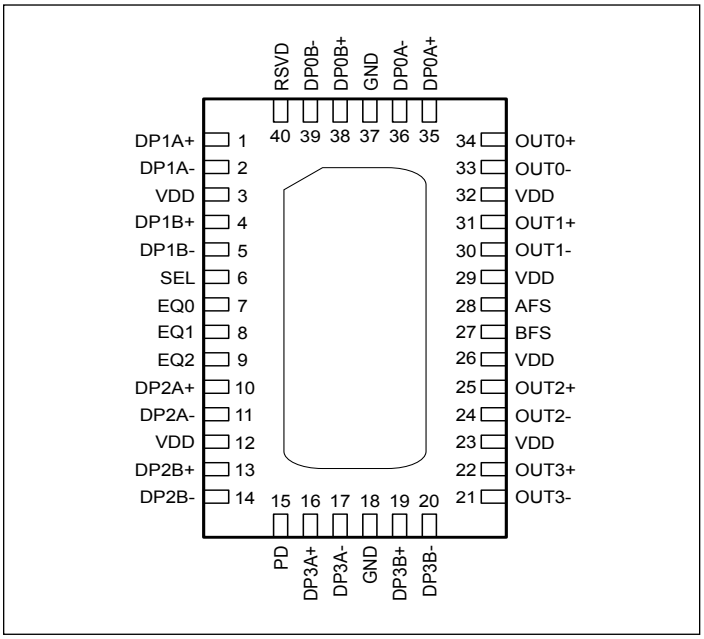
Block Diagram



System Application



Pin Configuration (Top-Side View)



Pin Description

Pin #	Pin Name	Type	Description
Power and GND			
3, 12, 23, 26, 29, 32	VDD	Power	3.3V power supply, +/-10%
18, 37, Center Pad	GND	Ground	Supply Ground
Control Pins			
15	PD	Input	Power down pin with internal 300K pull-up resistor pin. Power down control input or connector plug-in detection input for power saving operation. Default active state.
28, 27	AFS, BFS	Input	Port A and Port B, flat gain and output swing linearity selection.
7, 8, 9	EQ0, EQ1, EQ2	Input	Quad level logic input pints with internal 100K pull-up and 200K pull-down resistor. Equalization gain value selection for Port A or Port B.
6	SEL	Input	Port A or Port B selection with internal 300K pull-up resistor. Default selection is on Port A.
40	RSVD	Input (Ground)	Reserved pin. Must tie to Ground.
High Speed I/O Pins			
35, 36 1, 2 10, 11 16, 17	DP0A+, DP0A- DP1A+, DP1A- DP2A+, DP2A- DP3A+, DP3A-	Input	DisplayPort Port A input pins with internal 50-ohm to VDD or 78K-ohm to internal bias.

Pin Description Cont.

Pin #	Pin Name	Type	Description
38, 39 4, 5 13, 14 19, 20	DP0B+, DP0B- DP1B+, DP1B- DP2B+, DP2B- DP3B+, DP3B-	Input	DisplayPort Port B input pins with internal 50-ohm to VDD or 78K-ohm to internal bias.
34, 33 31, 30 25, 24 22, 21	Out0+, Out0- Out1+, Out1- Out2+, Out2- Out3+, Out3-	Output	DisplayPort Port output pins with internal 50-ohm pull up, 4K-ohm to internal bias or HIZ.

CTLE Equalization, Flat Gain, Output Linearity Selections

Equalization value selection of Port A (dB)					
EQ0	**EQ1**	**Logic state**	**@ 1.35GHz**	**@ 2.7GHz**	**@ 4.05GHz**
0	0/R	000	0.2	1.0	2.3
0	F/1	001	0.2	1.1	2.6
R	0/R	010	1.8	2.7	3.9
R	F/1	011	2.1	3.3	4.8
F	0/R	100	3.0	4.2	5.8
F	F/1	101	3.2	4.6	6.5
1	0/R	110	4.3	5.8	7.8
1	F/1	111	4.5	6.5	8.8

Equalization value selection of Port B (dB)					
EQ2	**EQ1**	**Logic state**	**@ 1.35GHz**	**@ 2.7GHz**	**@ 4.05GHz**
0	0/F	000	0.2	1.0	2.3
0	R/1	001	0.2	1.1	2.6
R	0/F	010	1.8	2.7	3.9
R	R/1	011	2.1	3.3	4.8
F	0/F	100	3.0	4.2	5.8
F	R/1	101	3.2	4.6	6.5
1	0/F	110	4.3	5.8	7.8
1	R/1	111	4.5	6.5	8.8

Note: F: Floating, R: External resistor to ground

Flat Gain and Output Swing Linearity Selections:

AFS or BFS	Flat Gain (dB)	Output Swing Linearity Range Selection (mVp-p)
0	-3.5	1000
R	-0.5	1000
F	-3.5	1200
1	-0.5	1200

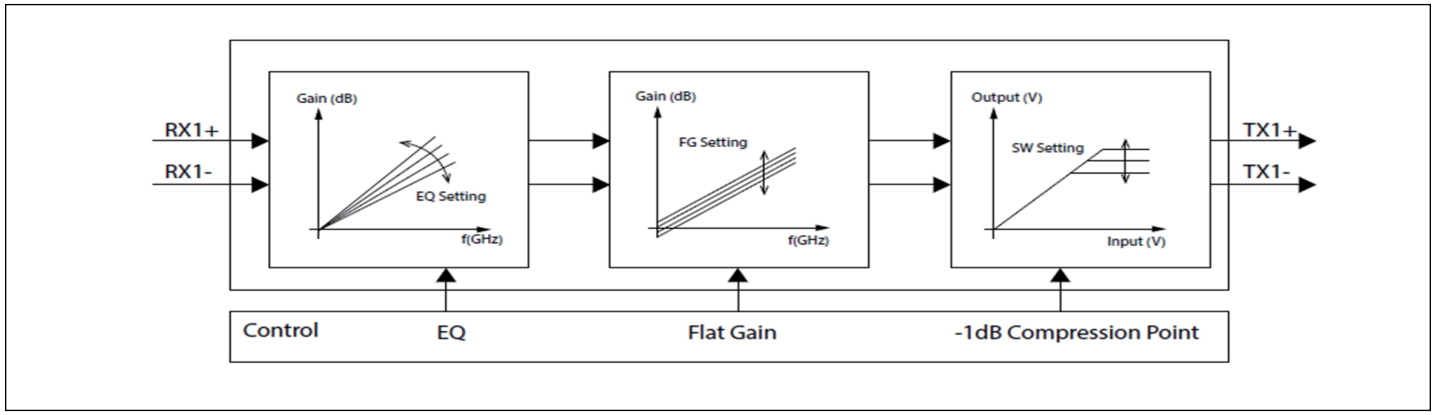


Figure 1. Illustration of EQ gain, Flat Gain and Output swing linearity (-1dB compression point) setting

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . +125°C
Supply Voltage to Ground Potential . . . . . –0.5V to +3.8V
Voltage Input to High Speed Differential Pins . . . . . –0.5V to +3.8V
Voltage Input to Control pins
(SEL, PD, AFS, BFS, RXDET, EQ0, EQ1, EQ2) . . . . . –0.5V to +3.8V
Power Dissipation Continuous 1.2W
ESD, HBM . . . . . –2kV to +2kV
ESD CDM . . . . . –500V to +500V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Thermal Information

Symbol	Parameter	40-pin TQFN (ZLD) package	Units
Theta JA	Junction to ambient thermal resistance	46.18	°C/W

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage	2.97	3.3	3.63	V
T_A	Ambient Temperature	0	-	+70	°C

AC/DC Characteristics:

LVCMOS I/O DC Specifications (VDD = 3.3 ± 0.3V, T_A = 0 to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
2-level Control Pins (PD, SEL)					
V_{IH}	DC Input logic high	$0.44V_{CC}$		V_{CC} + 0.3	V
V_{IL}	DC Input logic low	-0.3		$0.1V_{CC}$	V
V_{OH}	At I_{OH} = -200µA	V_{CC} - 0.2			V
V_{OL}	At I_{OL} = 200µA			0.2	V
4-level Logic Control Pins (EQ0, EQ1, EQ2, EQ1, AFS, BFS)					
V_{IH}	Input logic “High”	$0.92*V_{DD}$	V_{DD}		V
V_{IF}	Input logic “Float”	$0.59*V_{DD}$	$0.67*V_{DD}$	$0.75*V_{DD}$	V
V_{IR}	Input logic “With Rext to GND”	$0.25*V_{DD}$	$0.33*V_{DD}$	$0.41*V_{DD}$	V
V_{IL}	Input logic “Low”		GND	$0.08*V_{DD}$	V
I_{IH}	Input high current			50	uA
I_{IL}	Input Low current	-50			uA
Rext	External resistance connects to GND (+/-5%)	64.6	68	71.4	kOhm

High speed I/O AC/DC Specifications (V_{DD} = 3.3 ± 0.3V, T_A = 0 to 70°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{RX}	RX AC system coupling capacitance in front of high speed input pins			220		nF
P_{max}	Max Supply power	PD=0; AFS or BFS=1; FG=-0.5dB; Output swing linearity setting=1200mV			1.1	W
I_{max}	Max Supply current	PD=0; AFS or BFS=1; FG=-0.5dB; Output swing linearity setting=1200mV			305	mA
P_{idle}	Supply power	PD=1			3.6	mW
t_{pd}	Latency	From input to output			0.5	ns
R_{IN}	DC single-ended input impedance			50		Ω
	DC Differential Input Impedance			100		
R_{OUT}	DC single-ended output impedance			50	60	Ω
	DC Differential output Impedance			100	120	
Z_{RX-HIZ}	DC input CM input impedance during reset or power down			78		kΩ
$Z_{RX-DIFF-PP}$	Differential Input Peak-to-peak Voltage	Operational			1.2	Vppd
	Input source common-mode noise	DC – 200MHz			150	mVppd
V_{th+}	On threshold of signal detector	Signal swing @ 100MHz		66		mVppd
V_{th-}	Off threshold of signal detector	Signal swing @ 100MHz		64		mVppd
S11	Input return loss	10MHz to 4.05GHz differential		-17		dB
		1GHz to 4.05GHz common mode		-12		
S22	Output return loss	10MHz to 4.05GHz differential		-16		dB
		1GHz to 4.05GHz common mode		-10		
G_P	Peaking gain (Compensation at 4.05GHz, relative to 100MHz, 100mVp-p sine wave input)	EQ<2:0> = 111 EQ<2:0> = 000		7.6 3.5		
		Variation around typical	-3		+3	
G_F	Flat gain (100MHz)	AFS/BFS = R/1 AFS/BFS = 0/F		-0.5 -3.5		dB
		Variation around typical	-3		+3	dB
V_{1dB_100M}	-1dB compression point of output swing (at 100MHz)	AFS/BFS= 0 or R, EQ<2:0> = 111 AFS/BFS= F or 1, EQ<2:0> = 111		1200 1300		mVppd
V_{1dB_4G}	-1dB compression point of output swing (at 4.05GHz)	AFS/BFS= 0 or R, EQ<2:0> = 111 AFS/BFS= F or 1, EQ<2:0> = 111		1000 1100		mVppd

High Speed I/O AC/DC Specifications Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
NEXT	Near-end crosstalk at 4.05GHz	AFS/BFS = 1, EQ<2:0> = 111. Figure 2		-55		dB
FEXT	Far-end crosstalk at 4.05GHz	AFS/BFS = 1, EQ<2:0> = 111. Figure 3		-33		dB
V_{Coup}	Channel isolation	100MHz to 4.05GHz at EQ=000. Figure 4		-34		dB
V_{Noise_output}	Output idle noise with no input	100MHz to 4.05GHz, AFS/BFS = 1, EQ<2:0> = 000, Figure 5		0.6		mVRMS
		100MHz to 4.05GHz, AFS/BFS = 1, EQ<2:0> = 111, Figure 5		0.7		
DisplayPort Electrical Specification						
V_{TX-C}	Common-Mode Voltage	$\lvert V_{TX-D+} + V_{TX-D-} \rvert /2$	V_{DD}-1V		V_{DD}	V
$V_{TX-AC-CM\_HBR\_RBR}$	TX AC common mode voltage for HRB and RBR.	Measured using an 8b/10b pattern with 50% transition density			20	mVrms
$V_{TX-AC-CM\_HBR2}$	TX AC common mode voltage for HBR2				30	mVrms
$V_{TX-DIFFp-p-Level0}$	Differential peak-to-peak output voltage swing Level 0	Tested with Pre-emphasis at Level 0= 0dB Level 1= 3.5dB Level 2= 6.0 dB	0.34	0.4	0.46	V
$V_{TX-DIFFp-p-Level1}$	Differential peak-to-peak output voltage swing Level 1		0.51	0.6	0.68	V
$V_{TX-DIFFp-p-Level2}$	Differential peak-to-peak output voltage swing Level 2		0.69	0.8	0.92	V
Tj_Tx Differential Noise Budget	HBR3 (8.1Gbps)	PRBS7 test pattern. Measurement from CTS.		0.32		UI
	HBR2 (5.4Gbps)			0.30		UI
	HBR (2.7Gbps)			0.12		UI
	RBR (1.62Gbps)			0.11		UI

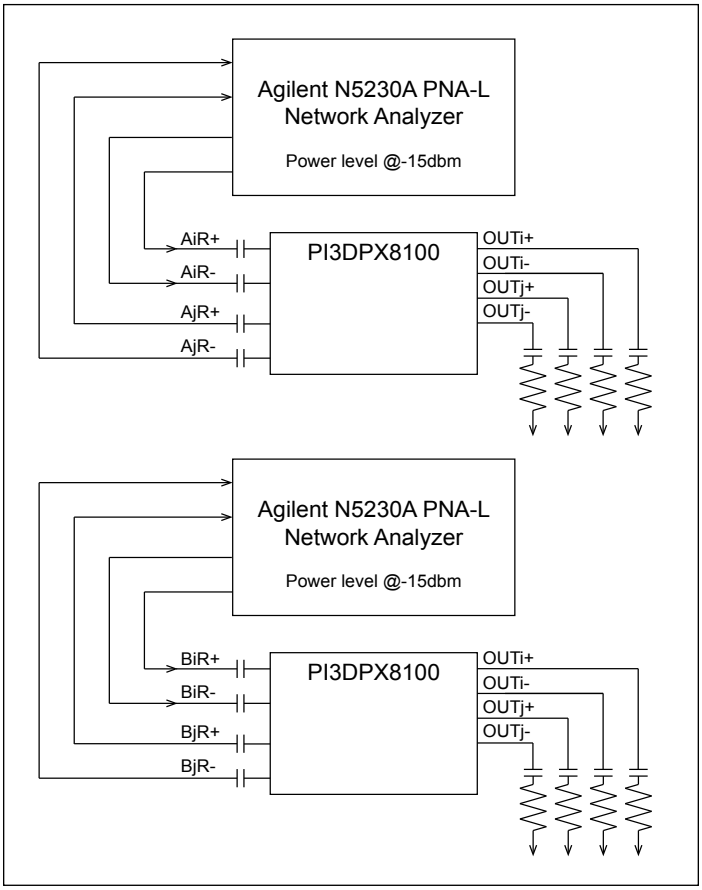


Figure 2. NEXT Test Configuration

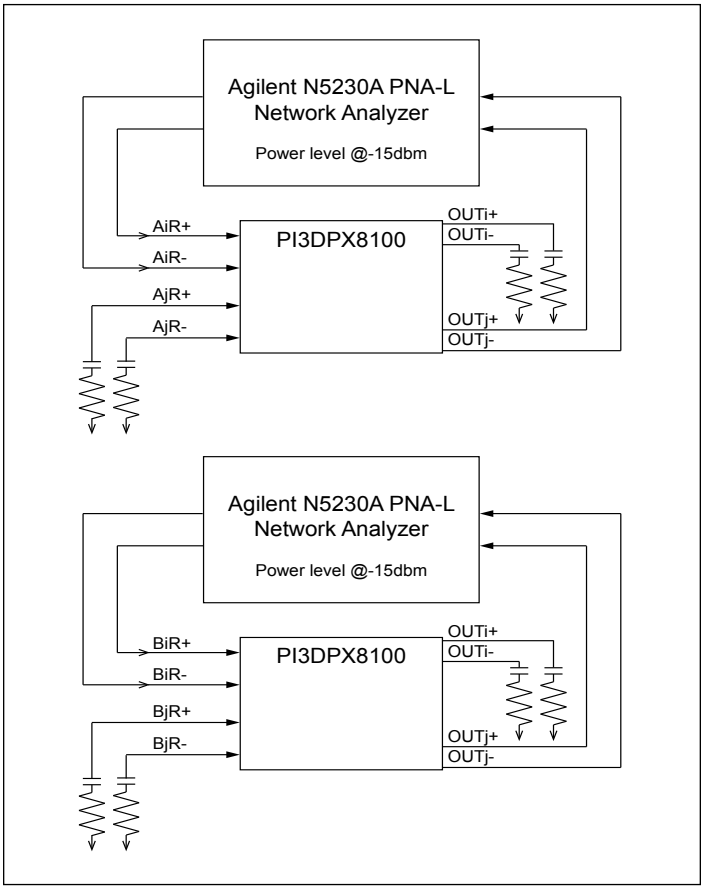


Figure 3. FEXT Test Configuration

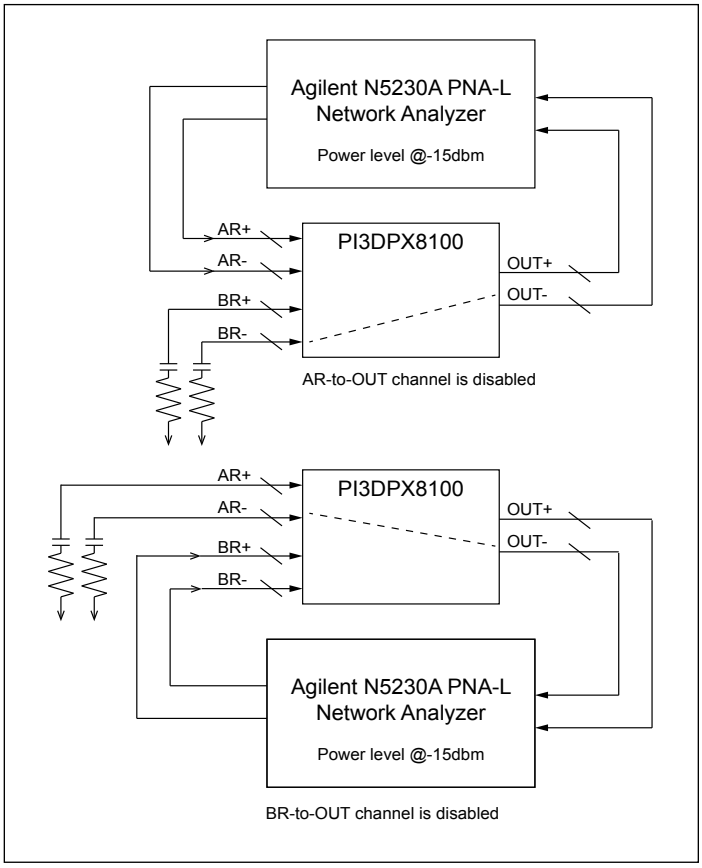


Figure 4. Input-to-Output Channel Isolation

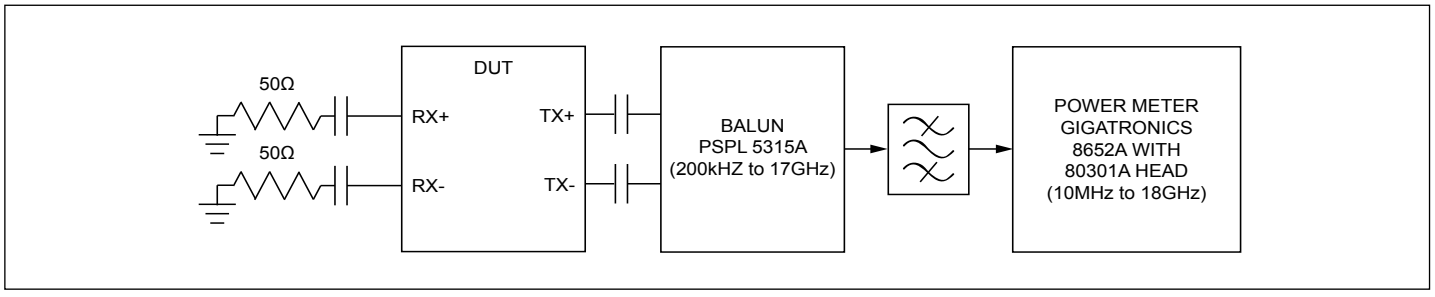


Figure 5. Idle Noise Test Configuration

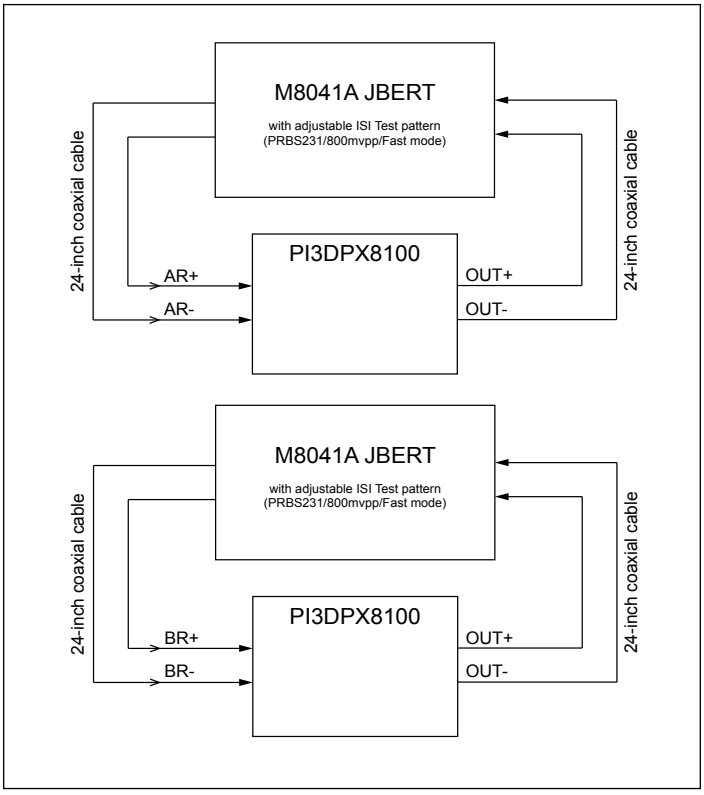
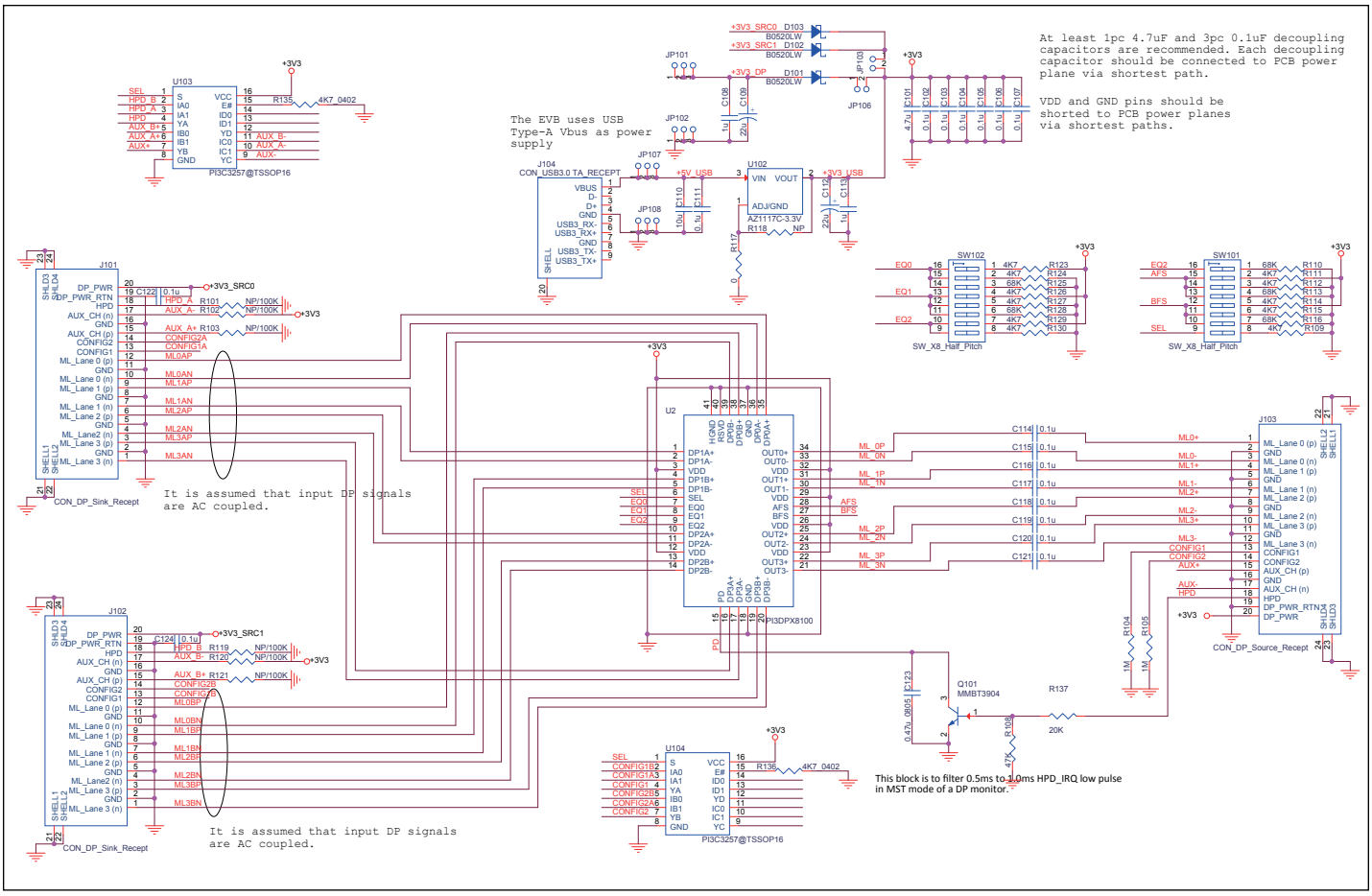


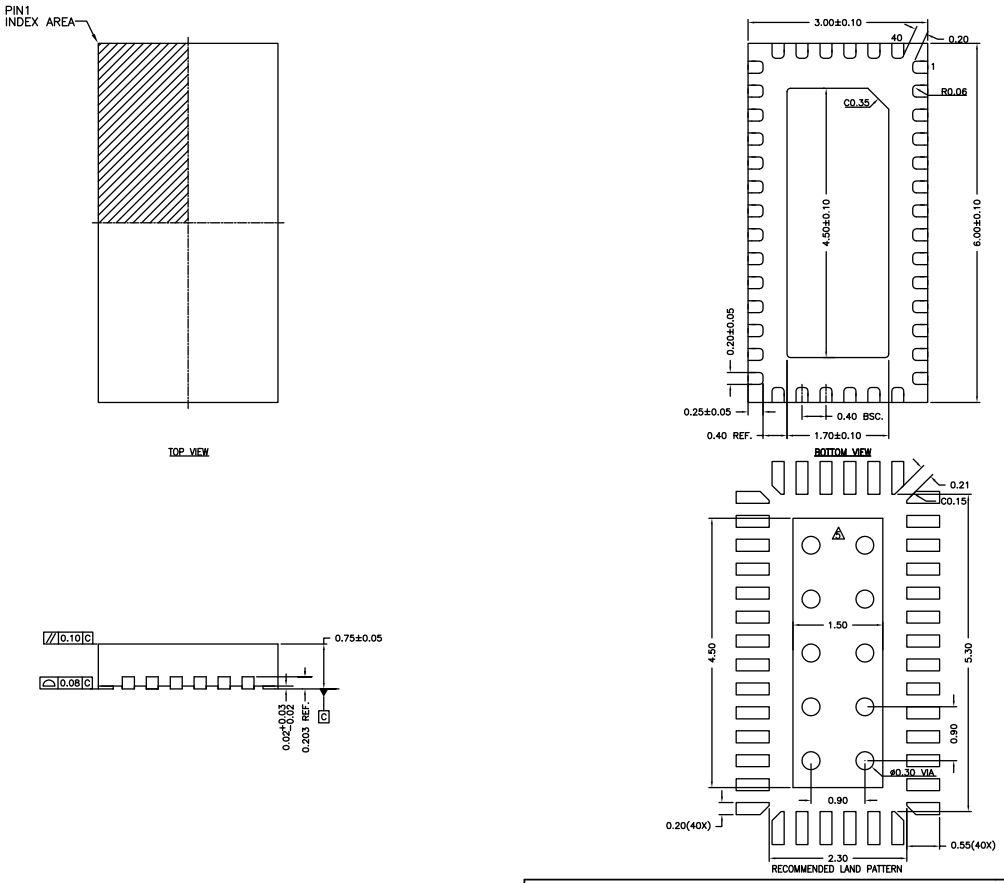
Figure 6. Tr, Tf, Rj, Dj and Tj test configuration (with -10dB added insertion loss on JBERT)

Application Diagram



Packaging Mechanical:

40-TQFN (ZLD)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)

DATE: 08/14/18

DESCRIPTION: 40-PIn, TQFN 3X6mm

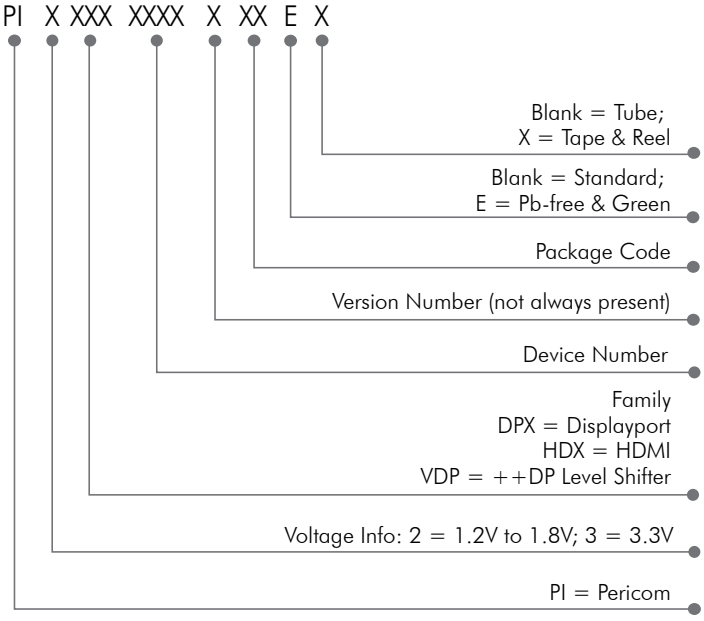
PACKAGE CODE: ZLD (ZLD40)

DOCUMENT CONTROL #: PD-2239 REVISION: --

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Part Marking Information



Part Marking

PI3DPX
8100ZLDE
YYWWXX

PI: Pericom
3DPX: 3.3v DisplayPort Product Family
8100: Part Number
ZLD: Package Code
E: Pb-Free and Green
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Plastic IC Package Information

Tape & Reel										
PKG. CODE	PKG. TYPE	REEL DIAMETER (inch)	TAPE WIDTH (mm)	TAPE PITCH (mm)	PIN 1 LOCATION	TAPE TRAILER LENGTH (Min# Pockets)	QTY PER REEL	TAPE LEADER LENGTH (Min# Pockets)	QTY PER TUBE	QTY PER TRAY
ZLD40	TQFN-40	13"	16	8	Top Left Corner	39 (12")	3500	64 (20")	N/A	490

Tape & Reel Materials and Design

Carrier Tape

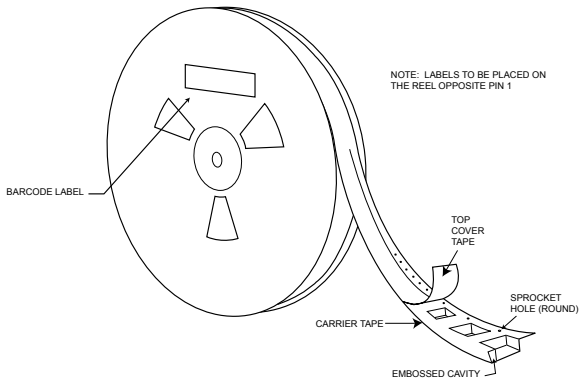
The Pocketed Carrier Tape is made of Conductive Polystyrene plus Carbon material (or equivalent). The surface resistivity is 106Ohm/sq. maximum. Pocket tapes are designed so that the component remains in position for automatic handling after cover tape is removed. Each pocket has a hole in the center for automated sensing if the pocket is occupied or not, thus facilitating device removal. Sprocket holes along the edge of the center tape enable direct feeding into automated board assembly equipment. See Figures 3 and 4 for carrier tape dimensions.

Cover Tape

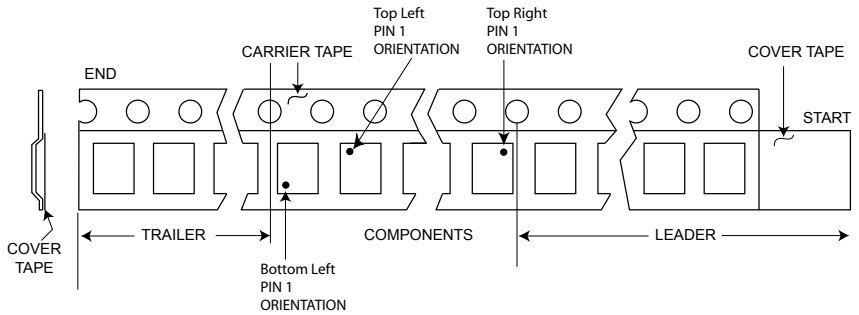
Cover tape is made of Anti-static Transparent Polyester film. The surface resistivity is 107Ohm/Sq. Minimum to 1011Ohm sq. maximum. The cover tape is heat-sealed to the edges of the carrier tape to encase the devices in the pockets. The force to peel back the cover tape from the carrier tape shall be a MEAN value of 20 to 80gm (2N to 0.8N).

Reel

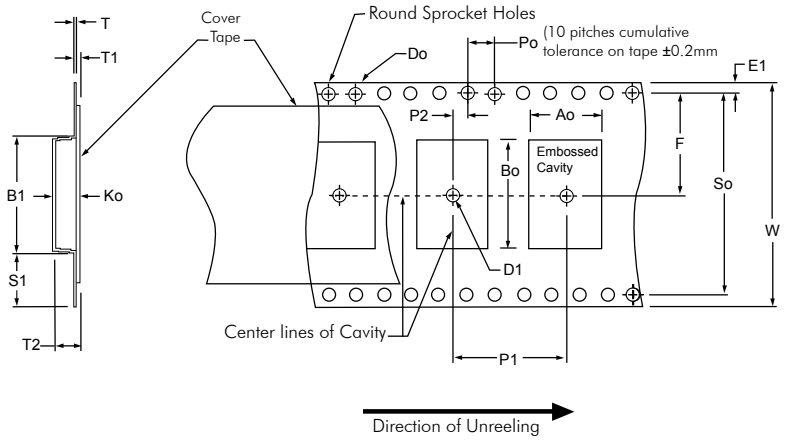
The device loading orientation is in compliance with EIA-481, current version (Figure 2). The loaded carrier tape is wound onto either a 13-inch reel, (Figure 4) or 7-inch reel. The reel is made of Antistatic High-Impact Polystyrene. The surface resistivity 107Ohm/sq. minimum to 1011Ohm/sq. max.



Tape & Reel Label Information



Tape Leader and Trailer Pin 1 Orientations



Standard Embossed Carrier Tape Dimensions

Tape & Reel Dimensions

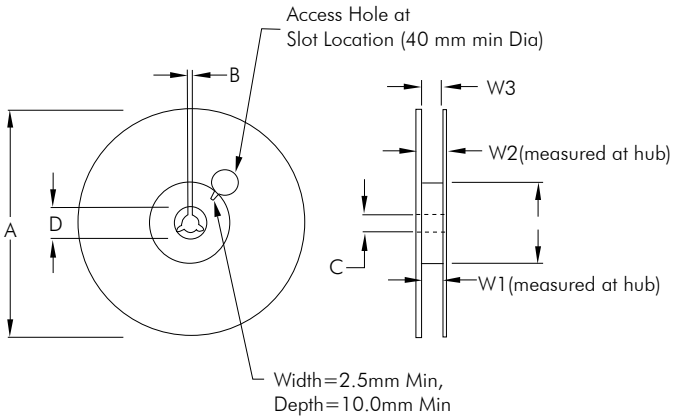
Constant Dimensions

TAPE SIZE	D_0	D_1 (Min)	E_1	P_0	P_2	R (2)	S_1 (Min)	T (Max)	T_1 (Max)
8mm	1.5 +0.1-0.0	1.0	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	25	0.6	0.6	0.1
12mm		1.5				30			
16mm					2.0 ± 0.1				
24mm									
32mm		2.0				50	N/A (3)		
44mm					2.0 ± 0.15				

Variable Dimensions

TAPE SIZE	P_1	B_1 (Max)	E_2 (Min)	F	So	T_2 (Max)	W (Max)	A_0, B_0 &K_0
8mm	Specific per package type. Refer to FR-0221 (Tape and Reel Packing Information) or visit www.diodes.com/assets/MediaList-Attachments/Diodes-Tape-Reel-Tube.pdf	4.35	6.25	3.5 ± 0.05	N/A (4)	2.5	8.3	See Note 1
12mm		8.2	10.25	5.5 ± 0.05		6.5	12.3	
16mm		12.1	14.25	7.5 ± 0.1		8.0	16.3	
24mm		20.1	22.25	11.5 ± 0.1		12.0	24.3	
32mm		23.0	N/A	14.2 ± 0.1	28.4 ± 0.1		32.3	
44mm		35.0	N/A	20.2 ± 0.15	40.4 ± 0.1	16.0	44.3	

NOTES:
1. A_0, B_0, and K_0 are determined by component size. The cavity must restrict lateral movement of component to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16,24,32, and 44mm wide carrier. The maximum component rotation within the cavity must be limited to 20o maximum for 8 and 12 mm carrier tapes and 10o maximum for 16 through 44mm.
2. Tape and components will pass around reel with radius "R" without damage.
3. S_1 does not apply to carrier width ≥32mm because carrier has sprocket holes on both sides of carrier where $D_o \geq S_1$.
4. S_o does not exist for carrier ≤32mm because carrier does not have sprocket hole on both side of carrier.



Reel Dimensions By Tape Size

TAPE SIZE	A	N (Min) (1)	W_1	W_2 (Max)	W_3	B (Min)	C	D (Min)
8mm	178 ± 2.0mm or 330 ± 2.0mm	60 ± 2.0mm or 100 ± 2.0mm	8.4 +1.5/-0.0 mm	14.4 mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
12mm			12.4 +2.0/-0.0 mm	18.4 mm				
16mm	330 ± 2.0mm	100 ± 2.0mm	16.4 +2.0/-0.0 mm	22.4 mm				
24mm			24.4 +2.0/-0.0 mm	30.4 mm				
32mm			32.4 +2.0/-0.0 mm	38.4 mm				
44mm			44.4 +2.0/-0.0 mm	50.4 mm				

NOTE:
1. If reel diameter A=178 ±2.0mm, then the corresponding hub diameter (N(min) will by 60 ±2.0mm. If reel diameter A=330±2.0mm, then the corresponding hub diameter (N(min)) will by 100±2.0mm.

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

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