PART OBSOLETE - USE PI3HDX1204E

PI3HDX1204D

HDMI 2.0 6Gbps Linear ReDriver

Features

- Support HDMI 2.0 Serial Link per each channels
- Dual-mode Displayport to HDMI 2.0 level shifter support
- 1Gbps up to 8Gbps linear equalizer
- Increases high-frequency signal level to help Receiver DFE achieve low BER
- Very Low Additive Jitter: 6ps @ 6Gb/s
- Transparent to DDC Source-side to Sink-side device communication
- Per Channel selectable adjustment of receiver equalization, output swing and flat gain
- Flexible ReDriver location; Source, Sink and Active Cable
- Pin mode or I2C selectable device programming
- I2C Master or slave selection
- Each channel polarity or channel order swap
- 4-bit selectable address for I^2C
- Power Supply voltage: 3.3V
- Package (Pb-Free & Green): 42-pin TQFN, 32-pin TQFN

General Description

Pericom Semiconductor's PI3HDX1204D linear redriver is suitable for HDMI 2.0 Redriver and Dual mode Displayport level shifter application.

The linear redriver offers unique advantage of the flexible placement between the source and sink-side devices. The linearity enables redriver to place at any location of the signal transmission trace such as on the Source or Sink-side PCB trace, inside of the Active cable. Pericom linear redriver technology provide 2 times better RJ and DJ jitter performance (Additive RJ = 0.23 ps $_{RMS}$, Additive DJ = 6.5 ps)

Linear redriver allows DDC channel to connect directly between Source and Sink device. This end-to-end sideband channel connection natively eliminates the potential interrupt compatibility issues caused by the EDID configuration registers exchange. Also it does not require special detection program handling for the Active cable application like Adaptor ID bits.

PI3HDX1204D extends 4 channels 100Ω DC or AC differential signals across the other distant data pathways on the user's platform.

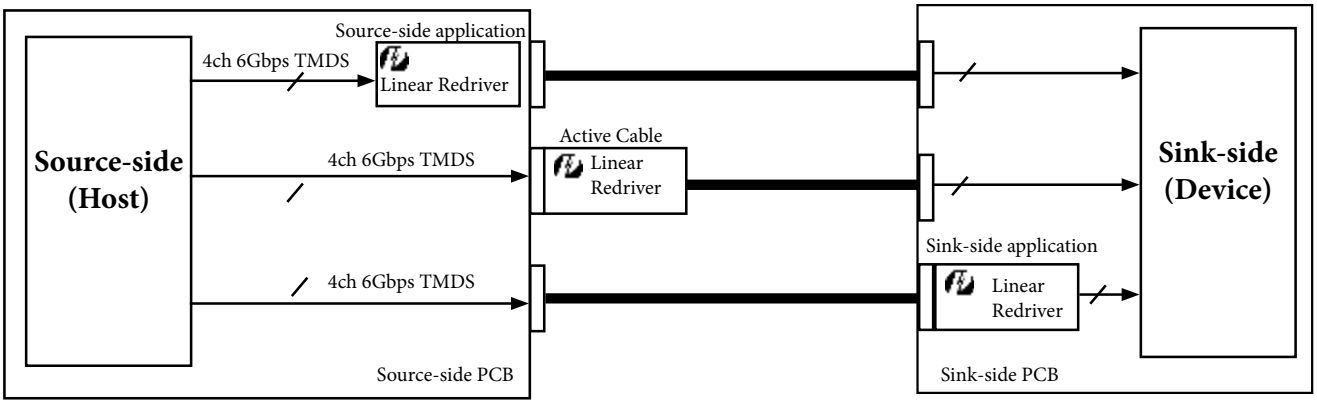
Applications

- PC, AV Receiver, Set Top Box, Video Players
- TV, Display Monitors, Active Cables

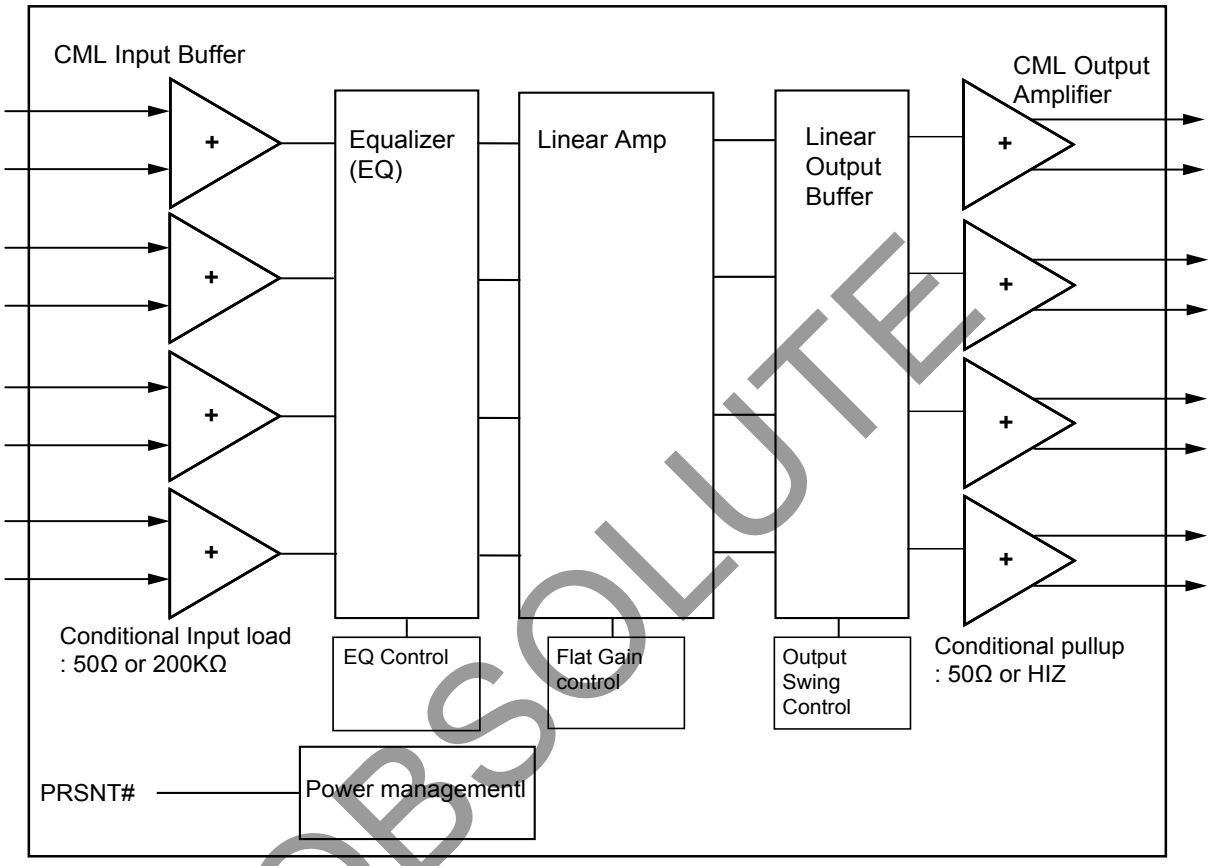
Ordering Information

Part Number	Package Description
PI3HDX1204DZHEX	42-TQFN (3.5x9mm), Pb-free, Tape/Reel, Package code: ZH 42
PI3HDX1204DZLEX	32-pin TQFN(3x6mm), Pb-free, Tape/Reel, Package code:ZL 42

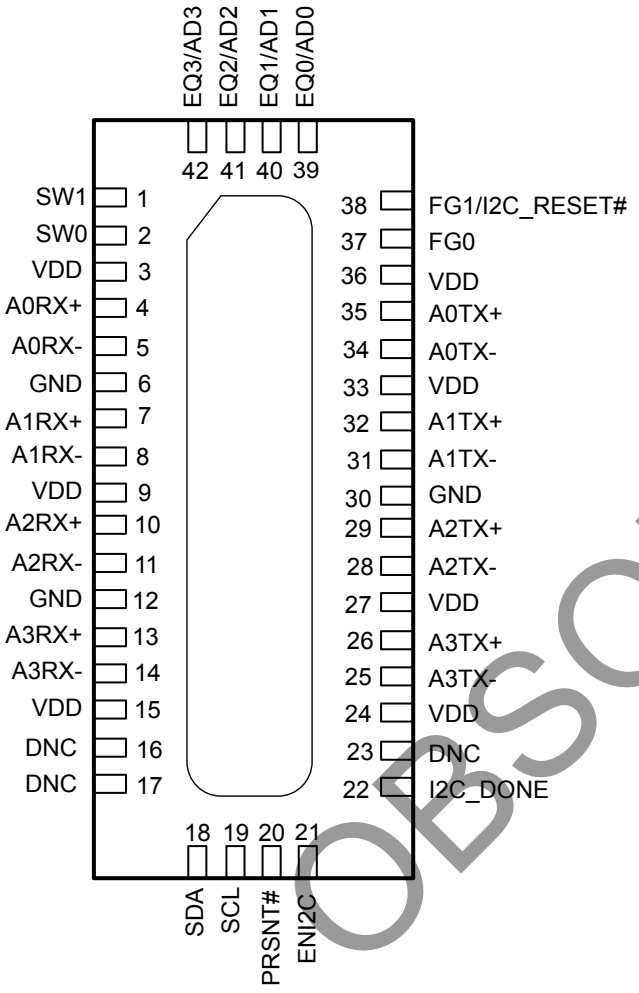
Typical Application Block Diagram



Block Diagram



Pin Configuration (42-pin TQFN)



Note: In TMDS Data and Clock Differential Pairs of Input and Output, the polarity (+/- or P/N) of each pairs and data A0, A1, A2, A3 channels can use interchangeably. Output pins of polarity and data channel will always follow the input polarity and data channel changes.

As following are examples for Source and Sink-side application.

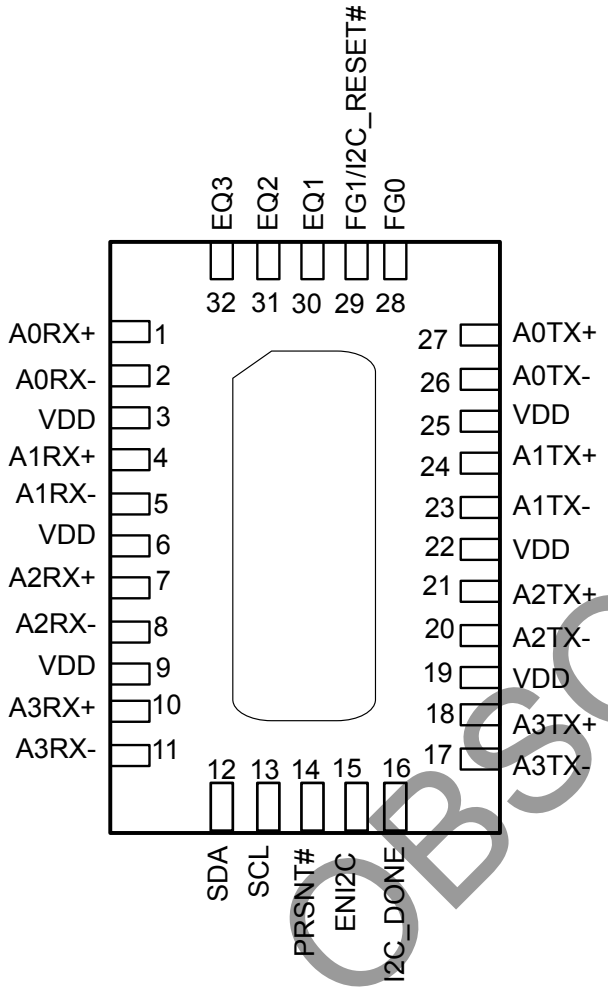
1) Source-side polarity +/- swap per each channel from **AxRx+/-:AxTx+/-** to **AxRX-/+:AxTx-/+.** "x" means each channel numbers 0, 1, 2, 3.

Pin#	Pin Name	Pin#	Pin Name
4	A0RX-	35	A0TX-
5	A0RX+	34	A0TX+
7	A1RX-	32	A1TX-
8	A1RX+	31	A1TX+
10	A2RX-	29	A2TX-
11	A2RX+	28	A2TX+
13	A3RX-(clk)	26	A3TX-(clk)
14	A3RX+(clk)	25	A3TX+(clk)

2) Sink-side channel order swap from **AxRX/AyRX/AzRX/ A3RX(clk): AxTX/AyTX/AzTX/A3TX(clk)** to **A3RX(clk)/ AxRX/AyRX/AzRX: A3TX(clk)/AxTX/AyTX/AzTX**.

Pin#	Pin Name	Pin#	Pin Name
4	A3RX+(clk)	35	A3TX+(clk)
5	A3RX-(clk)	34	A3TX-(clk)
7	AxRX+	32	AxTX+
8	AxRX-	31	AxTX-
10	AyRX+	29	AyTX+
11	AyRX-	28	AyTX-
13	AzRX+	26	AzTX+
14	AzRX-	25	AzTX-

Pin Configuration (32-pin TQFN)



Pin Description (42-pin TQFN)

Pin #	Pin Name	Type	Description
Data Signals			
4 5	A0RX+ A0RX-	I	TMDS inputs for Channel A0; with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
35 34	A0TX+, A0TX-	O	TMDS outputs for Channel A0; with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
7 8	A1RX+, A1RX-	I	TMDS inputs for Channel A1; with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
32 31	A1TX+, A1TX-	O	TMDS outputs for Channel A1; with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
10 11	A2RX+, A2RX-	I	TMDS inputs for Channel A2; with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
29 28	A2TX+, A2TX-	O	TMDS outputs for Channel A2; with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
13 14	A3RX+, A3RX-	I	TMDS inputs for Channel A3; with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
26 25	A3TX+, A3TX-	O	TMDS outputs for Channel A3; with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
Control Signals			
16,17	DNC		Do Not Connect
19	SCL	I/O	I^2C SCL Clock. In Master mode (ENI2C floating), SCL is an output. Otherwise it is an input.
18	SDA	I/O	I^2C SDA data input/output.
23	DNC		Do Not Connect
20	PRSNT#	I	This pin is active in both PIN mode (ENI2C=LOW) and I2C mode (ENI2C=HIGH). Cable present detect input. This pin has internal 100kΩ pull-up. When High, a cable is not present, and the device is put in lower power mode. When LOW, the device is enabled and in normal operation.
21	ENI2C	I	Enable I2C; When LOW, each channel is programmed by the external pin voltage. When HIGH, each channel is programmed by the data stored in the I^2C bus. When floating, master mode (Read External EEPROM)
39,40, 41,42	EQ[3:0]	I	EQ setting; Inputs with internal 100kΩ pull-up. This pins set the amount of Equalizer Boost in all channels, when ENI2C is LOW.
	AD[3:0]	I	I^2C programmable address bits with internal 100kΩ pull-up.
1,2	SW[1:0]	I	Swing Control; Inputs with internal 100kΩ pull-up. This pin sets the output Voltage Level in all channel when ENI2C is LOW.
38,37	FG[1:0]	I	Flat Gain Control; Inputs with internal 100kΩ pull up resistor. Sets the output flat gain level on all channels when ENI2C is low.

Pin #	Pin Name	Type	Description
38	I2C_RESET#	I	I2C reset pin; Inputs with internal 100kΩ pull up resistor. Reset pin for I^2C. When set low, reset the registers to default state.
22	I2C_DONE	O	I2C EEPROM load done pin; Valid register load status output, use for daisy chain master. • Low = External EEPROM load failed • HIGH = External EEPROM load passed
Power Pins			
3, 9, 15, 24, 27, 33, 36	VDD	PWR	3.3V Power Supply
6, 12, 30,	GND	GND	Ground
Center Pad	GND	GND	Exposed Ground pad.

Pin Description (32-pin TQFN)

Pin #	Pin Name	Type	Description
Data Signals			
1 2	A0RX+ A0RX-	I	TMDS inputs for Channel A0; with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
27 26	A0TX+, A0TX-	O	TMDS outputs for Channel A0; with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
4 5	A1RX+, A1RX-	I	TMDS inputs for Channel A1; with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
24 23	A1TX+, A1TX-	O	TMDS outputs for Channel A1; with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
7 8	A2RX+, A2RX-	I	TMDS inputs for Channel A2; with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
21 20	A2TX+, A2TX-	O	TMDS outputs for Channel A2; with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
10 11	A3RX+, A3RX-	I	TMDS inputs for Channel A3; with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.
18 17	A3TX+, A3TX-	O	TMDS outputs for Channel A3; with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.
Control Signals			
12	SDA	I/O	I^2C SDA data input/output.
13	SCL	I/O	I^2C SCL Clock; In master mode (ENI2C floating), SCL is an output. Otherwise it is an input.
14	PRSNT#	I	Cable Present Detect pin; This pin is active in both PIN mode (ENI2C=LOW) and I2C mode (ENI2C=HIGH). This pin has internal 100KΩ pull-up. When High, a cable is not present, and the device is put in lower power mode. When LOW, the device is enabled and in normal operation.
15	ENI2C	I	Enable I2C pin; When LOW, each channel is programmed by the external pin voltage. When HIGH, each channel is programmed by the data stored in the I^2C bus. When floating, master mode (Read External EEPROM)
32,31,30	EQ[3:1]	I	EQ Control pin; Inputs with internal 100kΩ pull-up. This pins set the amount of Equalizer Boost in all channel when ENI2C is LOW. Note: EQ0 tied "high", i.e. always "1" .
	AD[3:1]	I	I^2C programmable address bits with internal 100kΩ pull-up. Note: AD0 tied "high", i.e. always "1".
29	FG1/I2C_RESET#	I	Flat Gain Control [1] or I2C Reset pin; Inputs with internal 100kΩ pull up resistor. Sets the output flat gain level on all channels when ENI2C is low.
28	FG0	I	Flat Gain Control [0] pin; Inputs with internal 100kΩ pull up resistor. Reset pin for I^2C. When set low with reset the registers to default state.

Pin #	Pin Name	Type	Description
16	I2C_DONE	O	Valid register load status output, use for daisy chain master Low = External EEPROM load failed HIGH = External EEPROM load passed
Power Pins			
3,6,9, 19,22, 25	VDD	PWR	3.3V Power Supply
Center Pad	GND	GND	Exposed Ground pad.

Functional Description

Power Enable function:
One pin control or I2C control, when PRSNT# is set to HIGH, the IC goes into power down mode, both input and output termination set to 200kΩ and High impedance respectively. Individual Channel Enabling is done through the I2C register programming.

Equalization Setting:
EQ[3:0] are the selection pins for the equalization selection for each channel.

Equalization Setting

EQ3	EQ2	EQ1	EQ0	6Gbps Input EQ(dB)
0	0	0	0	3.6
0	0	0	1	4.0
0	0	1	0	4.4
0	0	1	1	4.7
0	1	0	0	5.1
0	1	0	1	5.5
0	1	1	0	5.9
0	1	1	1	6.2
1	0	0	0	6.6
1	0	0	1	6.9
1	0	1	0	7.3
1	0	1	1	7.6
1	1	0	0	8.0
1	1	0	1	8.2
1	1	1	0	8.6
1	1	1	1	8.9

Output -1 dB Compression Setting:

SW1 and SW0 affect the linearity of the output when input amplitude changes.

SW1	SW0	mVpp @100MHz	mVpp @3GHz (equ. @6Gbps)
0	0	1100	1000
0	1	1200	1100
1	0	1300	1200
1	1	1400	1300

Note: This device support input swings up to 1.4V.

Flat Gain Setting:

FG[1:0] pins are the selection bits for the DC value.

FG1	FG0	Gain
0	0	-3.5 dB
0	1	-1.5 dB
1	0	+0.5 dB
1	1	+2.5 dB

I2C Programming

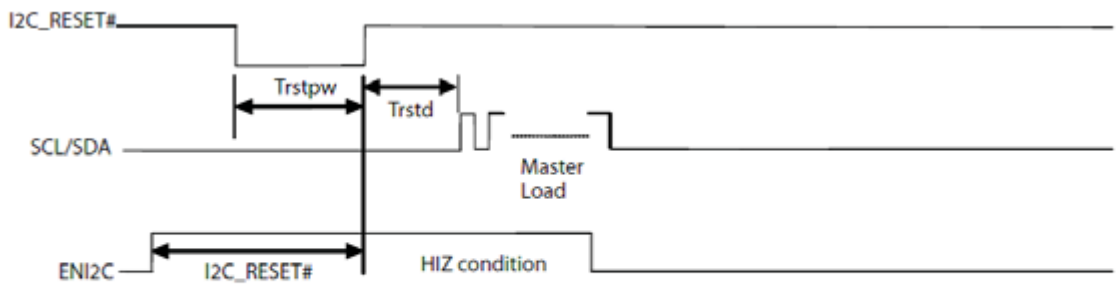
Address assignment							
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**R/W**
1	1	1	AD3	AD2	AD1	AD0	1=R, 0=W

BYTE 0					
Bit	**Type**	**Power up condition**		**Control affected**	**Comment**
7:0	R	Reserved			
BYTE 1					
Bit	**Type**	**Power up condition**		**Control affected**	**Comment**
7:0	R	Reserved			
BYTE 2					
Bit	**Type**	**Power up condition**		**Control affected**	**Comment**
7	R/W	0		A3 Power down	1 = Power down
6	R/W	0		A2 Power down	
5	R/W	0		A1 Power down	
4	R/W	0		A0 Power down	
3	R/W	0		Reserved	
2	R/W	0		Reserved	
1	R/W	0		Reserved	
0	R/W	0		Reserved	

BYTE 3					
Bit	**Type**	**Power up condition**		**Control affected**	Comment
7	R/W	0	Channel A0 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	
BYTE 4					
Bit	**Type**	**Power up condition**		**Control affected**	Comment
7	R/W	0	Channel A1 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	
BYTE 5					
Bit	**Type**	**Power up condition**		**Control affected**	Comment
7	R/W	0	Channel A2 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	

BYTE 6					
Bit	**Type**	**Power up condition**		**Control affected**	Comment
7	R/W	0	Channel A3 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	
BYTE 7					
Bit	**Type**	**Power up condition**		**Control affected**	Comment
7:0	R/W	Reserved			
BYTE 8-15 with "0" power up condition					

Reset and I2C Timing Diagram



Recommended minimum reset pulse width T_{rstpw}= 1µs
I^2C master cycle start from I2C_RESET# pulse go high, Trstd = 200µs
ENI2C = HIZ to I2C_RESET#(high) (min), Ti2cm_rst = 1 uS.

I2C Operation

The integrated I2C interface operates as a master or slave device depending on the pin ENI2C being HIZ or HIGH respectively. Standard mode (100Kbps) is supported with 7-bit addressing.
In the Slave mode (ENI2C = HIGH), the device supports Read/Write. The bytes must be accessed in sequential order from the lowest to the highest byte with the ability to stop after any complete byte has been transferred.
Address bits A3 to A0 are programmable to support multiple chips environment. The Data is loaded until a Stop sequence is issued.

Master mode (ENI2C = HIZ) supports up to 16 masters connected in daisy chain through connecting I2C_DONE pin to I2C_RESET# pin of the next part.

Master EEPROM data starting address for device address:

I2C address: AD3, AD2, AD1, AD0	Data starting location
0000	00H
0001	10H
0010	20H
0011	30H
0100	40H
0101	50H
0110	60H
0111	70H
1000	80H
1001	90H
1010	A0H
1011	B0H
1100	C0H
1101	D0H
1110	E0H
1111	F0H

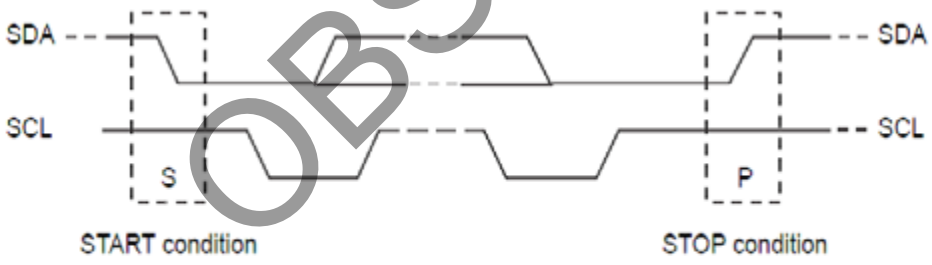
Transferring Data
Every byte put on the SDA line must be 8-bits long. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (see the I2C Data Transfer diagram). It will never hold the clock line SCL LOW to force the master into a wait state.

Acknowledge
Data transfer with acknowledge is required from the master. When the master releases the SDA line (HIGH) during the acknowledge clock pulse, it will pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse as indicated in the I^2C Data Transfer diagram. It will generate an acknowledge after each byte has been received.

Data Transfer
A data transfer cycle begins with the master issuing a start bit. After recognizing a start bit, it will watch the next byte of information for a match with its address setting. When a match is found it will respond with a read or write of data on the following clocks. Each byte must be followed by an acknowledge bit, except for the last byte of a read cycle which ends with a stop bit.

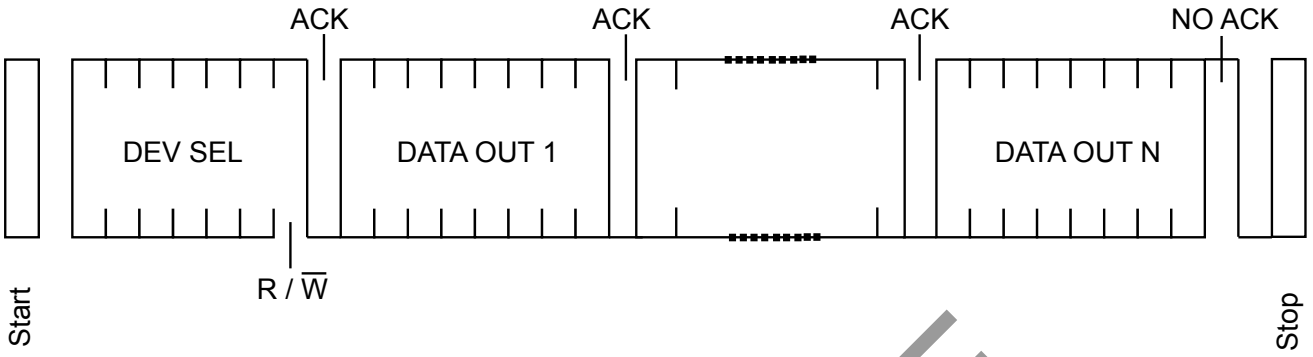
I2C Data Transfer

Start & Stop Conditions
A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition, as shown in the figure below

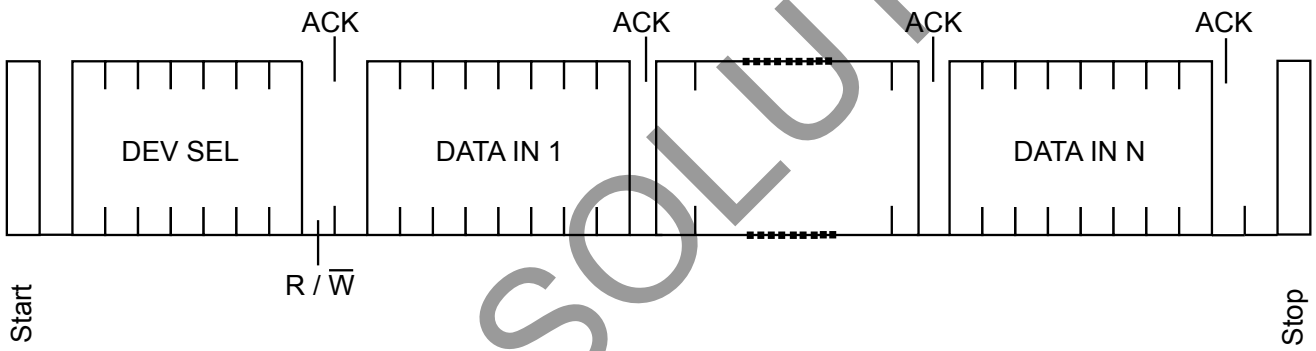


I^2C START and STOP conditions.

I2C Data Read



I2C Data Write



Absolute Maximum Ratings

Storage Temperature .....–65 °C to +150 °C
Supply Voltage to Ground Potential.....–0.5 V to +4.6 V
DC SIG Voltage ..... –0.5 V to V_{DD} + 0.5V
Current Output .....–25 mA to +25 mA
Power Dissipation Continuous.....1.63W
Operating Temperature .....0 to +70 °C
ESD, HBM ..... –2 kV to +2 kV

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical characteristics

LVCMOS I/O DC Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{IH}	DC input logic high		V_{DD}/2 + 0.7		V_{DD} + 0.3	V
V_{IL}	DC input logic low		-0.3		V_{DD}/2 - 0.7	V
V_{OH}	At I_{OH} = -200µA		V_{DD} + 0.2			V
V_{OL}	At I_{OL} = -200µA				0.2	V
V_{hys}	Hysteresis of Schmitt trigger input		0.8			V

Power Consumption

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Power supply voltage		3.0	3.3	3.6	V
IDD	Maximum supply current	PRSNT#=0		225	290	mA
IDDQ	Quiescent supply current	PRSNT#=1, TMDS Output Disable		2.0	4.2	mA

Note: "Supply current IDDmax data" on page 18.

Inputs Control Pins DC Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	DC input logic high		$V_{DD}/2 + 0.7$		$V_{DD} + 0.3$	V
V_{IL}	DC input logic low		-0.3		$V_{DD}/2 - 0.7$	V

SDA and SCL I/O Pins for I^2C-bus

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{IH}	DC input logic high		$V_{DD}/2 + 0.7$	$V_{DD} + 0.3$	V
V_{IL}	DC input logic low		-0.3	$V_{DD}/2 - 0.7$	V
V_{OL}	DC output logic low	I_{OL} = 3mA		0.4	V

TMDS Differential Pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Single-ended High Level Output Voltage	VDD = 3.3 V, Rout = 50 Ω	V_{DD}-10		V_{DD}+10	mV
V_{OL}	Single-ended Low Level Output Voltage		V_{DD}-600		V_{DD}-400	mV
V_{swing}	Output Voltage Swing		400		600	mVppd
I_{OS}	Short Circuit Current Limit (Ios)				12	mA
R_T	Input Termination Resistance	V_{IN} = 2.9V	45	50	55	Ω
I_{OZ}	Leakage Current with Hi-Z I/O	V_{DD} = 3.6V			10	uA

Switching Characteristics

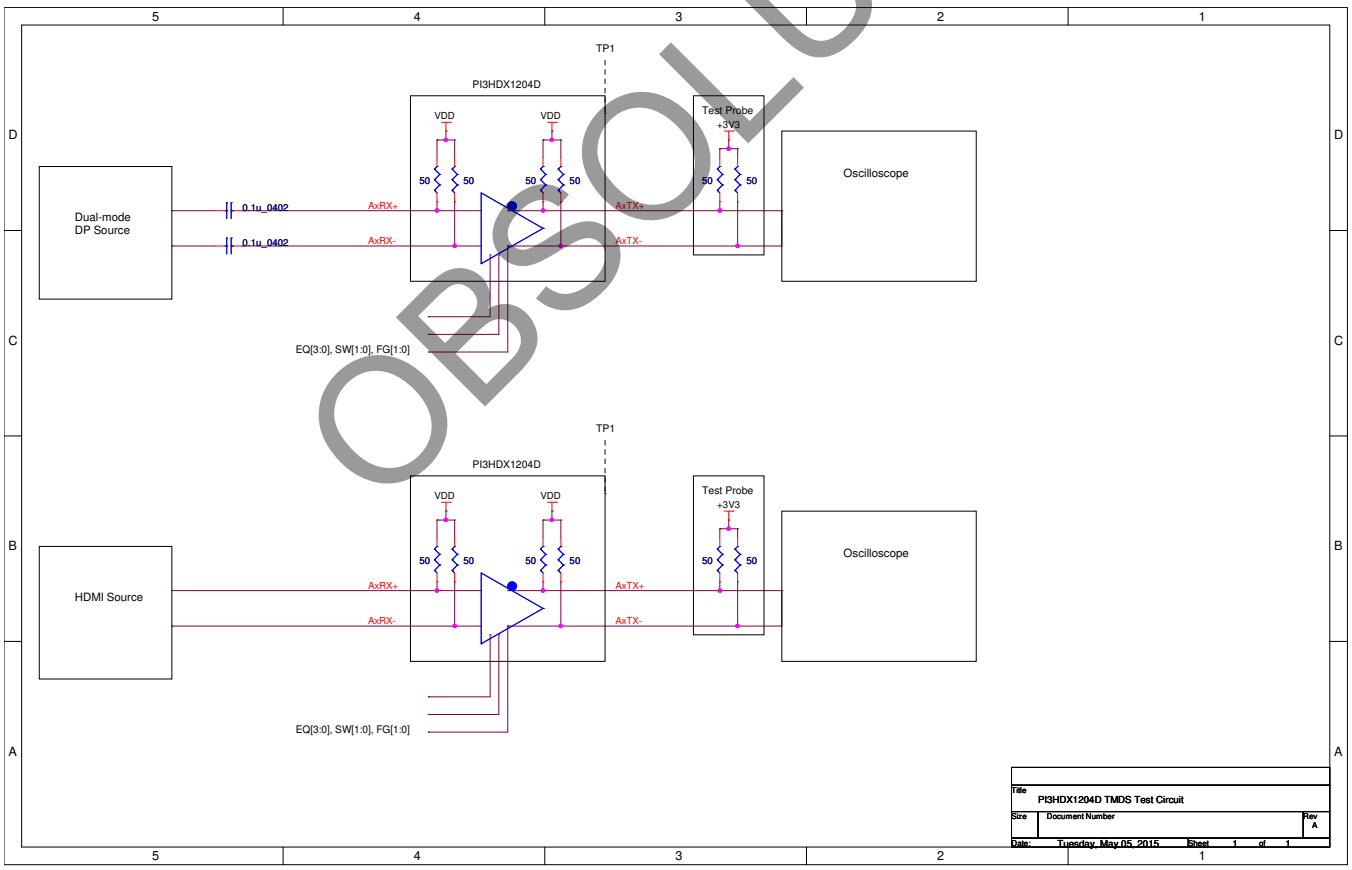
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
T_{pd}	Propagation Delay				2000	ps
$T_{sk(p)}$	Pulse Skew			10	50	ps
$T_{sk(D)}$	Intra-pair Differential Skew			23	50	ps
$T_{sk(O)}$	Inter-pair Differential Skew				100	ps
$T_{Jit\text{-}Clk}$	Peak-to-peak Output Jitter for Clock channel	Pre-/De-EMP = 0 dB Data Input = 6 Gbps HDMI Pattern, Clock input = 150 MHz		15	30	ps
$T_{Jit\text{-}Data}$	Peak-to-peak Output Jitter for Data channels			18	50	ps
t_{sx}	Select to switch Output				10	ns

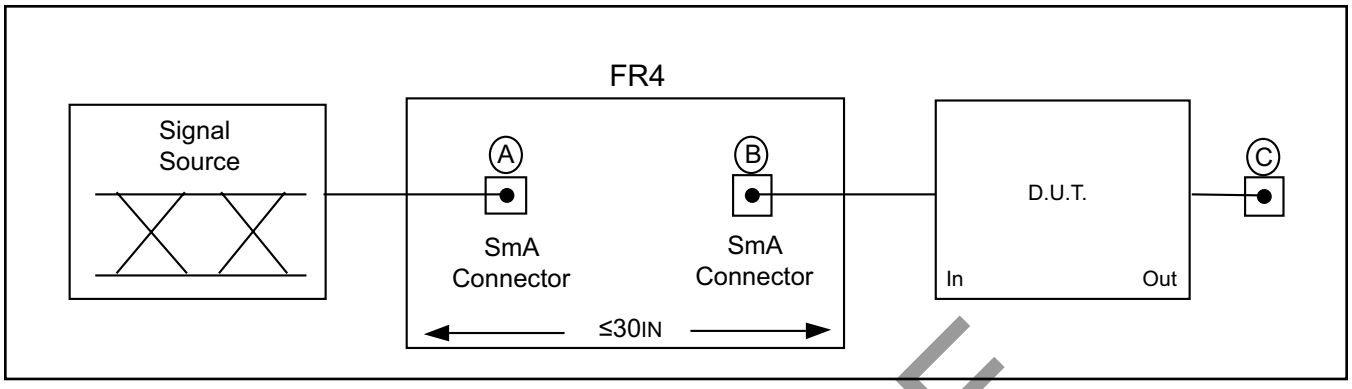
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{en}	Enable Time				200	ns
t_{dis}	Disable Time				10	ns

Add-in Jitter Information

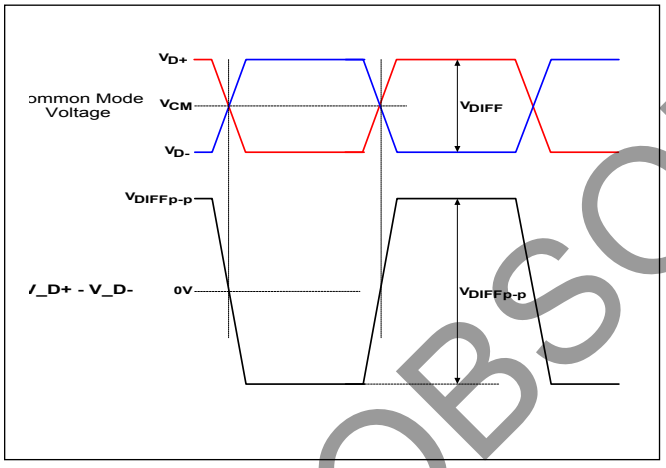
	Parameters	Input Jitter (TP1)	Output Jitter (TP2)	Add-in Jitter	Units
R_J	Random Jitter 6Gb/s	0.74	0.775	0.23	RMS ps
D_J	Deterministic Jitter	9.13	15.70	6.57	ps

HDMI and Dual-mode DisplayPort Test Circuit





AC Test Circuit Referenced in the Electrical Characteristic Table

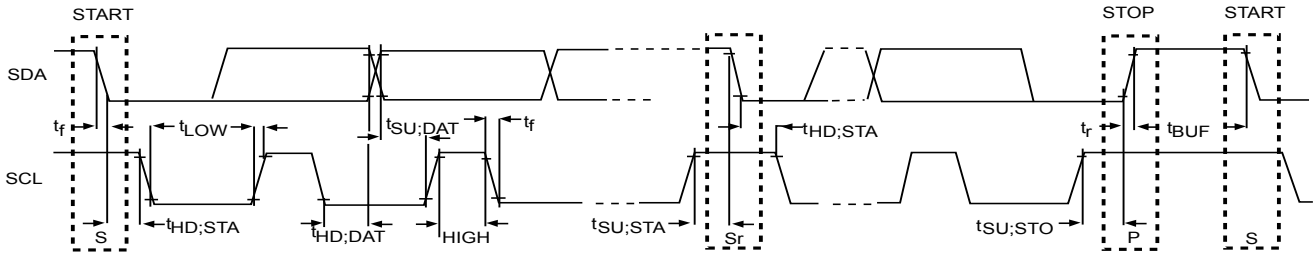


Definition of Peak-to-Peak Differential Voltage

I²C BUS SCL/SDA

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{IH}	DC input logic high		$V_{DD}/2$ + 0.7		V_{DD} + 0.3	V
V_{IL}	DC input logic low		-0.3		$V_{DD}/2$ - 0.7	V
V_{OL}	DC output logic low	I_{OL} = 3mA			0.4	V
Ipullup	Current Through Pull-Up Resistor or Current Source	High Power specification	3.0		3.6	mA
VDD	Nominal Bus Voltage		3.0		3.6	V
Ileak-bus	Input leakage per bus segment		-200		200	uA
Ileak-pin	Input leakage per device pin			-15		uA
CI	Capacitance for SDA/SCL				10	pF
Freq	Bus Operation Frequency				100k	Hz
TBUF	Bus Free Time Between Stop and Start condition		1.3			us
THD:STA	Hold time after (Repeated) Start condition. After this period, the first clock is generated.	At pull-up, Max	0.6			us
TSU:STA	Repeated start condition setup time		0.6			us
TSU:STO	Stop condition setup time		0.6			us
THD:DAT	Data hold time		0			ns
TSU:DAT	Data setup time		100			ns
Tlow	Clock low period		1.3			us
Thigh	Clock high period		0.6		50	us
tF	Clock/Data fall time				300	ns
tR	Clock/Data rise time				300	ns
tPOR	Time in which a device must be operation after power-on reset				500	ms

Note: (1) Recommended value.
(2) Recommended maximum capacitance load per bus segment is 400pF.
(3) Compliant to I2C physical layer specification.
(4) Ensured by Design. Parameter not tested in production.

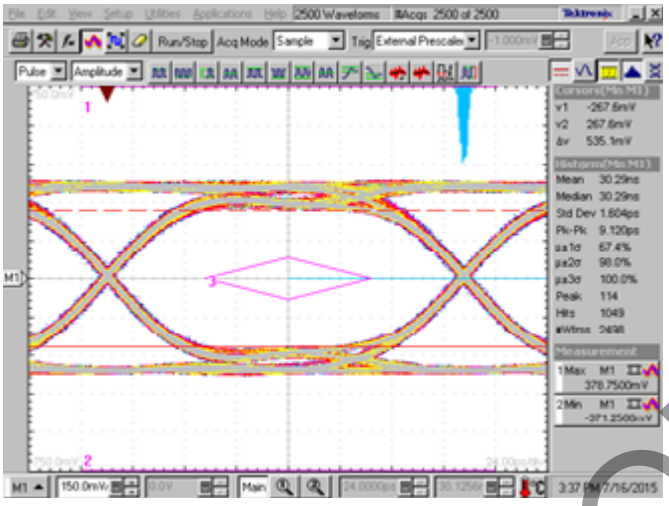


I^2C Timing

Output Eye Diagram with different Trace lengths & Input EQ settings

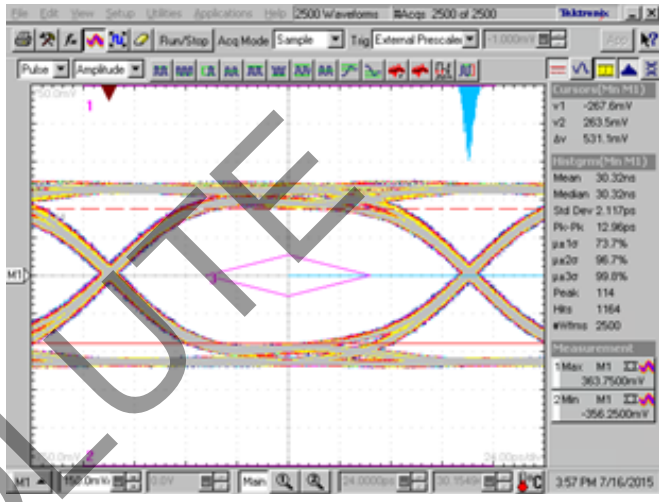
Using PRBS 2^23-1 pattern, Input Swing=800mVd, Output Swing= 1000mVdiff,

- FG = 10 (+0.5dB), EQ=4.7dB, Trace length =18-in



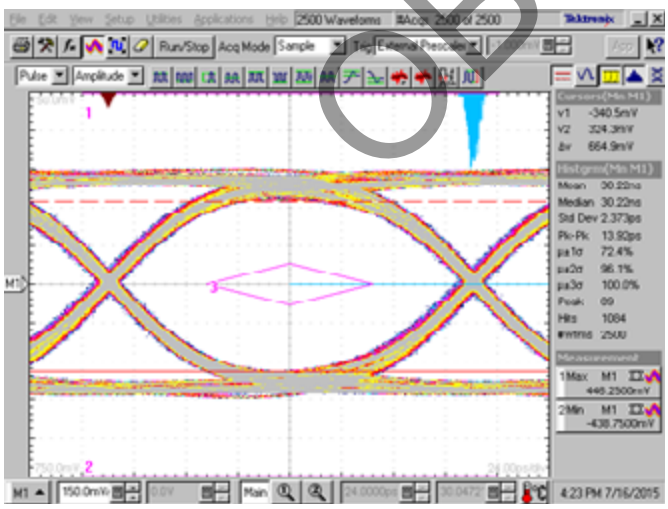
Using PRBS 2^23-1 pattern, Input Swing=800mVd, Output Swing= 1000mVdiff,

- FG =11 (+0.5dB), EQ=6.2dB, Trace length = 24-in



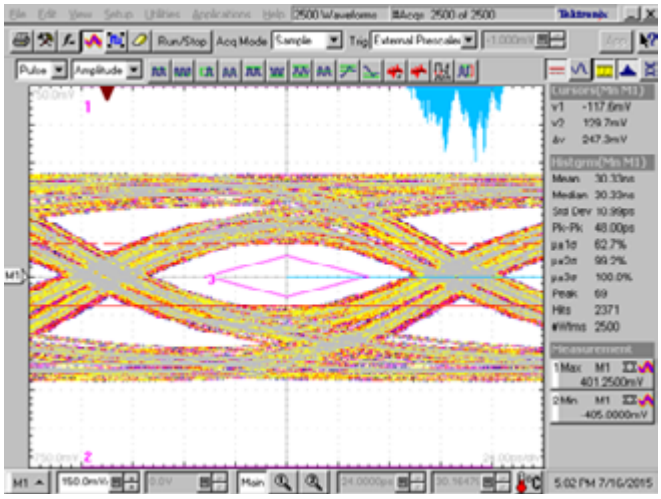
Using PRBS 2^23-1 pattern, Input Swing=800mVdiff, Output Swing= 1000mVdiff,

- FG = 11 (+2.5dB), EQ=8.9dB, Trace length = 30-in



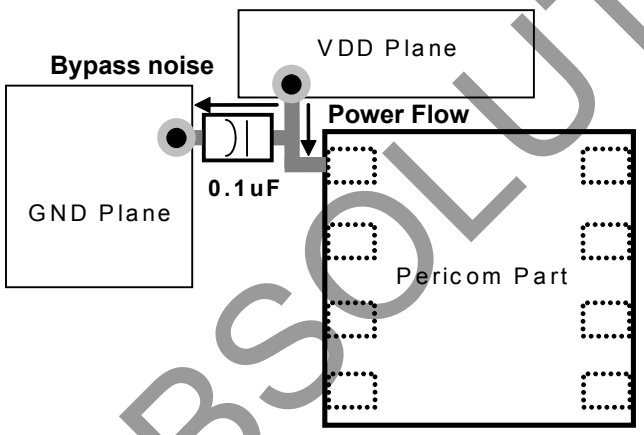
Using PRBS 2^23-1 pattern, Input Swing=800mVd, Output Swing= 1000mVdiff,

- FG = 11 (+2.5dB), EQ=8.9dB Trace length = 48-in



Layout and Decoupling Capacitor Placement Guidelines

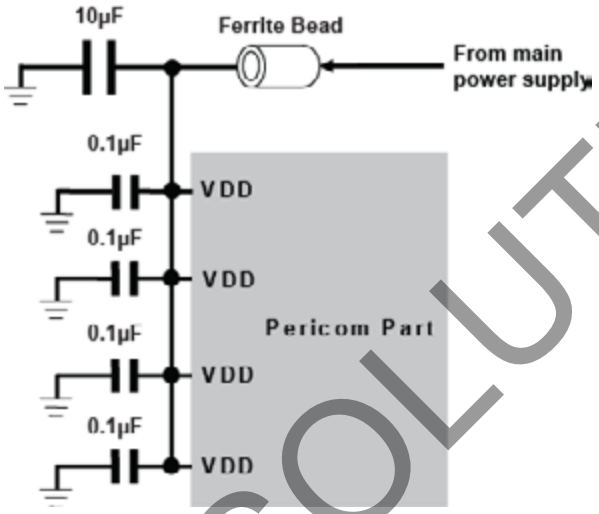
- Each 0.1µF decoupling capacitor should be placed as close as possible to each VDD pin.
- VDD and GND planes should be used to provide a low impedance path for power and ground.
- Via holes should be placed to connect to VDD and GND planes directly.
- Trace should be as wide as possible
- Trace should be as short as possible.
- The placement of decoupling capacitor and the way of routing trace should consider the power flowing criteria.
- 10µF capacitor should also be placed closed to our part and should be placed in the middle location of 0.1µF capacitors.
- Avoid the large current circuit placed close to our part; especially when it is shared the same VDD and GND planes. Since large current flowing on our VDD or GND planes will generate a potential variation on the VDD or GND of our part.



Decoupling Capacitor Placement Diagram

Power Supply Decoupling Circuit

It is recommended to put 0.1 µF decoupling capacitors on each VDD pins of our part, there are four 0.1 µF decoupling capacitors are put in Figure 1 with an assumption of only four VDD pins on our part, if there is more or less VDD pins on our Pericom parts, the number of 0.1 µF decoupling capacitors should be adjusted according to the actual number of VDD pins. On top of 0.1 µF decoupling capacitors on each VDD pins, it is recommended to put a 10 µF decoupling capacitor near our part's VDD, it is for stabilizing the power supply for our part. Ferrite bead is also recommended for isolating the power supply for our part and other power supplies in other parts of the circuit. But, it is optional and depends on the power supply conditions of other circuits.



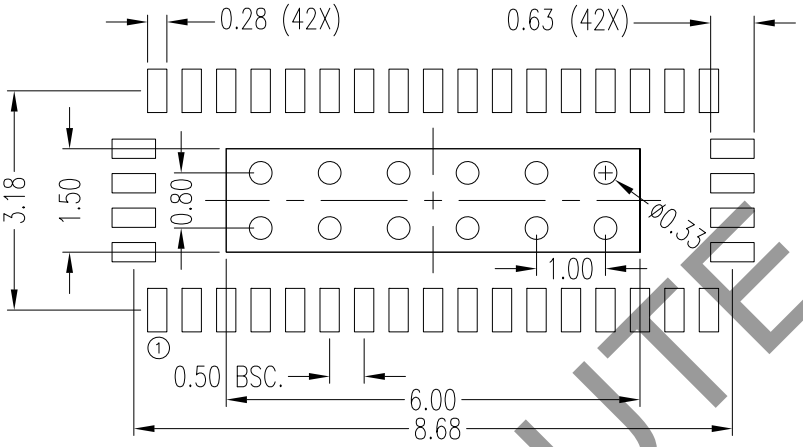
Recommended Power Supply Decoupling Capacitor Diagram

Requirements on the Decoupling Capacitors

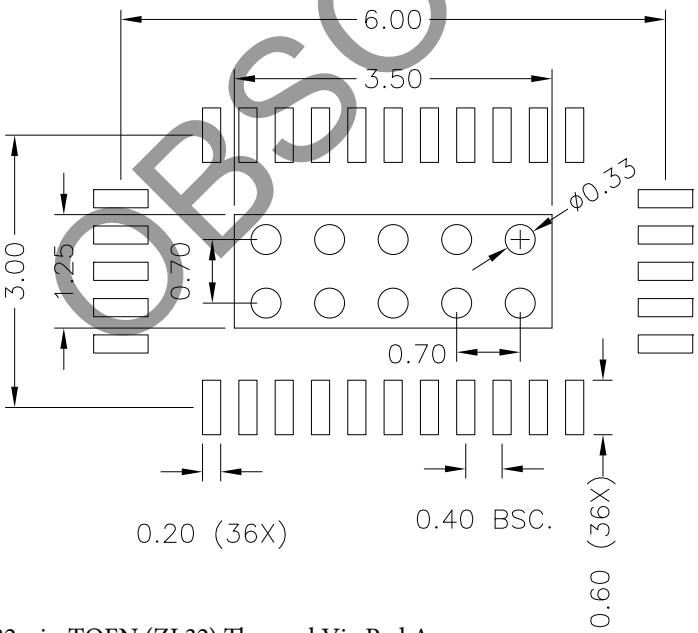
There is no special requirement on twhe material of the capacitors. Ceramic capacitors are generally being used with typically materials of X5R or X7R.

GND via on the thermal pad area Recommendation

Several GND via are "must" required on thermal area. The via size is 12/24 mil. Below are the recommendations

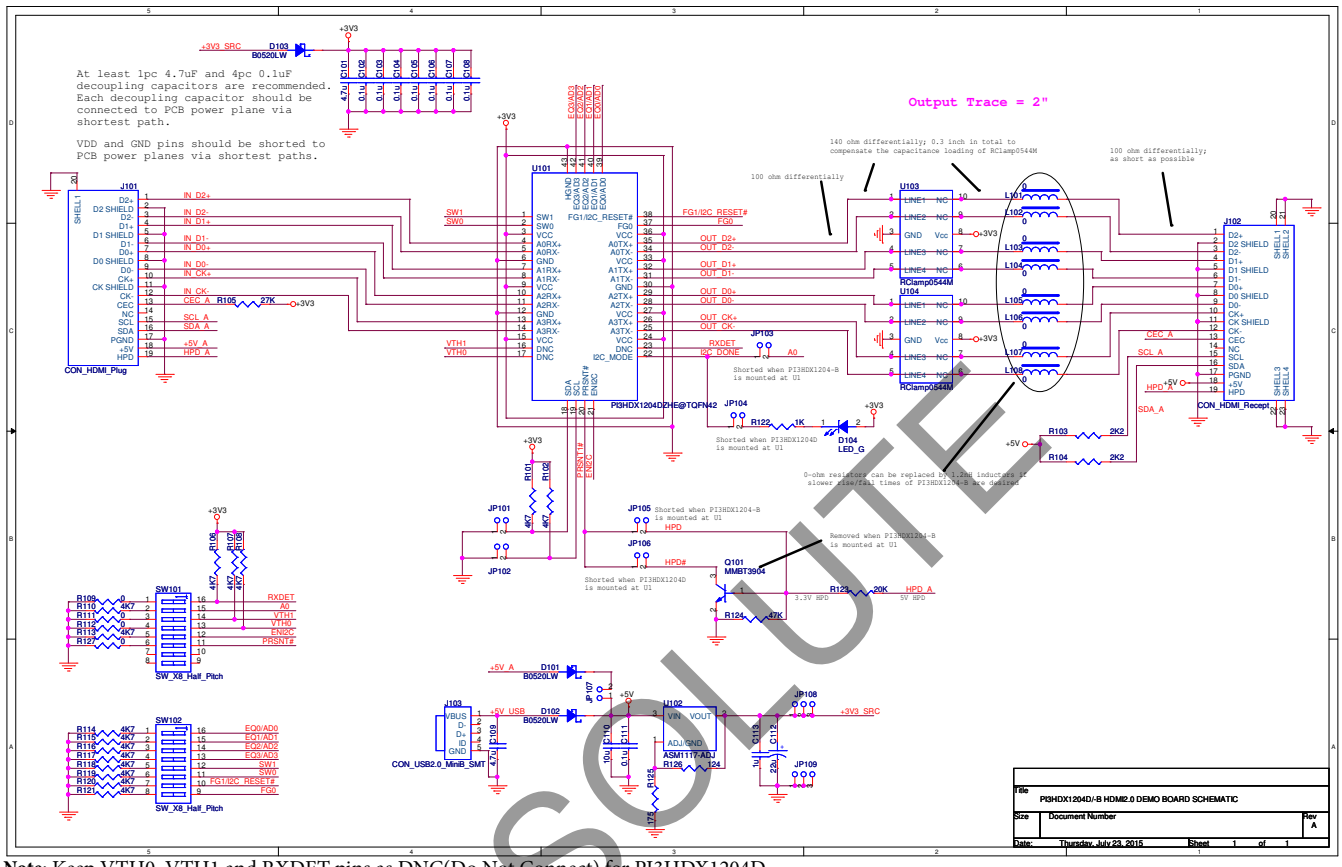


42-pin TQFN (ZH42) Thermal Via Pad Area



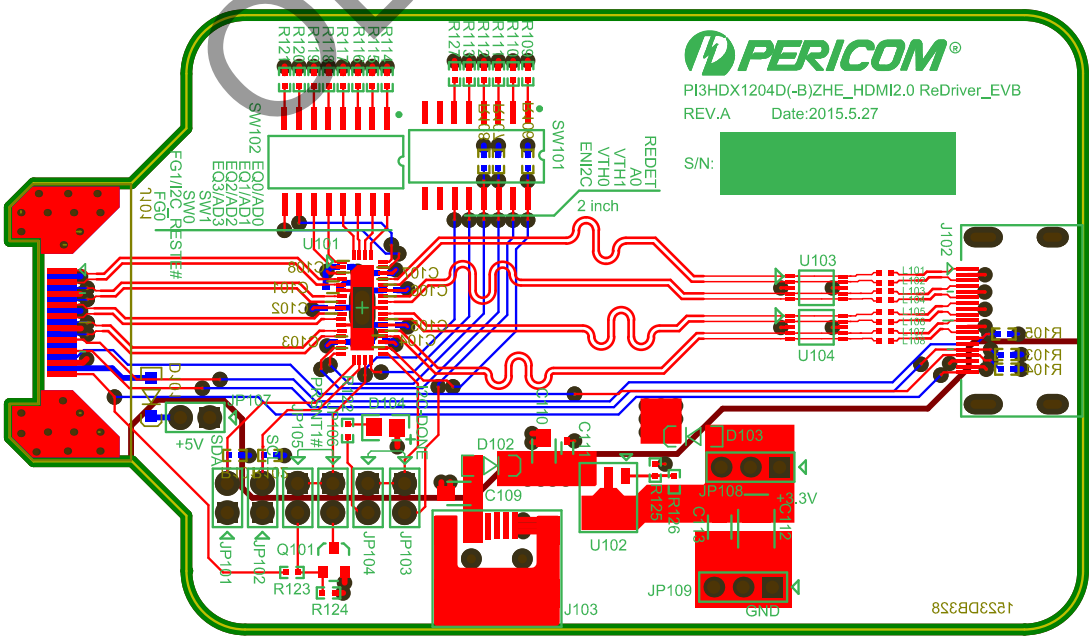
32-pin TQFN (ZL32) Thermal Via Pad Area

Reference Schematic



Note: Keep VTH0, VTH1 and RXDET pins as DNC(Do Not Connect) for PI3HDX1204D.

Evaluation Board PCB Layout



HDMI 2.0 Compliance Test Report

HDMI Test Report

Overall Result: PASS

Test Configuration Details	
Device Description	
Device ID	Transmitter
Fixture Type	Other
Probe Connection	4 Probes
Probe Head Type	N5444A
Lane Connection	1 Data Lane
HDMI Specification	2.0
HDMI Test Type	TMDS Physical Layer Tests
Test Session Details	
Infiniium SW Version	05.20.0013
Infiniium Model Number	DSOX92504A
Infiniium Serial Number	MY54410104
Application SW Version	2.11
Debug Mode Used	No
Probe (Channel 1)	Model: N2801A Serial: US54094067 Head: N5444A Atten: Calibrated (18 FEB 2015 11:16:48), Using Cal Atten (5.7831E+000) Skew: Calibrated (18 FEB 2015 11:16:56), Using Cal Skew
Probe (Channel 2)	Model: N2801A Serial: US54094054 Head: N5444A Atten: Calibrated (18 FEB 2015 11:19:29), Using Cal Atten (5.5882E+000) Skew: Calibrated (18 FEB 2015 11:13:57), Using Cal Skew
Probe (Channel 3)	Model: N2801A Serial: US54094059 Head: N5444A Atten: Calibrated (18 FEB 2015 11:15:19), Using Cal Atten (5.7320E+000) Skew: Calibrated (18 FEB 2015 11:15:29), Using Cal Skew
Probe (Channel 4)	Model: N2801A Serial: US54094057 Head: N5444A Atten: Calibrated (18 FEB 2015 11:11:30), Using Cal Atten (5.5123E+000) Skew: Calibrated (18 FEB 2015 11:12:12), Using Cal Skew
Last Test Date	2015-05-27 14:58:02 UTC +08:00

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	HF1-2: Clock Rise Time	162.046 ps	116.1 %	VALUE >= 75.000 ps
✓	0	1	HF1-2: Clock Fall Time	152.277 ps	103.0 %	VALUE >= 75.000 ps
✓	0	1	HF1-6: Clock Duty Cycle(Minimum)	49.640	24.1 %	>=40%
✓	0	1	HF1-6: Clock Duty Cycle(Maximum)	50.190	16.4 %	<=60%
✓	0	1	HF1-6: Clock Rate	148.562300000 MHz	2.2 %	85.000000000 MHz <= VALUE <= 150.000000000 MHz
✓	0	1	HF1-5: D0 Maximum Differential Voltage	648 m	16.9 %	VALUE <= 780 m
✓	0	1	HF1-5: D0 Minimum Differential Voltage	-659 m	15.5 %	VALUE >= -780 m
✓	0	1	HF1-2: D0 Rise Time	145.660 ps	242.7 %	VALUE >= 42.500 ps
✓	0	1	HF1-2: D0 Fall Time	143.400 ps	237.4 %	VALUE >= 42.500 ps
✓	0	1	HF1-8: D0 Mask Test (TP2_EQ with Worst Case Positive Skew)	0.000	50.0 %	No Mask Failures
✓	0	1	HF1-8: D0 Mask Test (TP2_EQ with Worst Case Negative Skew)	0.000	50.0 %	No Mask Failures
✓	0	1	HF1-1: VL Clock +	2.698 V	49.8 %	2.300 V <= VALUE <= 3.100 V
✓	0	1	HF1-1:Clock + VSwing	490 mV	27.5 %	200 mV <= VALUE <= 600 mV
✓	0	1	HF1-1: VL Clock -	2.718 V	47.8 %	2.300 V <= VALUE <= 3.100 V
✓	0	1	HF1-1:Clock - VSwing	486 mV	28.5 %	200 mV <= VALUE <= 600 mV
✓	0	1	HF1-4: Intra-Pair Skew - Clock	45 mTbit	35.0 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	HF1-1: VL D0+	2.697 V	33.8 %	2.300 V <= VALUE <= 2.900 V
✓	0	1	HF1-1: D0+ VSwing	518 mV	41.0 %	400 mV <= VALUE <= 600 mV
✓	0	1	HF1-1: VL D0-	2.699 V	33.5 %	2.300 V <= VALUE <= 2.900 V
✓	0	1	HF1-1: D0- VSwing	519 mV	41.0 %	400 mV <= VALUE <= 600 mV
✓	0	1	HF1-4: Intra-Pair Skew - Data Lane 0	17 mTbit	44.3 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	HF1-7: Differential Clock Voltage Swing, Vs (TP1)	933 mV	33.4 %	400 mV < VALUE < 1.200 V
✓	0	1	HF1-7: Clock Jitter (TP2_EQ with Worst Case Positive Skew)	250 mTbit	16.7 %	VALUE <= 300 mTbit
✓	0	1	HF1-7: Clock Jitter (TP2_EQ with Worst Case Negative Skew)	250 mTbit	16.7 %	VALUE <= 300 mTbit

Report Detail

Next

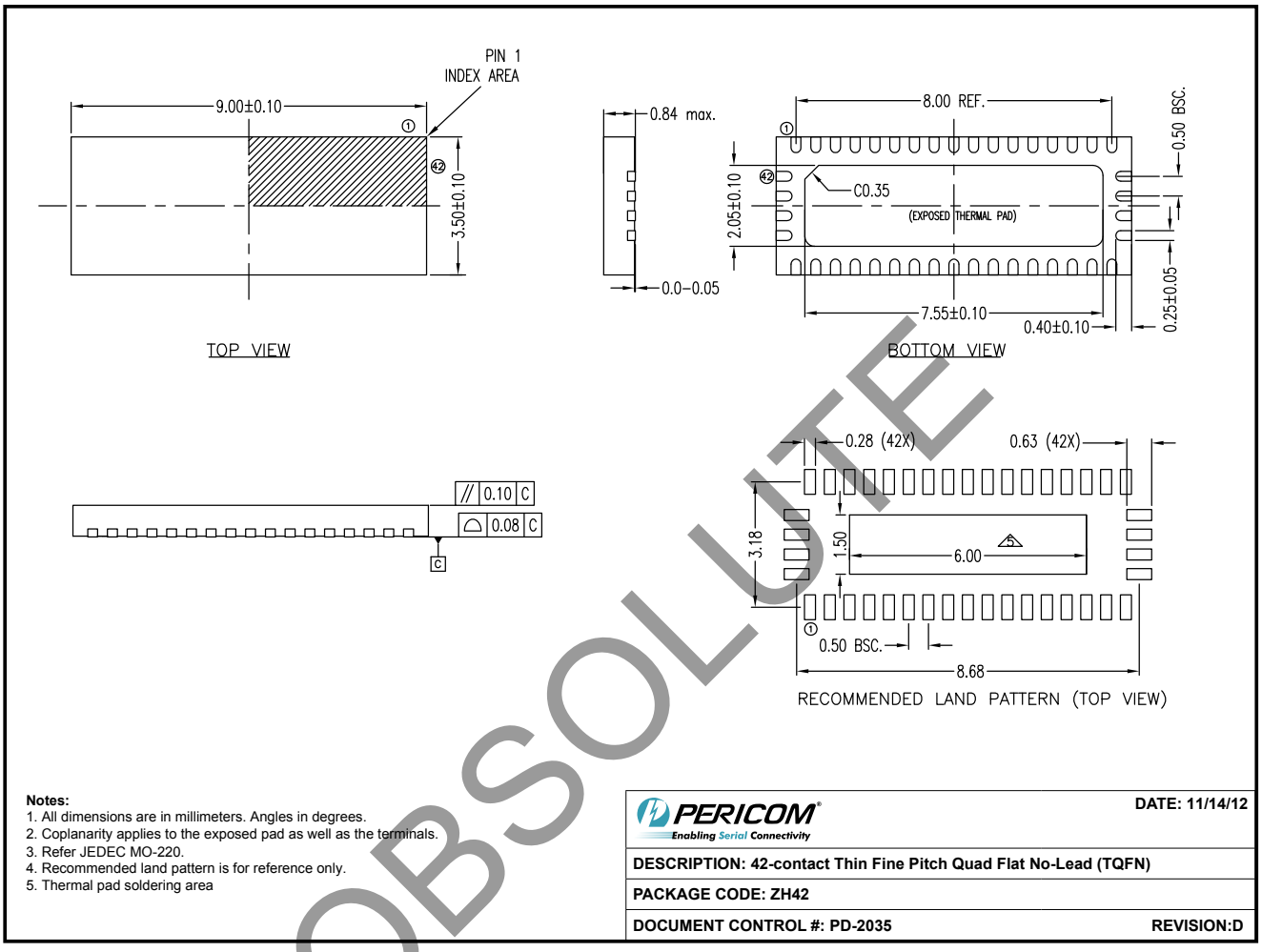
✓HF1-2: Clock Rise Time

Reference: Test ID HF1-2

Test Summary: Pass Test Description: 2 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Pass Limits: >= 75.000 ps **Raw Clock Transition Time** 162.046 ps

Packaging Mechanical: 42-Contact TQFN (ZH)



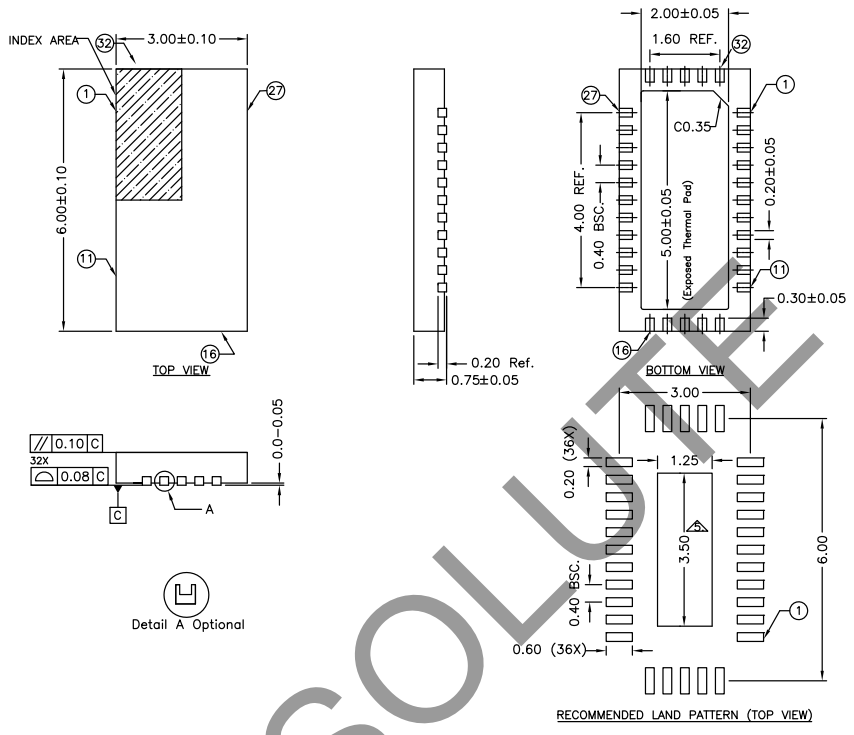
Note: For latest package info, please check: https://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Number	Package Code	Package Description
PI3HDX1204DZHE	ZH	Pb-free & Green 42-Contact TQFN

Notes:
- ZH suffix = Package Code
- E suffix = Pb-free and Green
- X suffix = Tape/Reel

Packaging Mechanical: 32-Contact TQFN (ZL)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).

PERICOM Enabling Serial Connectivity — DATE: 09/21/15

DESCRIPTION: 32-Contact, Very Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZL (ZL32)

DOCUMENT CONTROL #: PD-2044 — REVISION: B

Note: For latest package info, please check: https://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Number	Package Code	Package Description
PI3HDX1204DZLE	ZL	Pb-free & Green 32-Contact TQFN

Notes:
- ZL suffix = Package Code
- E suffix = Pb-free and Green
- X suffix = Tape/Reel

Related Products

Part Numbers	Products Description
PI3DPX1203	DisplayPort 1.3 Linear Redriver for Source/Sink/Cable Application
PI3HDX1204-B	HDMI 2.0 Redriver for sink-side application
PI3WVR12412	Wide Voltage Range 1:2 DP 1.2 & HDMI2.0 Passive Switch
PI3WVR31310	Wide Voltage Range 1:3 DP 1.2 & HDMI2.0 Passive Switch
PI3HDX414	HDMI 1.4b Splitter 1:4 with Signal Conditioning for 3.4Gb Application
PI3HDX412BD	HDMI 1.4b Splitter 1:2 with Signal Conditioning for 3.4Gb Application
PI3HDX511D/E	Ultra Low Power HDMI 1.4b Redriver and DP++ Level Shifter
PI3HDX511F	High EQ HDMI 1.4b Redriver and DP++ Level Shifter for Sink/Source Application
PI3EQXDP1201	DisplayPort 1.2 Redriver with built-in AUX Listener
PI3VDP3212/12412	2/4 Lanes DisplayPort 1.2 Compliant Passive Switch
PI3HDX621	HDMI 1.4 2:1 Active Switch with built-in ARC and Fast Switching support
PI3HDMI336	Active HDMI 3:1 Switch/Re-driver with I2C control and ARC Transmitter

Product Status Definition

Datasheet	Product Status	Definition
Advanced Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Pericom Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Pericom Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Pericom Semiconductor. The datasheet is for reference information only.

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