40V N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV_{DSS}	$R_{DS(ON)}$	I_D T_A = +25°C
40V	30mΩ @V_{GS} = 10V	13.7A
	50mΩ @V_{GS} = 4.5V	10.6A

Features

- Low On-Resistance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**
- **PPAP Capable (Note 4)**

Description and Applications

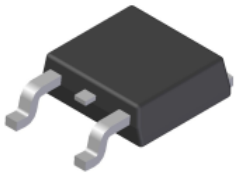
This MOSFET is designed to meet the stringent requirements of Automotive applications. It is qualified to AEC-Q101, supported by a PPAP and is ideal for use in:

- Backlighting
- DC-DC Converters
- Power Management Functions

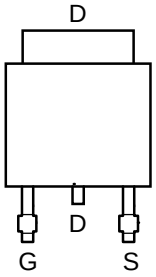
Mechanical Data

- Case: TO252 (DPAK)
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.33 grams (Approximate)

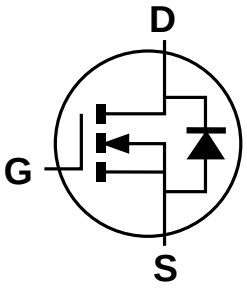
TO252 (DPAK)



Top View



Top View
Pin-Out



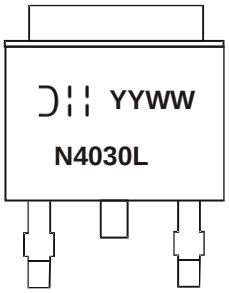
Equivalent Circuit

Ordering Information (Note 5)

Part Number	Case	Packaging
DMN4030LK3Q-13	TO252 (DPAK)	2,500/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. Automotive products are AEC-Q101 qualified and are PPAP capable. Refer to https://www.diodes.com/quality/product-compliance-definitions/
5. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



= Manufacturer's Marking
N4030L = Product Type Marking Code
YYWW = Date Code Marking
YY = Year (ex: 17 = 2017)
WW = Week (01 to 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	40	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 7) V_{GS} = 10V	Steady State	T_A = +25°C T_A = +70°C	I_D	13.7 10.9	A
Continuous Drain Current (Note 6) V_{GS} = 10V			I_D	9.4	A
Maximum Body Diode Continuous Current (Note 7)			I_S	10.7	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%) (Note 8)			I_{DM}	37.7	A
Pulsed Source Current (10µs Pulse, Duty Cycle = 1%) (Note 8)			I_{SM}	37.7	A

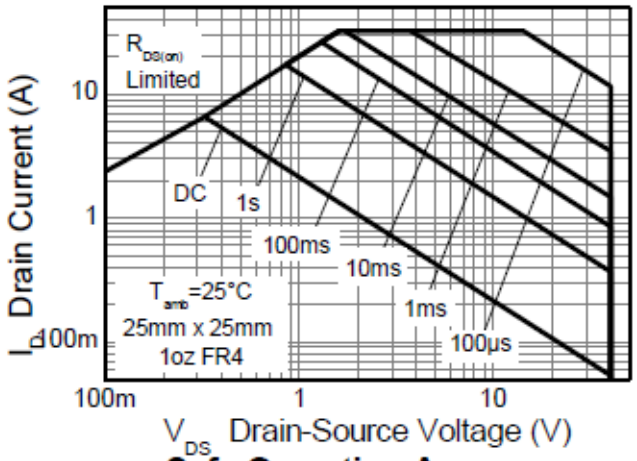
Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	4.18	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	29.9	°C/W
Total Power Dissipation (Note 7)	T_A = +25°C	P_D	8.9	W
Thermal Resistance, Junction to Ambient (Note 7)	T_A = +25°C	$R_{\theta JA}$	14.0	°C/W
Thermal Resistance, Junction to Case (Note 10)		$R_{\theta JC}$	2.46	
Total Power Dissipation (Note 9)	T_A = +25°C	P_D	2.14	W
Thermal Resistance, Junction to Ambient (Note 9)	Steady State	$R_{\theta JA}$	58.4	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

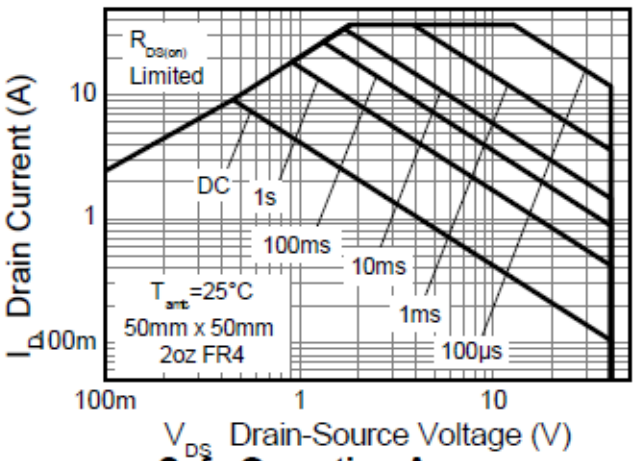
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 11)						
Drain-Source Breakdown Voltage	BV_{DSS}	40	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = 40V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 11)						
Gate Threshold Voltage	$V_{GS(TH)}$	1	—	3	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	21	30	mΩ	V_{GS} = 10V, I_D = 12A
		—	37	50		V_{GS} = 4.5V, I_D = 6A
Diode Forward Voltage	V_{SD}	—	0.95	1.1	V	V_{GS} = 0V, I_S = 12A
DYNAMIC CHARACTERISTICS (Note 12)						
Input Capacitance	C_{iss}	—	604	—	pF	V_{DS} = 20V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	106	—		
Reverse Transfer Capacitance	C_{rss}	—	59.6	—		
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	6.5	—	nC	V_{DS} = 20V, I_D = 12A
Total Gate Charge (V_{GS} = 10V)	Q_g	—	12.9	—		
Gate-Source Charge	Q_{gs}	—	2.3	—		
Gate-Drain Charge	Q_{gd}	—	3.6	—		
Turn-On Delay Time	$t_{D(ON)}$	—	4.2	—	ns	V_{DD} = 20V, I_D = 12A V_{GS} = 10V, R_G = 6Ω
Turn-On Rise Time	t_R	—	12.4	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	13.8	—		
Turn-Off Fall Time	t_F	—	10.7	—		
Body Diode Reverse Recovery Time	t_{RR}	—	135	—	ns	I_F = 12A, di/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q_{RR}	—	799	—	nC	I_F = 12A, di/dt = 100A/µs

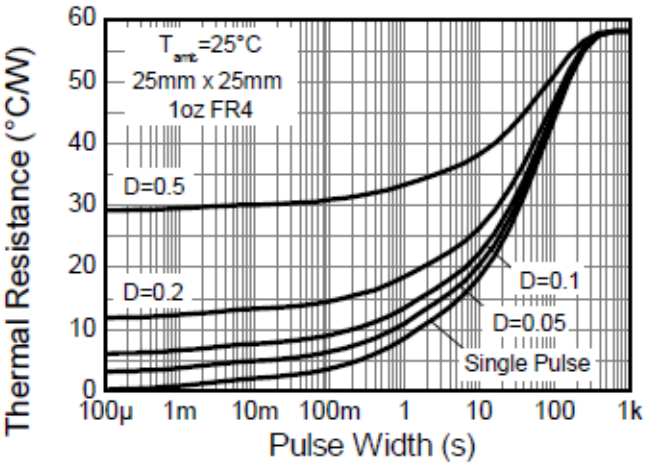
Notes:
6. For a device surface mounted on 50mm x 50mm x 1.6mm FR-4 PCB with high coverage of single sided 2oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
7. Same as note 6, except the device is measured at t ≤ 10 sec.
8. Same as note 6, except the device is pulsed with D = 0.02 and pulse width 300µs. The pulse current is limited by the maximum junction temperature.
9. For a device surface mounted on 25mm x 25mm x 1.6mm FR-4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
10. Thermal resistance from junction to solder-point (at the end of the drain lead).
11. Short duration pulse test used to minimize self-heating effect.
12. Guaranteed by design. Not subject to product testing.



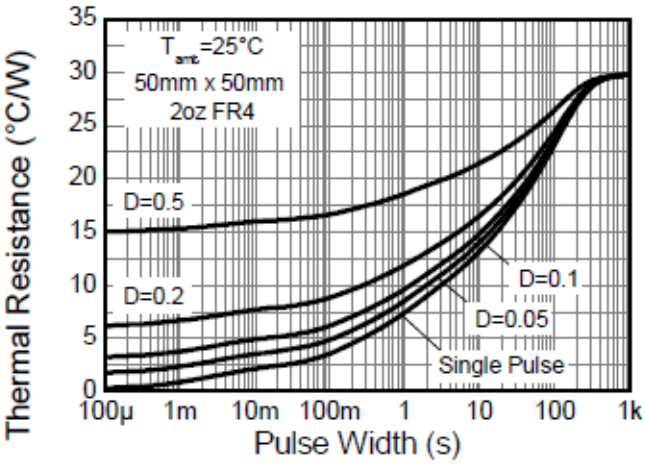
Safe Operating Area



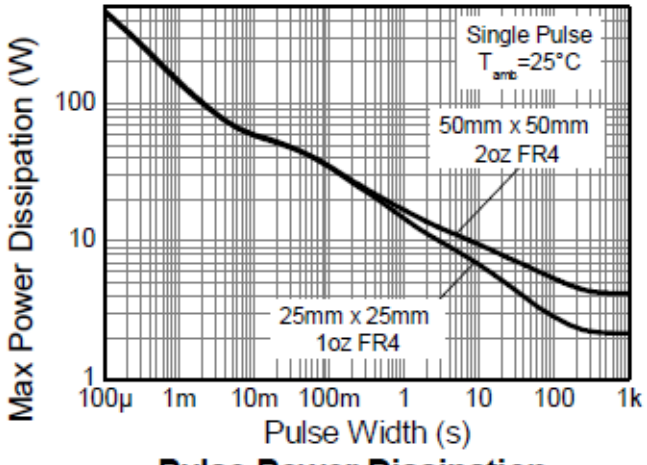
Safe Operating Area



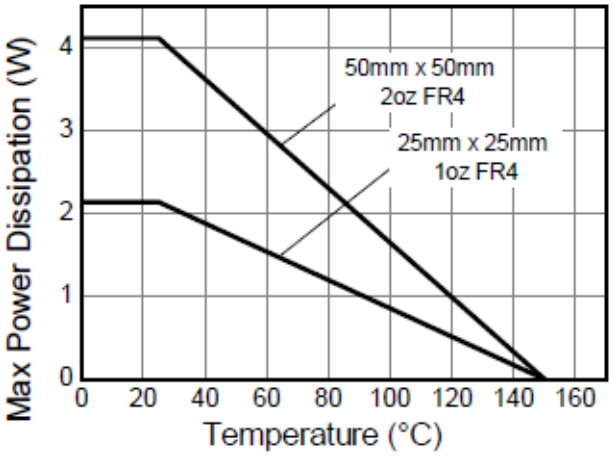
Transient Thermal Impedance



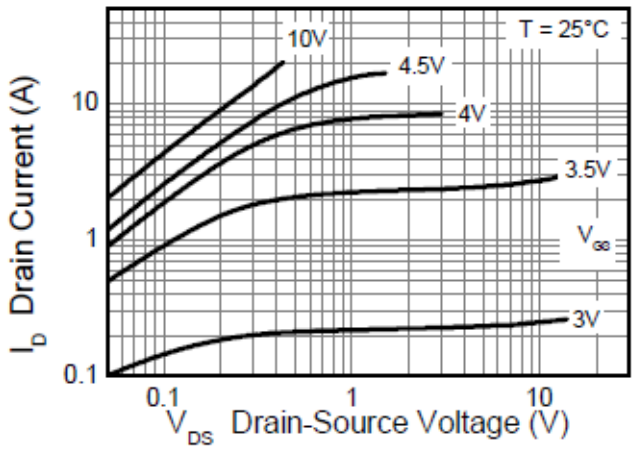
Transient Thermal Impedance



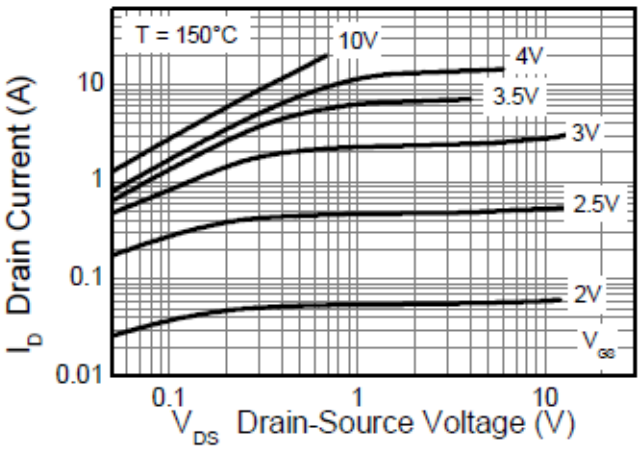
Pulse Power Dissipation



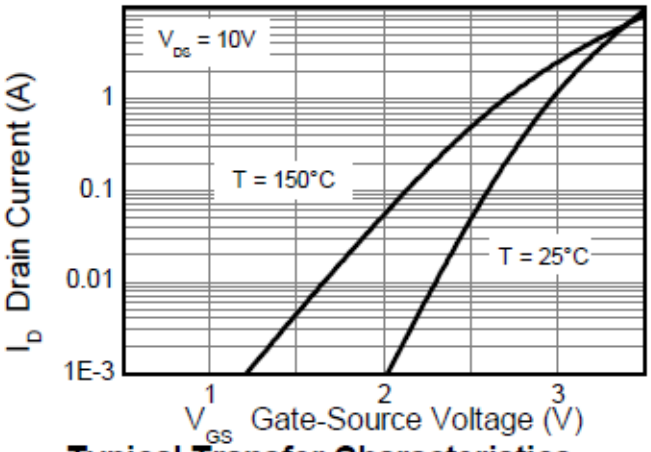
Derating Curve



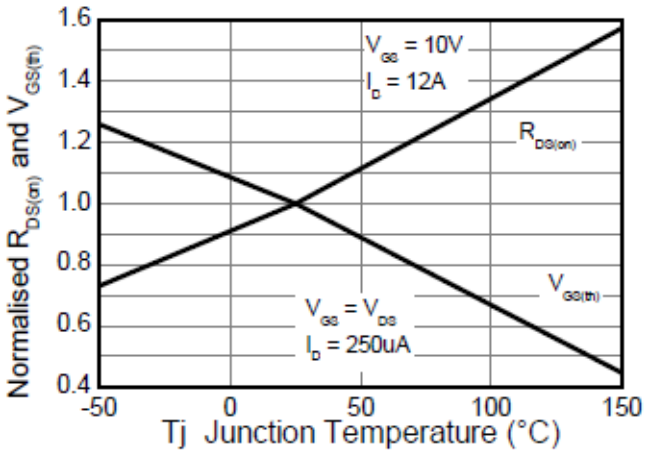
Output Characteristics



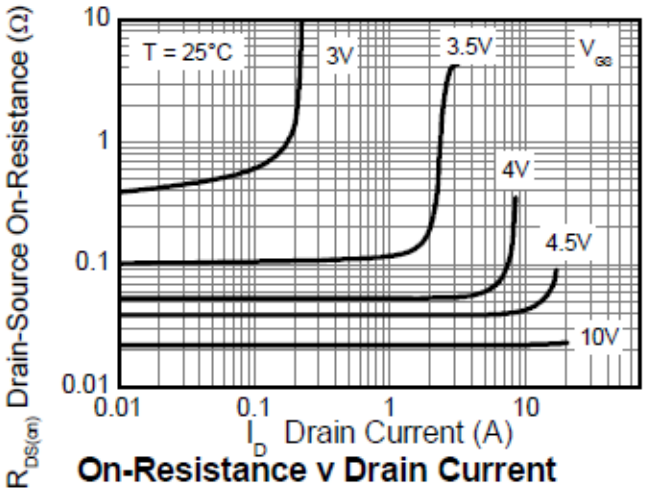
Output Characteristics



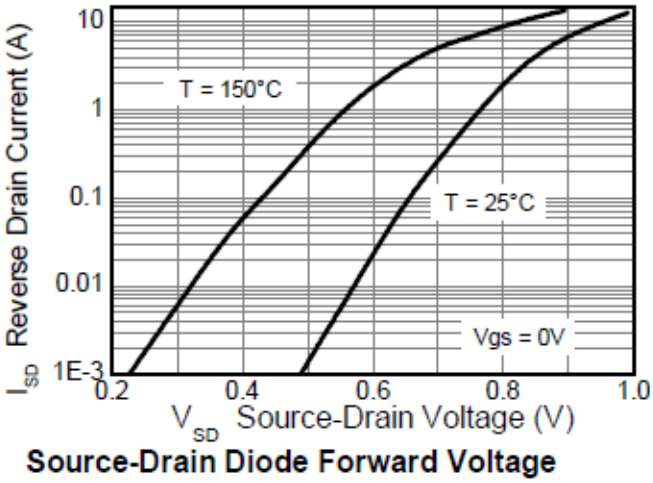
Typical Transfer Characteristics



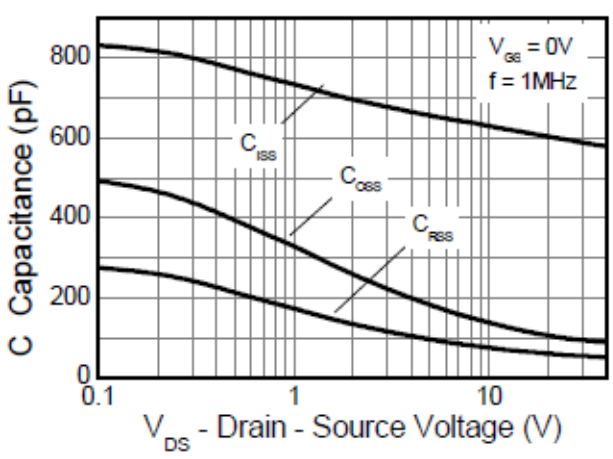
Normalised Curves v Temperature



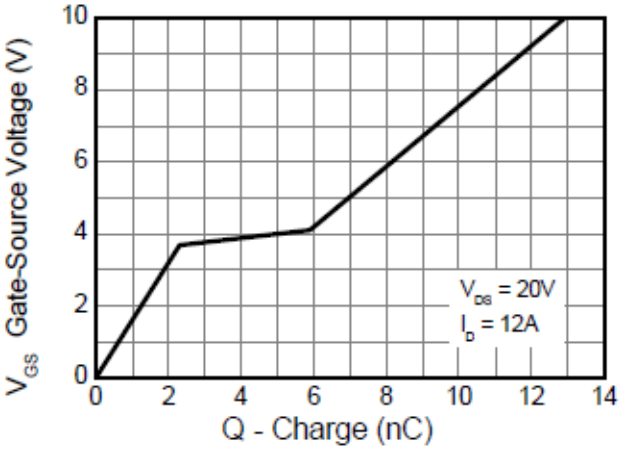
On-Resistance v Drain Current



Source-Drain Diode Forward Voltage



Capacitance v Drain-Source Voltage

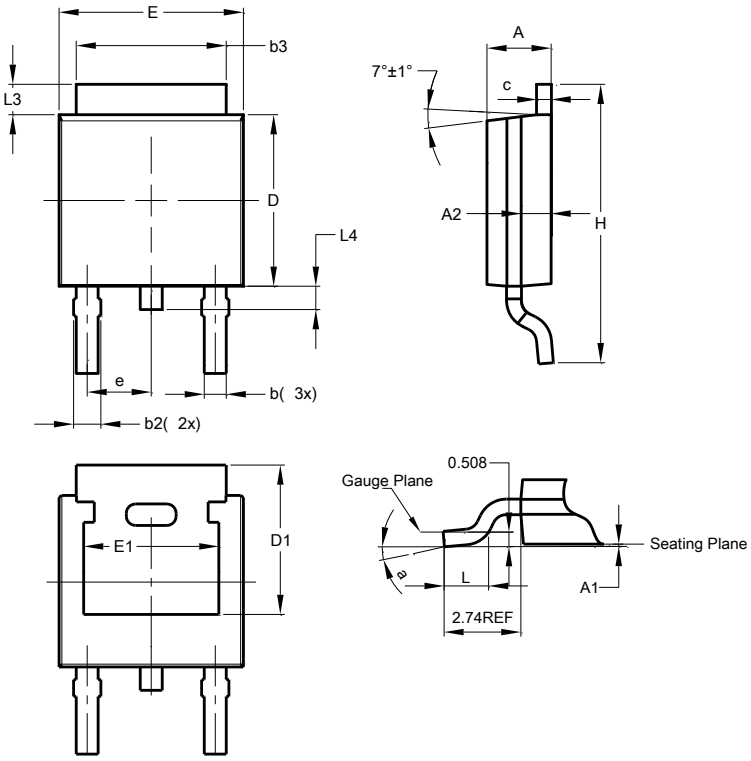


Gate-Source Voltage v Gate Charge

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

TO252 (DPAK)

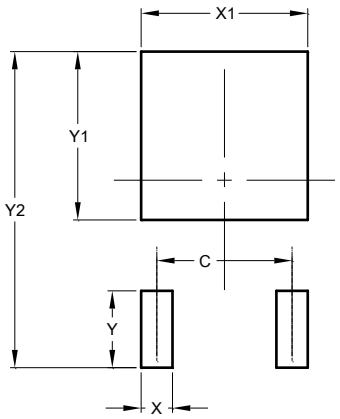


TO252 (DPAK)			
Dim	**Min**	**Max**	**Typ**
A	2.19	2.39	2.29
A1	0.00	0.13	0.08
A2	0.97	1.17	1.07
b	0.64	0.88	0.783
b2	0.76	1.14	0.95
b3	5.21	5.46	5.33
c	0.45	0.58	0.531
D	6.00	6.20	6.10
D1	5.21	-	-
e	-	-	2.286
E	6.45	6.70	6.58
E1	4.32	-	-
H	9.40	10.41	9.91
L	1.40	1.78	1.59
L3	0.88	1.27	1.08
L4	0.64	1.02	0.83
a	0°	10°	-
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

TO252 (DPAK)



Dimensions	Value (in mm)
C	4.572
X	1.060
X1	5.632
Y	2.600
Y1	5.700
Y2	10.700

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