A product Line of
Diodes Incorporated

PI3EQX12902A

12Gbps 1 Port/2 Channels SAS3/10GE/PCIe3/SATA3 Combo ReDriver with Linear Equalization

Features

- 12Gbps serial link with linear equalizer.
- Two 12Gbps differential signal pairs
- Support SAS3/10GE/PCIe3/SATA3 protocols
- Transparent to link training, OOB, Idle
- Pin Adjustable Receiver Equalization
- Pin Adjustable output linear swing
- Pin Adjustable Flat Gain
- 100Ω Differential CML I/O's
- Auto receiver detection for adaptive power management
- Auto "low power" mode for adaptive power management
- Single Supply Voltage: 3.3V ± 0.3V
- Industrial Temperature range: -40°C to 85°C
- Packaging: (Pb-free & Green)
  - 30-pin, TQFN 2.5x4.5 mm (ZL30)

Applications

- Notebook PC
- Server motherboards
- Rack server
- JBOD storage
- Blade server

Description

PI3EQX12902A is a low power, high performance 12Gbps 2 channels SAS3/10GE/PCIe3/SATA3 linear ReDriver.

The device provides programmable equalization, linear swing and flat gain to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference. PI3EQX12902A supports two 100Ω Differential CML data I/O's between the Protocol ASIC to a switch fabric, over cable, or to extend the signals across other distant data pathways on the user's platform.

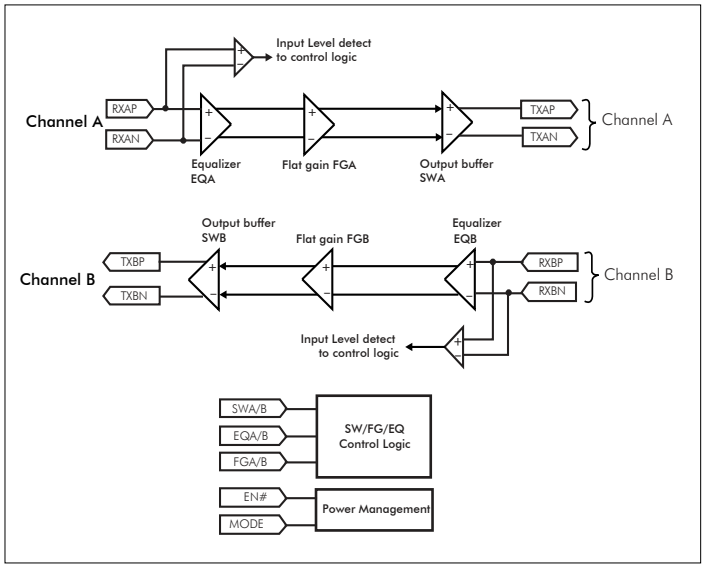
The integrated equalization circuitry provides flexibility with signal integrity of the signal before and after the ReDriver.

Each channel operates fully independently. The channels' input signal level determines whether the output is active.

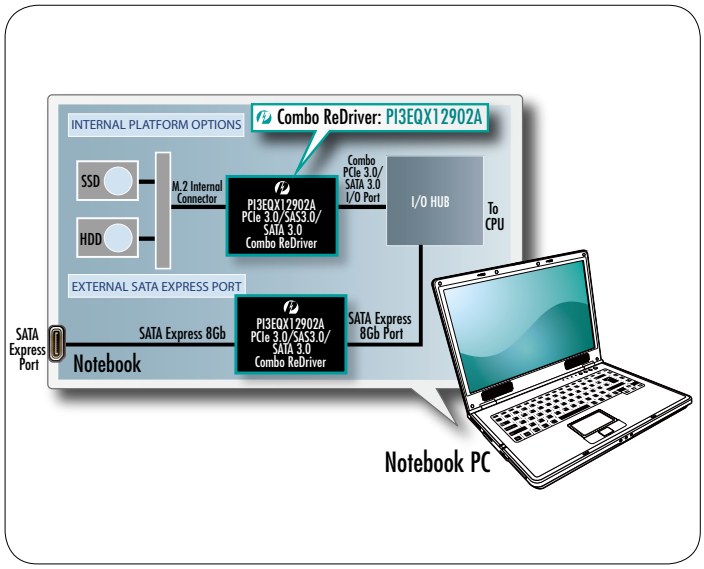
The PI3EQX12902A is a flexible, multi-protocol linear ReDriver designed to support new processor chipsets with dual protocol I/O pins, supporting SAS3 12Gbps, 10GE 10Gbps, PCIe3 8Gbps, SATA3 6Gbps speeds and connectors such as mSATA/M.2/SATAe/U.2 that can provide control signals.

The PI3EQX12902A is also an excellent choice for single lane applications requiring low power and small package such as docking station connectivity.

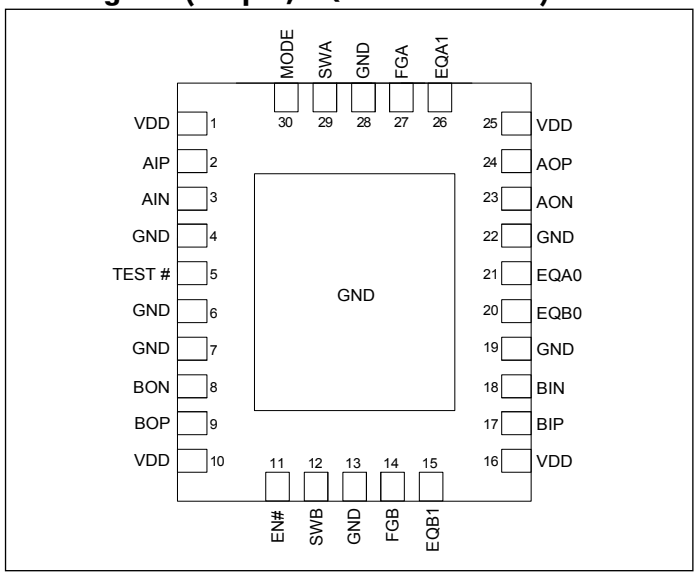
Block Diagram



Application Diagram



Pin Diagram (30-pin, TQFN 2.5x4.5mm) ZL30



Pin Description (30-pin, TQFN 2.5x4.5mm)

Pin #	Pin Name	Type	Description
1, 10, 16, 25	VDD	Power	3.3V power supply, +/-0.3V
27, 14	FGA FGB	Input	The DC flat gain selection. 4-level input pins. With internal 100KΩ pull-up resistor and 200kΩ pull-down resistor.
29, 12	SWA SWB	Input	The Output Swing selection. 4-level input pins. With internal 100KΩ pull-up resistor and 200kΩ pull-down resistor.
26, 21 15, 20	EQA1, EQA0 EQB1, EQB0	Input	The EQ selection. 4-level input pins. With internal 100KΩ pull-up resistor and 200kΩ pull-down resistor.
2, 3 17, 18	AIP, AIN BIP, BIN	Input	Differential input terminals. With selectable input termination between 50Ω to VDD and 67kΩ to VbiasRx or 67kΩ to GND.
24, 23 9, 8	AOP, AON BOP, BON	Output	Differential output terminals. With selectable output termination between 50Ω, 4K to VbiasTx or Hi-Z
5	TEST#	Input	Test mode Enable pin. With internal 300kΩ pull-up resistor. "High" – Test mode disabled. "Low" – Test mode enabled.
11	EN#	Input	Channel Enable pin. With internal 300kΩ pull down resistor. “High” – Channel is in power down mode. “Low” – Channel is in normal operation.
30	MODE	Input	Operation mode pin. “High” – For PCIe applications. “Low” – For SAS/SATA/10GE applications.
4, 6, 7, 13, 19, 22, 28, Center Pad	GND	GND	Supply Ground

Power Management

Notebooks, netbooks, and other power sensitive consumer devices require judicious use of power in order to maximize battery life. In order to minimize the power consumption of our devices, Pericom has added an additional adaptive power management feature.

SAS/SATA/10GE Application mode (MODE = Low)

When a signal detector is idle for longer than 1.3ms, the corresponding channel will move to low power mode ONLY. (It means both channels will move to low power mode individually).

In the low power mode, the signal detector will still be monitoring the input channel. If a channel is in low power mode and the input signal is detected, the corresponding channel will wake-up immediately.

Power Modes

Mode	R_{IN}	R_{OUT}
PD	67KΩ to GND	HIZ
Low Power Mode	50Ω to Vdd	4KΩ to V_{DD}
Active Mode	50Ω to Vdd	50Ω to V_{DD}

PCIe Application mode (MODE = High)

When a signal detector is idle for longer than 1.3ms, the corresponding channel will move to low power mode ONLY. (It means both channels will move to low power mode individually).

In the low power mode, the signal detector will still be monitoring the input channel. If a channel is in low power mode and the input signal is detected, the corresponding channel will wake-up immediately. If a channel is in low power mode and the signal detector is idle longer than 6ms, the receiver detection loop will be active again. if load is not detected, then the Channel will move to Device Unplug Mode and monitor the load continuosly. If load is detected, it will return to Low Power Mode and reciever detection will be active again for 6ms.

Operating Modes

Mode	R_{IN}	R_{OUT}
PD	67KΩ to GND	HIZ
Unplug Mode	67Ω to V_{BIASRx}	4KΩ to V_{BIASTx}
Low Power Mode	50Ω to Vdd	4KΩ to V_{DD}
Active Mode	50Ω to Vdd	50Ω to V_{DD}

Equalization Setting:

EQA/B are the selection pins for the equalization selection

EQ		Equalizer setting (dB)					
A1/B1	*A0/B0*	*@1.25GHz*	*@2.5GHz*	*@3GHz*	*@4GHz*	*@5GHz*	*@6GHz*
0	0	0.4	1.8	2.4	3.9	5.4	7.3
0	R	0.6	2.3	3.2	4.9	6.6	8.6
0	F	0.8	2.9	3.9	5.8	7.6	9.7
0	1	1.0	3.5	4.6	6.6	8.5	10.6
R	0	2.1	4.4	5.3	7.2	9.0	11.3
R	R	2.3	4.9	5.9	7.9	9.7	12.0
R	F	2.5	5.3	6.4	8.5	10.4	12.7
R	1	2.7	5.8	7.0	9.1	11.0	13.3
F	0	3.7	6.5	7.7	9.7	11.5	13.8
F	R	3.9	6.9	8.1	10.2	12	14.2
F	F	4.1	7.3	8.5	10.6	12.4	14.7
F	1	4.3	7.6	8.9	11.0	12.8	15.1
1	0	5.4	8.4	9.5	11.4	13.1	15.2
1	R	5.6	8.7	9.8	11.8	13.4	15.6
1	F	5.8	9.0	10.2	12.1	13.7	15.8
1	1	5.9	9.2	10.4	12.5	14.0	16.1

Flat Gain Setting:

FGA/B are the selection bits for the DC gain

	Flat Gain Settings
FGA/B	*dB*
0	-3.5
R	-1.5
F	0 (Default)
1	+1.5

-1dB compression point output Swing Setting:

SWA/B are the selection bits for the -1dB compression point output swing setting (100Mhz)

	Output Linear Swing Settings
SWA/B	*mVppd*
0	990
R	1050
F	1000 (Default)
1	1120

Channel Enable Setting:

EN are the channel enable pin

Channel Enable Setting	
EN#	*Setting*
1	Disabled
0	Enabled (Default)

Test and Normal Operating Mode Setting:

TEST#	MODE	Supported Application	Supported Power Mode	Supported input trace length is VTH dependent
0	x	Active mode only (For any application)	-Active only	No
1	0	SATA3	-Active -Slumber -No RxDet	Yes
1	1	PCIe3	-Active mode -Slumber mode -Unplug mode	Yes

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....–65°C to +150°C
Supply Voltage to Ground Potential.....–0.5V to +4.6V
DC SIG Voltage.....–0.5V to V_{DD} +0.5V
Output Current .....–25mA to +25mA
Power Dissipation Continuous 1.0W
Operating Temperature.....–40°C to +85°C
Junction Temperature (Tj).....125°C
ESD, HBM .....-2kV to +2kV
ESD, CDM .....-500V to +500V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Control pin Specifications

(V_{DD} = 3.3 ± 0.3V TA = -40°C to 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
2-level control pins					
V_{IH}	DC input logic High	V_{DD}*0.65			V
V_{IL}	DC input logic Low			V_{DD}*0.35	V
I_{IH}	Input High current			25	uA
I_{IL}	Input Low current	-25			uA
4-level control pins					
V_{IH}	DC input logic "High"	0.92*VDD	V_{DD}		V
V_{IF}	DC input logic "Float"	0.59*V_{DD}	0.67*V_{DD}	0.75*V_{DD}	V
V_{IR}	DC input logic "With Rext to GND"	0.25*V_{DD}	0.33*V_{DD}	0.41*V_{DD}	V
V_{IL}	DC input logic "Low"		GND	0.08*V_{DD}	V
I_{IH}	Input High current			50	uA
I_{IL}	Input Low current	-50			uA
Rext	External resistor connects to GND (±5%)	64.6	68	71.4	kΩ

High speed I/O AC/DC Specifications of PCIe mode (Mode = 1)

(V_{CC} = 3.3 ± 0.3V, T_A = -40 to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{RX}	RX AC coupling capacitance			220		nF
S_{11}	Input return loss	10MHz to 4GHz differential		14		dB
		1GHz to 4GHz common mode		4.9		
S_{22}	Output return loss	10MHz to 4GHz differential		12.0		dB
		1GHz to 4GHz common mode		4.8		
R_{IN}	DC single-ended input impedance			50		Ω
	DC Differential Input Impedance			100		
R_{OUT}	DC Differential output Impedance			100		Ω
Z_{RX-HIZ}	DC input CM input impedance during reset or power down			67		kΩ
$V_{RX-DIFF-PP}$	Differential Input Peak-to-peak Voltage	Operational			1.2	Vppd
	Input source common-mode noise	DC – 200MHz			150	mVpp
$T_{TX-IDLE-SET-TO-IDLE}$	Max time to electrical idle after sending an EIOS			4	8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Max time to valid diff signal after leaving electrical idle			4	8	ns
V_{th+}	On threshold of signal detector	Signal swing @ 4GHz		100		mVppd
V_{th-}	Off threshold of signal detector	Signal swing @ 100MHz		85		mVppd
Vcc	Power supply voltage		3	3.3	3.6	V
P	Supply power	EN#=0		0.21	0.33	W
I	Supply current			64	92	mA
P_{idle}	Supply power	EN#=1		0.1	0.2	mW
G_P	Peaking gain (Compensation at 4GHz, relative to 100MHz, 100mVp-p sine wave input)	EQA1/A0 = 11		12.5		dB
		EQA1/A0 = F0		9.7		
		EQA1/A0 = 00		3.9		
		Variation around typical	-3		+3	dB
G_F	Flat gain (100MHz, EQ<3:0> = 1000, SW<1:0> = 10, EQx = FF, SW = F)	FG = 1		1.5		dB
		FG = F		0		
		FG = R		-1.5		
		FG = 0		-3.5		
		Variation around typical	-3		+3	dB
V_{1dB_100M}	-1dB compression point of output swing (at 100MHz)	SW = 1		1120		mVppd
		SW = F		1000		
		SW = R		1050		
		SW = 0		990		

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{1dB_4G}	-1dB compression point of output swing (at 4GHz)	SW = 1 SW = F SW = R SW = 0		1.0 0.9 0.95 0.80		Vppd
V_{Coup}	Channel isolation	100MHz to 4GHz, Figure 1 (Note 1)		25		dB
Vnoise_input	Input-referred noise	100MHz to 4GHz, FG<1:0> = 0, EQA1/A0 = 00, Figure 2		0.6		mV_{RMS}
		100MHz to 4GHz, FG<1:0> = 1, EQA1/A0 = 11, Figure 2		0.4		
Vnoise_output	Output-referred noise (Note 2)	100MHz to 4GHz, FG<1:0> = 0, EQA1/A0 = 00, Figure 2		0.7		mV_{RMS}
		100MHz to 4GHz, FG<1:0> = 1, EQA1/A0 = 11, Figure 2		0.9		

Note: (1) Measured using a vector-network analyzer (VNA) with -15dBm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.

(2) Guaranteed by design and characterization.

High speed I/O AC/DC Specifications of SAS/SATA/10GE mode (MODE = 0)

(V_{CC} = 3.3 ± 0.3V, T_A = -40 to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{RX}	RX AC coupling capacitance			220		nF
S_{11}	Input return loss	10MHz to 3GHz differential		11.0		dB
		1GHz to 3GHz common mode		5.0		
S_{22}	Output return loss	10MHz to 3GHz differential		11.5		dB
		1GHz to 3GHz common mode		4.8		
R_{IN}	DC single-ended input impedance			50		Ω
	DC Differential Input Impedance			100		
R_{OUT}	DC Differential output Impedance			100		Ω
Z_{RX-HIZ}	DC input CM input impedance during reset or power down			67		kΩ
$V_{RX-DIFF-PP}$	Differential Input Peak-to-peak Voltage	Operational			1.2	Vppd
	Input source common-mode noise	DC – 200MHz			150	mVpp
$T_{TX-IDLE-SET-TO-IDLE}$	Max time to electrical idle after sending an EIOS			4	8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Max time to valid diff signal after leaving electrical idle			4	8	ns
Vcc	Power supply voltage		3	3.3	3.6	V
P_{max}	Max Supply power	EN#=0		0.24	0.33	W

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{max}	Max Supply current			64	92	mA
P_{idle}	Supply power	EN#=1		0.1	0.2	mW
t_{pd}	Latency	From input to output		0.5		ns
G_P	Peaking gain (Compensation at 3GHz, relative to 100MHz, 100mVp-p sine wave input)	EQA1/A0 = 11 EQA1/A0 = F0 EQA1/A0 = 00		10.4 7.7 2.4		dB
		Variation around typical	-3		+3	dB
G_F	Flat gain (100MHz, EQ<3:0> = 1000, SW<1:0> = 10, EQx = FF, SW = F)	FG = 1 FG = F FG = R FG = 0		1.5 0 -1.5 -3.5		dB
		Variation around typical	-3		+3	dB
V_{1dB_100M}	-1dB compression point of output swing (at 100MHz)	SW = 1 SW = F SW = R SW = 0		1120 1000 1050 990		mVppd
V_{1dB_6G}	-1dB compression point of output swing (at 6GHz)	SW = 1 SW = F SW = R SW = 0		1.0 0.9 0.95 0.8		Vppd
V_{Coup}	Channel isolation	100MHz to 6GHz, Figure 1 (Note 1)		25		dB
Vnoise_input	Input-referred noise	100MHz to 6GHz, FG = 0, EQA1/A0 = 00, Figure 2		0.6		mV_{RMS}
		100MHz to 6GHz, FG = 1, EQA1/A0 = 11, Figure 2		0.4		
Vnoise_output	Output-referred noise (Note 2)	100MHz to 6GHz, FG = 0, EQA1/A0 = 00, Figure 2		0.7		mV_{RMS}
		100MHz to 6GHz, FG = 1, EQA1/A0 = 11, Figure 2		0.9		

Note:

(1) Measured using a vector-network analyzer (VNA) with -15dBm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.

(2) Guaranteed by design and characterization.

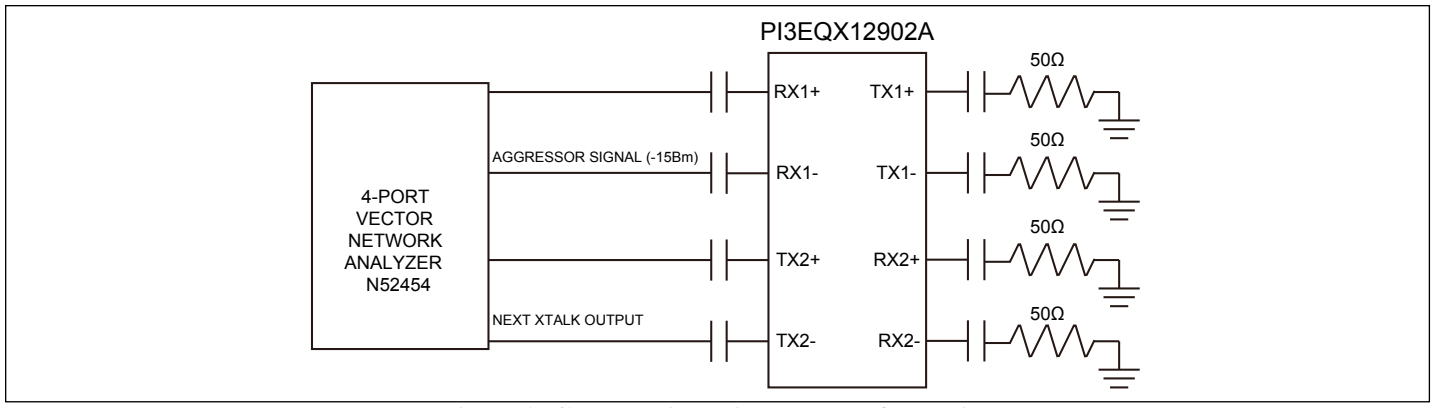


Figure1. Channel-isolation test configuration

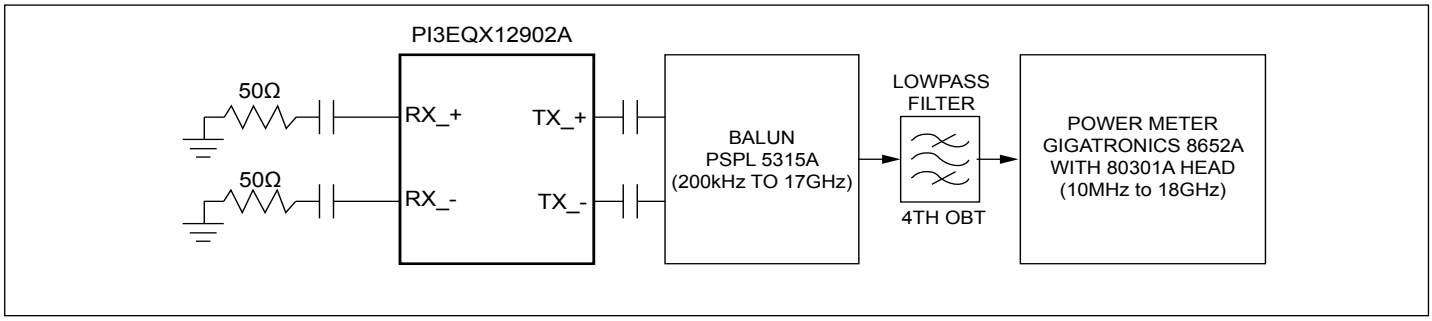
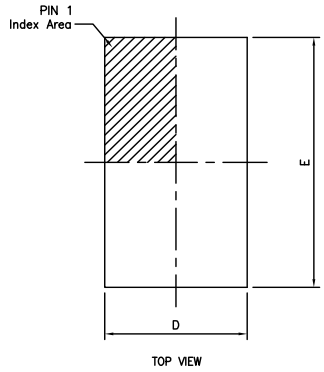
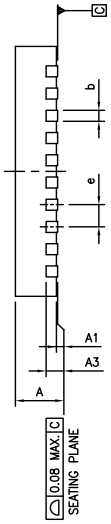
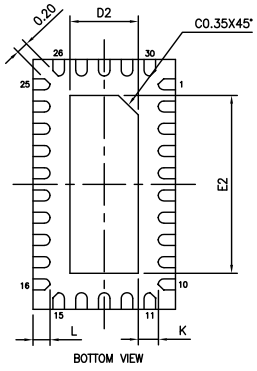


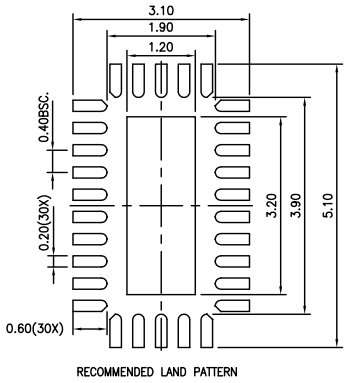
Figure2. Noise test configuration

Packaging Mechanical: 30-pin TQFN









SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D	2.40	2.50	2.60
E	4.40	4.50	4.60
D2	1.15	1.20	1.25
E2	3.15	3.20	3.25
e		0.40 BSC	
L	0.25	0.30	0.35
K	0.20	—	—

Notes:
1. All dimensions are in mm. Angles in degrees.
2. Refer JEDEC MO-220.
3. Recommended land pattern is for reference only.

PERICOM Enabling Serial Connectivity

DATE: 10/21/13

DESCRIPTION: 30-contact, Thin Fine Pitch Quad Flat No lead Package (TQFN)

PACKAGE CODE: ZL

DOCUMENT CONTROL #: PD-2172 **REVISION: --**

14-0006

For latest package info.
please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Number	Package Code	Package Description
PI3EQX12902AZLEX	ZL	30-contact, Thin Fine Pitch Quad Flat No-Lead (TQFN), Tape & Reel

Notes:

- Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
- E = Pb-free and Green
- Adding an X suffix = Tape/Reel

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

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