A product Line of
Diodes Incorporated

PI3EQX16904GL

16Gbps 4-Channel ReDriver with Linear Equalization

Features

- 2.5 to 16 Gbps Serial Link with Linear Equalizer
- Supports SAS3/ IB FDR/ PCIe4/ UPI Protocols
- Supporting Four Differential Channels
- Independent Channel Configuration of Receiver Equalization, Output Swing, and Flat Gain
- Rate and Coding Agnostic
- Transparent to Link Training, Idle, OOB
- Pin Strap and I^2C Selectable Device Programming
- 3-bit Selectable Address bit for I^2C
- Supply Voltage: 3.3V±0.3V
- Industrial Temperature Range: -40°C to 85°C
- Pin Strap Value Latched into I^2C Register
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Packaging (Pb-free & Green):
  - 42-contact TQFN (9mm × 3.5mm)

Description

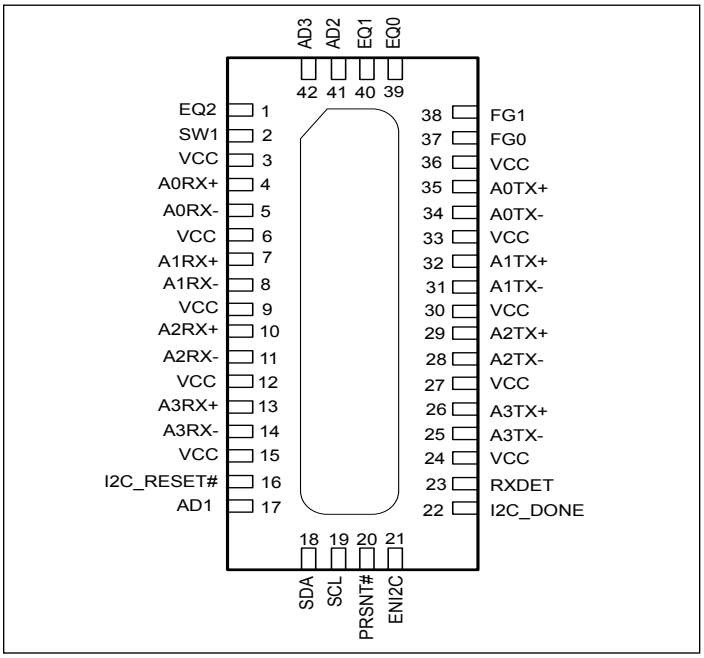
Diodes' PI3EQX16904GL is a multi-data rate, four differential channel ReDriver™. The device provides programmable linear equalization, output swing, and flat gain, by either pin strapping option or I^2C Control, to optimize performance over a variety of physical mediums by reducing intersymbol interference. PI3EQX16904GL supports four 100Ω differential CML data I/Os and extends the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver, whereas the integrated linear amplifier/buffer circuitry provides flexibility with signal integrity of the signal after the ReDriver.

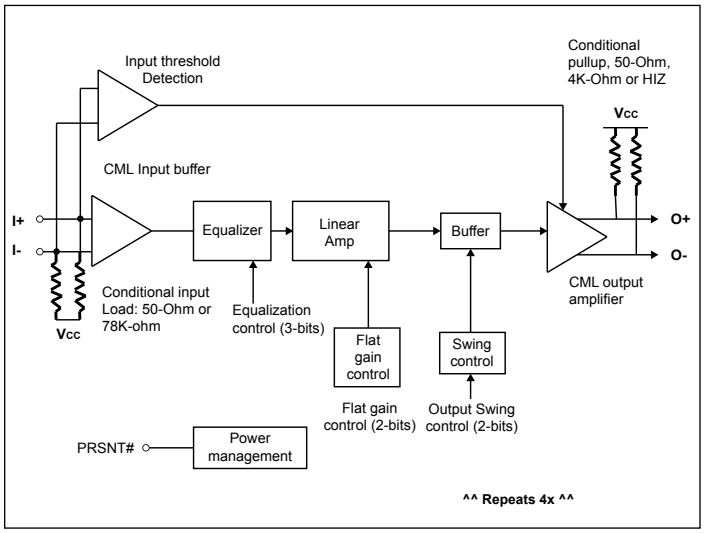
Applications

- Networking
- Enterprise
- Server
- Storage

Pin Configuration (Top-Side View)



Block Diagram



Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

ReDriver is a trademark of Diodes Incorporated.

Pin Description

Pin #	Pin Name	Type	Description
Data Signals			
4 5	A0RX+ A0RX-	I I	CML inputs for Channel A0 with internal 50Ω pullup and~78KΩ to Vbias Rx otherwise.
35 34	A0TX+ A0TX-	O O	CML outputs for Channel A0 with internal 50Ω pullup, 4KΩ to Vbias Tx, or high impedance.
7 8	A1RX+ A1RX-	I I	CML inputs for Channel A1 with internal 50Ω pullup and ~78KΩ to Vbias Rx otherwise.
32 31	A1TX+ A1TX-	O O	CML outputs for Channel A1 with internal 50Ω pullup, 4KΩ to Vbias Tx, or high impedance.
10 11	A2RX+ A2RX-	I I	CML inputs for Channel A2 with internal 50Ω pullup and ~78KΩ to Vbias Rx otherwise.
29 28	A2TX+ A2TX-	O O	CML outputs for Channel A2 with internal 50Ω pullup, 4KΩ to Vbias Tx, or high impedance.
13 14	A3RX+ A3RX-	I I	CML inputs for Channel A3 with internal 50Ω pullup and ~78KΩ to Vbias Rx otherwise.
26 25	A3TX+ A3TX-	O O	CML outputs for Channel A3 with internal 50Ω pullup, 4KΩ to Vbias Tx, or high impedance.
Control Signals			
19	SCL	I/O	I^2C SCL Clock. In Master mode (ENI2C floating), SCL is an output. Otherwise it is an input.
18	SDA	I/O	I^2C SDA data input/output.
42, 41, 17	AD[3:1]	I	I^2C programmable address bits with internal 300kΩ pullup.
20	PRSNT#	I	This pin is active in both PIN mode (ENI2C=LOW) and I^2C mode (ENI2C=HIGH). Cable present detect input. This pin has internal 300KΩ pullup. When HIGH, a cable is not present, and the device is put in lower power mode. When LOW, the device is enabled and in normal operation.
21	ENI2C	I	When LOW, each channel is programmed by the external pin voltage. When HIGH, each channel is programmed by the data stored in the I^2C bus. When floating, Master mode (Read External EEPROM). Input with 150KΩ pullup and down.
1, 40, 39	EQ[2:0]	I	Inputs with internal 300kΩ pullup. This pins set the amount of Equalizer Boost in all channel when ENI2C is LOW.
2	SW1	I	Inputs with internal 300kΩ pullup. This pin sets the output Voltage Level in all channel when ENI2C is LOW.
38, 37	FG[1:0]	I	Inputs with internal 300KΩ pull up resistor. Sets the output flat gain level on all channels when ENI2C is LOW.
16	I2C_RESET#	I	Inputs with internal 300KΩ pull up resistor. Reset pin for I^2C. When set LOW, the registers reset to default state.

Pin Description Cont.

Pin #	Pin Name	Type	Description
22	I2C_DONE	O	Valid register load status output, use for daisy chain master LOW = External EEPROM load failed HIGH = External EEPROM load passed
23	RXDET	I	This pin is active in both PIN mode(ENI2C=LOW) and I2C mode (ENI2C=HIGH). RXDET pin controls the receiver detect function. Tie High = Enable receiver detect to support PCIe3.0/PCIe4.0 and UPI interface Tie Low = Disable receiver detect to support SATA3/SAS3 interface, input is 50Ω to VDD RXDET pin has 300KΩ internal pullup
Power Pins			
3, 6, 9, 12, 15, 24, 27, 30, 33, 36	V_{CC}	PWR	3.3V Supply Voltage
EP	GND	PWR	Exposed pad. Supply Ground.

Note: 1. Be sure to use good conductive adhesive to properly attach package *Ground Pad* to PCB pad. This is both for thermal nd electrical conduction.

Description of Operation

Power Enable Function:

One pin control or I2C control. When PRSNT# is set to HIGH, the IC goes into power down mode—both input and output termination set to 78K and high impedance respectively. Individual Channel Enabling is done through the I2C register programming.

Equalization Setting:

EQ[2:0] are the selection pins for the equalization selection.

Table 1. Equalization Setting

Equalizer Setting (dB)						
EQ2	EQ1	EQ0	@1.25GHz	@2.5GHz	@4GHz	@8GHz
0	0	0	0.2	1.0	2.3	5.6
0	0	1	0.2	1.1	2.6	6.2
0	1	0	1.8	2.7	3.9	7.0
0	1	1	2.1	3.3	4.8	8.5
1	0	0	3.0	4.2	5.8	9.4
1	0	1	3.2	4.6	6.5	10.4
1	1	0	4.3	5.8	7.8	11.7
1	1	1	4.5	6.5	8.8	13.0

Flat Gain Setting:

FG[1:0] are the selection bits for the DC gain.

Table 2. Flat Gain Setting

Flat Gain Setting		
FG1	FG0	dB
0	0	-3.5
0	1	-2
1	0	-0.5
1	1	1

Swing Setting:

SW[1:0] are the selection bits for the output swing value.

Table 3. Swing Setting

Output Swing Setting		
SW1	SW0	mVp-p
0	0	800
0	1	1000
1	0	1100
1	1	1200

Note: 1. SW0 is from I2C, SW1 is from pin or I2C.

I²C Programming

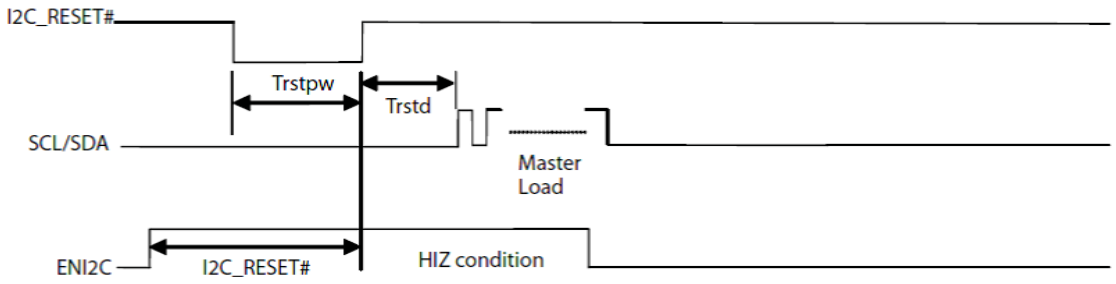
Address Assignment							
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**R/W**
1	1	1	AD3	AD2	AD1	0	1=R, 0=W

BYTE 0 Reserved					
BYTE 1 Reserved					
BYTE 2					
Bit	**Type**	**Powerup Condition**	**—**	**Control Affected**	**Comment**
7	R/W	0	—	A3 Powerdown	1 = Powerdown
6	R/W	0	—	A2 Powerdown	
5	R/W	0	—	A1 Powerdown	
4	R/W	0	—	A0 Powerdown	
3	R/W	0	—	—	
2	R/W	0	—	—	
1	R/W	0	—	—	
0	R/W	0	—	—	
BYTE 3					
Bit	**Type**	**Powerup Condition**	**—**	**Control Affected**	**Comment**
7	R/W	0	Channel A0 Configuration	—	Equalizer
6	R/W	EQ2		EQ2	
5	R/W	EQ1		EQ1	
4	R/W	EQ0		EQ0	
3	R/W	FG1		FG1	Flat Gain
2	R/W	FG0		FG0	
1	R/W	SW1		SW1	Swing
0	R/W	1		SW0	

I²C Programming Cont.

BYTE 4					
Bit	**Type**	**Powerup Condition**	**–**	**Control Affected**	**Comment**
7	R/W	0	Channel A1 Configuration	–	Equalizer
6	R/W	EQ2		EQ2	
5	R/W	EQ1		EQ1	
4	R/W	EQ0		EQ0	
3	R/W	FG1		FG1	Flat Gain
2	R/W	FG0		FG0	
1	R/W	SW1		SW1	Swing
0	R/W	1		SW0	
BYTE 5					
Bit	**Type**	**Powerup Condition**	**—**	**Control Affected**	**Comment**
7	R/W	0	Channel A2 Configuration	–	Equalizer
6	R/W	EQ2		EQ2	
5	R/W	EQ1		EQ1	
4	R/W	EQ0		EQ0	
3	R/W	FG1		FG1	Flat Gain
2	R/W	FG0		FG0	
1	R/W	SW1		SW1	Swing
0	R/W	1		SW0	
BYTE 6					
Bit	**Type**	**Powerup Condition**	**—**	**Control Affected**	**Comment**
7	R/W	0	Channel A3 Configuration	—	Equalizer
6	R/W	EQ2		EQ2	
5	R/W	EQ1		EQ1	
4	R/W	EQ0		EQ0	
3	R/W	FG1		FG1	Flat Gain
2	R/W	FG0		FG0	
1	R/W	SW1		SW1	Swing
0	R/W	1		SW0	
BYTE 7-9 with '0' Powerup Condition Reserved					

Reset and I2CM Timing Diagram



Recommended minimum reset pulse width T_{rstpw}= 1µs
I^2C master cycle start from I2C_RESET# pulse go high, Trstd = 200µs
ENI2C = HIZ to I2C_RESET#(high) (min), Ti2cm_rst = 1 uS.

I2C Operation

The integrated I2C interface operates as a master or slave device depending on the pin ENI2C being HIZ or HIGH respectively. Standard mode (100Kbps) is supported with 7-bit addressing. The data byte format is 8-bit bytes and supports the format of indexing to be compatible with other bus devices. In the Slave mode (ENI2C = HIGH), the device supports Read/Write. The bytes must be accessed in sequential order from the lowest to the highest byte with the ability to stop after any complete byte has been transferred.

Address bits A3 to A1 are programmable to support multiple chips environment.

In the Master mode (ENI2C = HIZ), PI3EQX16904GL supports up to eight masters connected in daisy chain through connecting I2C_DONE pin to I2C_RESET# pin of the next part.

Master EEPROM data starting address for device address:

I2C Address: AD3, AD2, AD1	Data Starting Location
000	00H
001	10H
010	20H
011	30H
100	40H
101	50H
110	60H
111	70H

Transferring Data

Every byte put on the SDA line must be 8-bits long. Each byte must be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (see the I2C Data Transfer diagram). The PI3EQX16904GL never holds the clock line SCL LOW to force the master into a wait state.

Acknowledge

Data transfer with acknowledge is required from the master. When the master releases the SDA line (HIGH) during the acknowledge clock pulse, the PI3EQX16904GL pulls down the SDA line during the acknowledge clock pulse, so it remains stable LOW during the HIGH period of this clock pulse as indicated in the I2C Data Transfer diagram. The PI3EQX16904GL generates an acknowledge after each byte has been received.

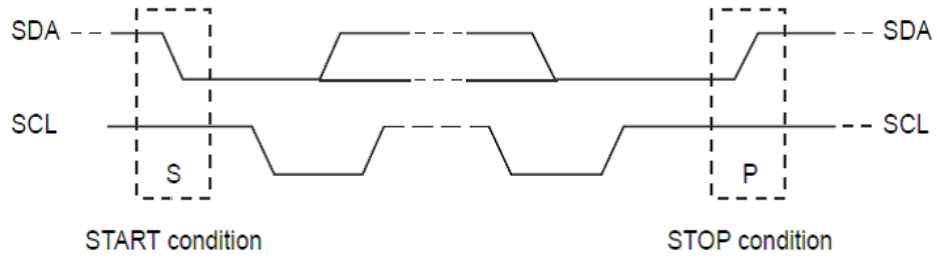
Data Transfer

A data transfer cycle begins with the master issuing a start bit. After recognizing a start bit, the PI3EQX16904GL watches the next byte of information for a match with its address setting. When a match is found it responds with a read or write of data on the following clocks. Each byte must be followed by an acknowledge bit except for the last byte of a read cycle, which ends with a stop bit. For a write cycle, the first data byte following the address byte is an index byte that is used by the PI3EQX16904GL. Data is transferred with the most significant bit (MSB) first.

I2C Data Transfer

Start & Stop Conditions

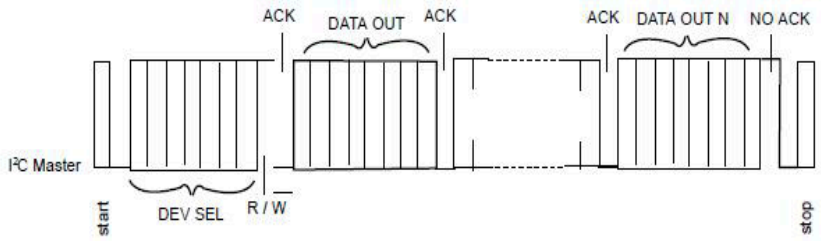
A HIGH-to-LOW transition on the SDA line while SCL is HIGH indicates a START condition. A LOW-to-HIGH transition on the SDA line while SCL is HIGH defines a STOP condition, as shown in the figure below.



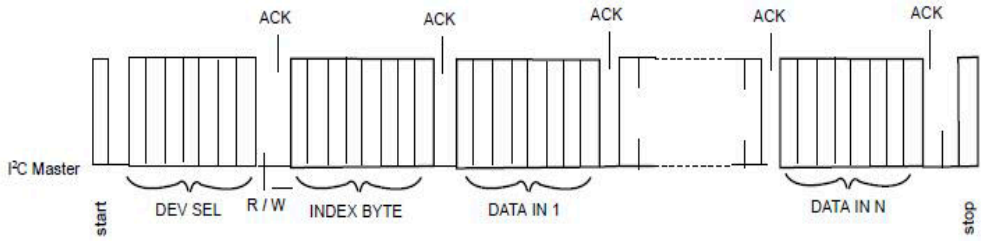
I^2C START and STOP conditions.

I2C Data Transfer

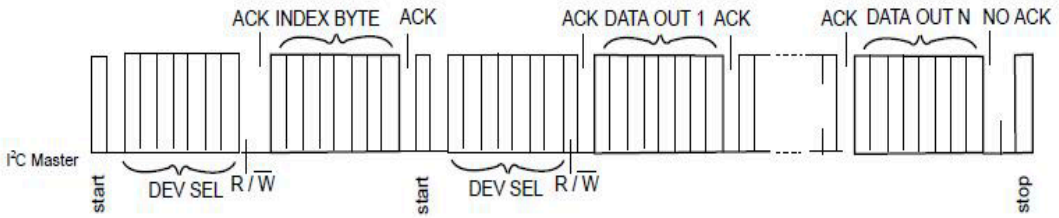
1. Read sequence



2. Write sequence



3. Combined sequence



Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +3.8V
DC SIG Voltage	–0.5V to V_{CC}+0.5V
Output Current	–25mA to +25mA
Power Dissipation Continuous	1.35W
Max Junction Temperature	125°C
ESD, HBM	–2kV to +2kV

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics:

LVCMOS I/O DC Specifications (V_{CC} = 3.3 ± 0.3V, T_A = -40°C to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	DC Input Logic High	—	0.4Vcc	—	V_{CC} + 0.3	V
V_{IL}	DC Input Logic Low	—	-0.3	—	0.1Vcc	V
V_{OH}	At IOH = -200µA	—	V_{CC} - 0.2	—	—	V
V_{OL}	At IOL = 200µA	—	—	—	0.2	V

SDA and SCL I/O for I2C-bus (V_{CC} = 3.3 ± 0.3V, T_A = -40°C to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	DC Input Logic High	—	V_{CC}/2 + 0.7	—	V_{CC} + 0.3	V
V_{IL}	DC Input Logic Low	—	-0.3	—	V_{CC}/2 - 0.7	V
V_{OL}	DC Output Logic Low	I_{OL} = 3mA	—	—	0.4	V
V_{hys}	Hysteresis of Schmitt Trigger Input	—	0.8	—	—	V
t_{of}	Output Fall Time from VIHmin to VILmax with bus cap. 10pF-400pF	—	—	—	250	ns
f_{SCLK}	SCLK Clock Frequency	—	—	—	100	kHz

High Speed I/O AC/DC Specifications (V_{CC} = 3.3 ± 0.3V, T_A = -40°C to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{RX}	RX AC Coupling Capacitance	—	—	220	—	nF
S_{11}	Input Return Loss	2.5GHz to 8GHz Differential	—	-6	—	dB
		2.5GHz to 8GHz Common Mode	—	-3	—	
S_{22}	Output Return Loss	2.5GHz to 8GHz Differential	—	-6	—	dB
		2.5GHz to 8GHz Common Mode	—	-3	—	

High Speed I/O AC/DC Specifications Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
R_{IN}	DC Single-Ended Input Impedance	—	—	50	—	Ω
	DC Differential Input Impedance	—	—	100	—	
R_{OUT}	DC Single-Ended Output Impedance	—	—	50	—	Ω
	DC Differential Output Impedance	—	—	100	—	
Z_{RX-HIZ}	DC Input CM Input Impedance During Reset or Power Down	—	—	78	—	kΩ
$V_{RX-DIFF-PP}$	Differential Input Peak-to-Peak Voltage	Operational	—	—	1.2	Vppd
	Input Source Common-Mode Noise	DC – 200MHz	—	—	150	mVpp
Vcc	Power Supply Voltage	—	3	3.3	3.6	V
P_{max}	Max Supply Power	PRSNT#=0	—	—	1.35	W
I_{max}	Max Supply Current	—	—	—	370	mA
P_{idle}	Supply Power	PRSNT#=1	—	—	3.6	mW
t_{pd}	Latency	From Input to Output	—	0.5	—	ns
G_P	Peaking Gain (Compensation at 8GHz, Relative to 100MHz, 100mVp-p Sine Wave Input)	EQ<2:0> = 111 EQ<2:0> = 000	— —	13.0 5.6	— —	dB
		Variation Around Typical	-3	—	+3	dB
G_F	Flat Gain (100MHz, EQ<2:0> = 100, SW<1:0> = 10)	FG<1:0> = 11 FG<1:0> = 10 FG<1:0> = 01 FG<1:0> = 00	— — — —	1 -0.5 -2 -3.5	— — — —	dB
		Variation Around Typical	-3	—	+3	dB
V_{1dB_100M}	-1dB Compression Point of Output Swing (at 100MHz)	SW<1:0> = 11 SW<1:0> = 10 SW<1:0> = 01 SW<1:0> = 00	— — — —	1200 1100 1000 800	— — — —	mVppd
V_{1dB_8G}	-1dB Compression Point of Output Swing (at 8GHz)	SW<1:0> = 11, FG<1:0> = 11, EQ<2:0>=111 SW<1:0> = 10, FG<1:0> = 11, EQ<2:0>=111 SW<1:0> = 01, FG<1:0> = 11, EQ<2:0>=111 SW<1:0> = 00, FG<1:0> = 11, EQ<2:0>=111	— — — —	1000 900 700 600	— — — —	mVppd
V_{Coup}	Channel Isolation	100MHz to 8GHz, Figure 1 (Note 1)	—	25	—	dB

High Speed I/O AC/DC Specifications Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Vnoise_input	Input-Referred Noise	100MHz to 8GHz, FG<1:0> = 10, EQ<2:0> = 000, Figure 2	—	0.8	—	mV_{RMS}
		100MHz to 8GHz, FG<1:0> = 10, EQ<2:0> = 111, Figure 2	—	0.5	—	
Vnoise_output	Output-Referred Noise (Note 2)	100MHz to 8GHz, FG<1:0> = 10, EQ<2:0> = 000, Figure 2	—	0.5	—	mV_{RMS}
		100MHz to 8GHz, FG<1:0> = 10, EQ<2:0> = 111, Figure 2	—	0.7	—	

Note: 1. Measured using a vector-network analyzer (VNA) with -15dBm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.
2. Guaranteed by design and characterization.

AC/DC Specifications - SCL/SDA for I2C BUS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	DC Input Logic High	—	$V_{CC}/2 + 0.7$	—	$V_{CC} + 0.3$	V
V_{IL}	DC Input Logic Low	—	-0.3	—	$V_{CC}/2 - 0.7$	V
V_{OL}	DC Output Logic Low	I_{OL} = 3mA	—	—	0.4	V
Ipullup	Current Through Pullup Resistor or Current Source	High Power specification	3.0	—	3.6	mA
VDD	Nominal Bus Voltage	—	3.0	—	3.6	V
Ileak-bus	Input Leakage per Bus Segment	—	-200	—	200	µA
Ileak-pin	Input Leakage per Device pin	—	—	-15	—	µA
CI	Capacitance for SDA/SCL	—	—	—	10	pF
Freq	Bus Operation Frequency	—	—	—	100k	Hz
TBUF	"Bus Free Time Between Stop and Start Condition"	—	1.3	—	—	µs
THD:STA	Hold Time After (Repeated) Start Condition After this period, the first clock is generated.	At Ipull-up, Max	0.6	—	—	µs
TSU:STA	Repeated Start Condition Setup Time	—	0.6	—	—	µs
TSU:STO	Stop Condition Setup Time	—	0.6	—	—	µs
THD:DAT	Data Hold Time	—	0	—	—	ns
TSU:DAT	Data Setup Time	—	100	—	—	ns
Tlow	Clock Low Period	—	1.3	—	—	µs
Thigh	Clock high period	—	0.6	—	50	µs

AC/DC Specifications - SCL/SDA for I2C BUS Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
tF	Clock/Data Fall Time	—	—	—	300	ns
tR	Clock/Data Rise Time	—	—	—	300	ns
tpor	"Time in which a device must be operation after power-on reset"	—	—	—	500	ms

Note: 1. Recommended value.
2. Recommended maximum capacitance load per bus segment is 400pF.
3. Compliant to I2C physical layer specification.
4. Ensured by Design. Parameter not tested in production.

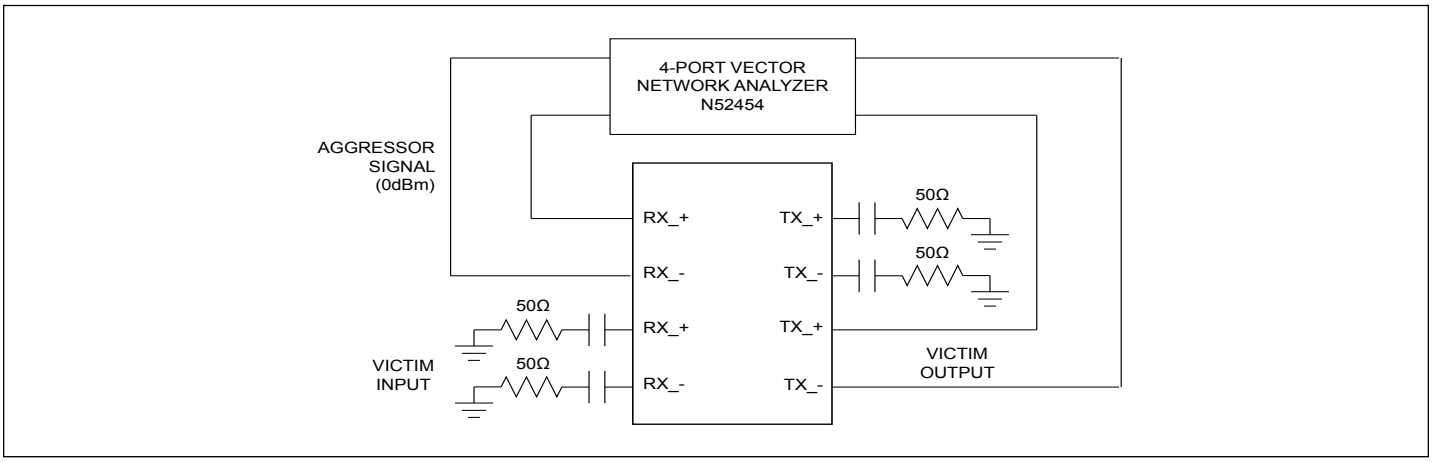


Figure 1. Channel-Isolation Test Configuration

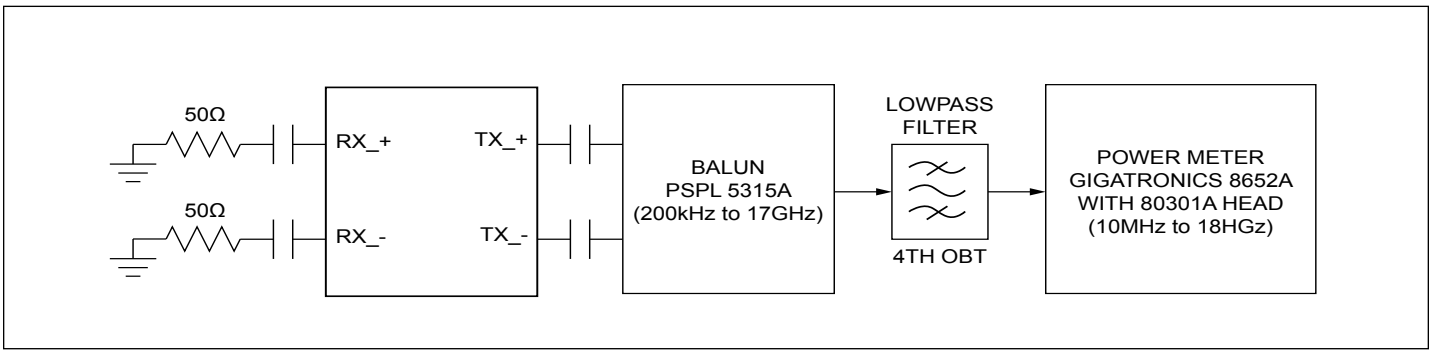
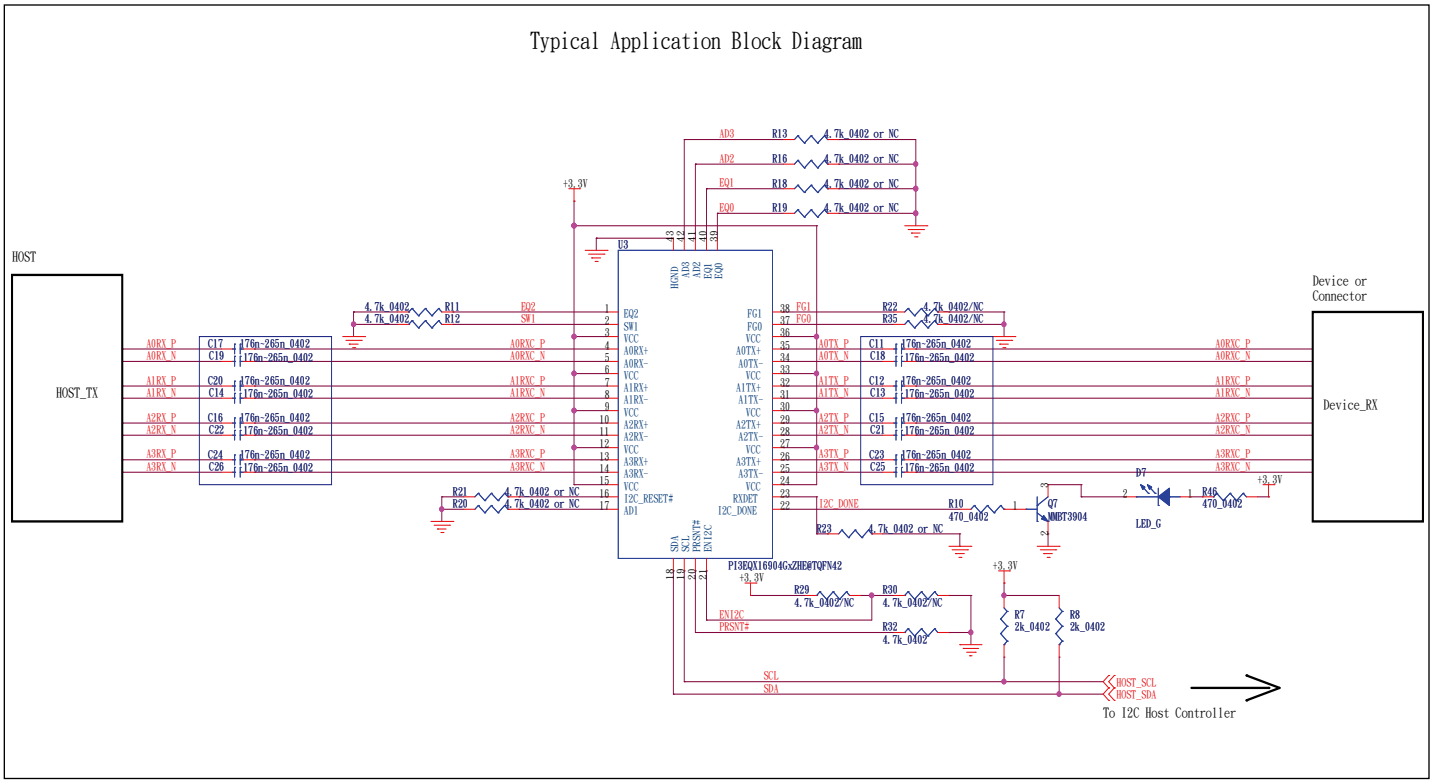


Figure 2. Noise Test Configuration

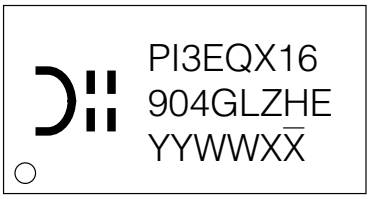
ESD Specification

- 2000V HBM
- 500V CDM

Application Diagram

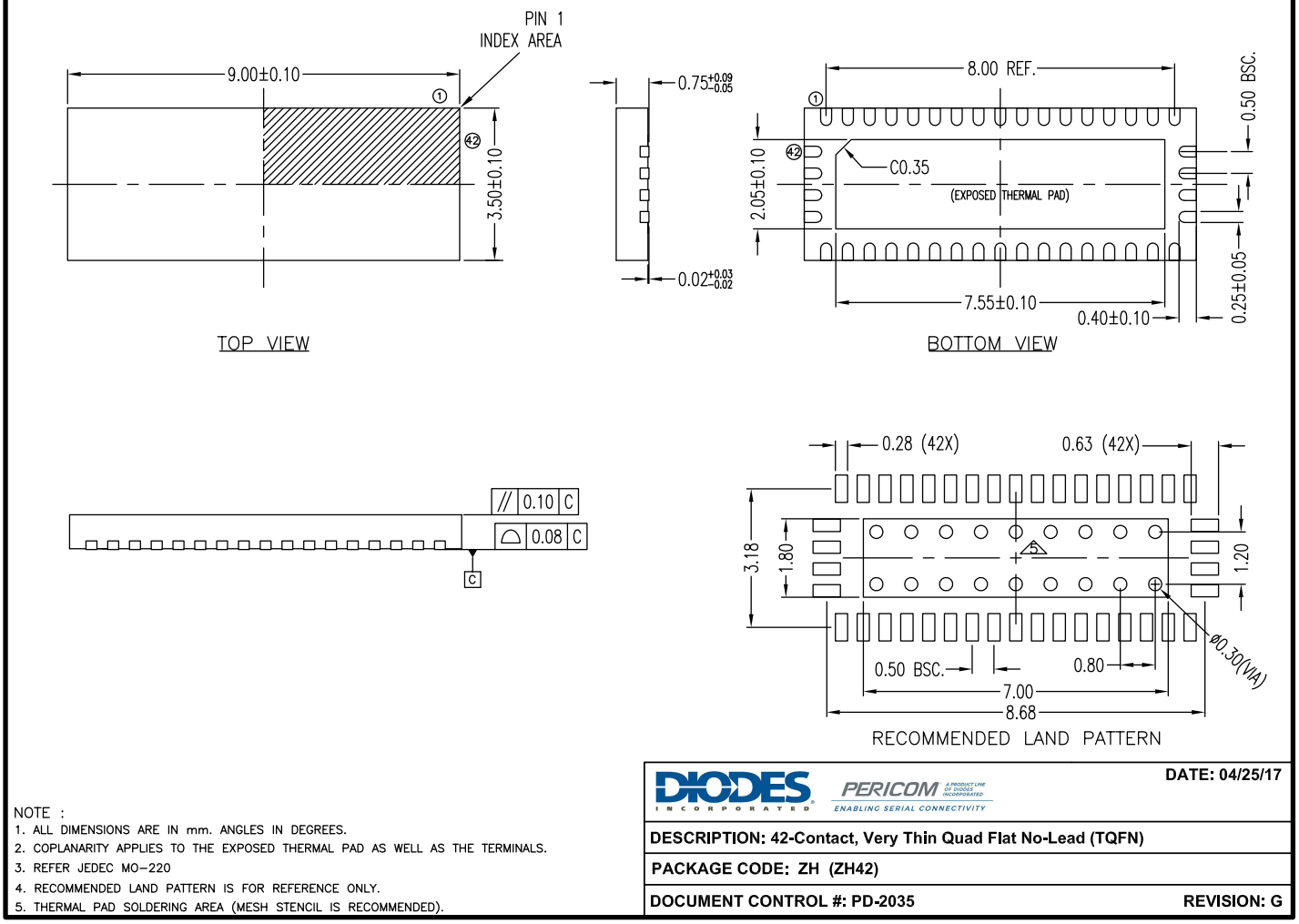


Part Marking



YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Package Mechanical: 42-TQFN (ZH)



17-0266

For latest package information:

See http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

Ordering Information

Ordering Number	Package Code	Package Description
PI3EQX16904GLZHEX	ZH	42-Contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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