Fact Sheet
DA9053 Flexible High Power System PMIC variants to support Freescale i.MX53 designs

General Description

The DA9053 is a quad buck PMIC subsystem suitable for use on Freescale's Multimedia Reference Platforms.

Combining a powerful switched-mode DC input/USB compatible charger, full power path management and multiple sleep modes the device offers an energy-optimised solution suitable for portable handheld, wireless and infotainment applications.

Interfacing directly to a Li-Ion/Polymer battery pack the high efficiency switching charger supports precise current/voltage charging as well as pre-charge and USB modes without processor interaction. During charging the die temperature is thermally regulated enabling higher capacity batteries to be rapidly charged at currents up to 1.8A with minimum thermal impact to space-constrained PCB's.

USB suspend mode operation is supported and for robustness the USB power inputs are protected against over-voltage conditions.

The autonomous power path controller seamlessly detects and manages energy flow between an AC adaptor, USB cable and battery whilst maintaining USB power specification compliance.

The internally-generated system power rail supports power scenarios such as instant-on with a full discharged battery. A reverse-protected backup battery charger is also integrated into the power path function.

The power efficiency and flexibility of the switching input stage is maintained to the generated supplies. Controlled by a programmable digital power manager the 14 user- programmable switched/linear regulators may be configured for a variety of start up sequences, levels and timings.

For optimal processor energy-per-task performance dynamic voltage scaling is available on up to five supply domains. Dialog's patented Smart Mirror™ dynamic biasing is implemented on all linear regulators.

Available in VFBGA 7x7mm package
VFBGA 11x11mm package

Features

- Switched DC/USB Charger with power path management
- 4 Buck Converters (3 with DVS) 0.5V-2.5V up to 2Amp
- 10 Programmable LDO's, High PSRR, 1% accuracy.
- Low power Backup Charger 1.1-3.1V up to 6mA
- 32kHz RTC Oscillator
- 10 channel general Purpose ADC with touch screen interface with pen down detect
- High voltage Boost for white LED Backlights
- 16 bit GPIO bus for enhanced wakeup and peripheral control
- Dual serial control interfaces with arbitration
- Flexible autoboot and memory configurations
- Variants to support DDR3 and LPDDR2 memory
- Autoboot option available
- Extended temperature & AEC Q100 grades available.

Applications

- Mobile Internet Devices
- Tablet PC's
- Personal Navigation devices
- Consumer & In-Vehicle Infotainment devices

dialog SEMICONDUCTOR

DA9053 Standard variants to support i.MX53 designs

Important notice

- The Freescale Quickstart board uses DA9053-30 this supports i.MX53 800Mhz operation with DDR3 memory but does not support suspend/resume operation, battery charging or auto-boot

- The Freescale Sabre Tablet board uses DA9053-3B this supports i.MX53 1GHz operation with DDR3 memory and will support suspend/resume operation, but does not support battery charging or auto-boot

- Standard variants are orderable for production. DA9053-3F will directly replace both of the above variants but will also support battery charging if a battery NTC thermistor is detected. All other standard variants can also replace the above variants to support Auto-boot or LPDDR2 memory

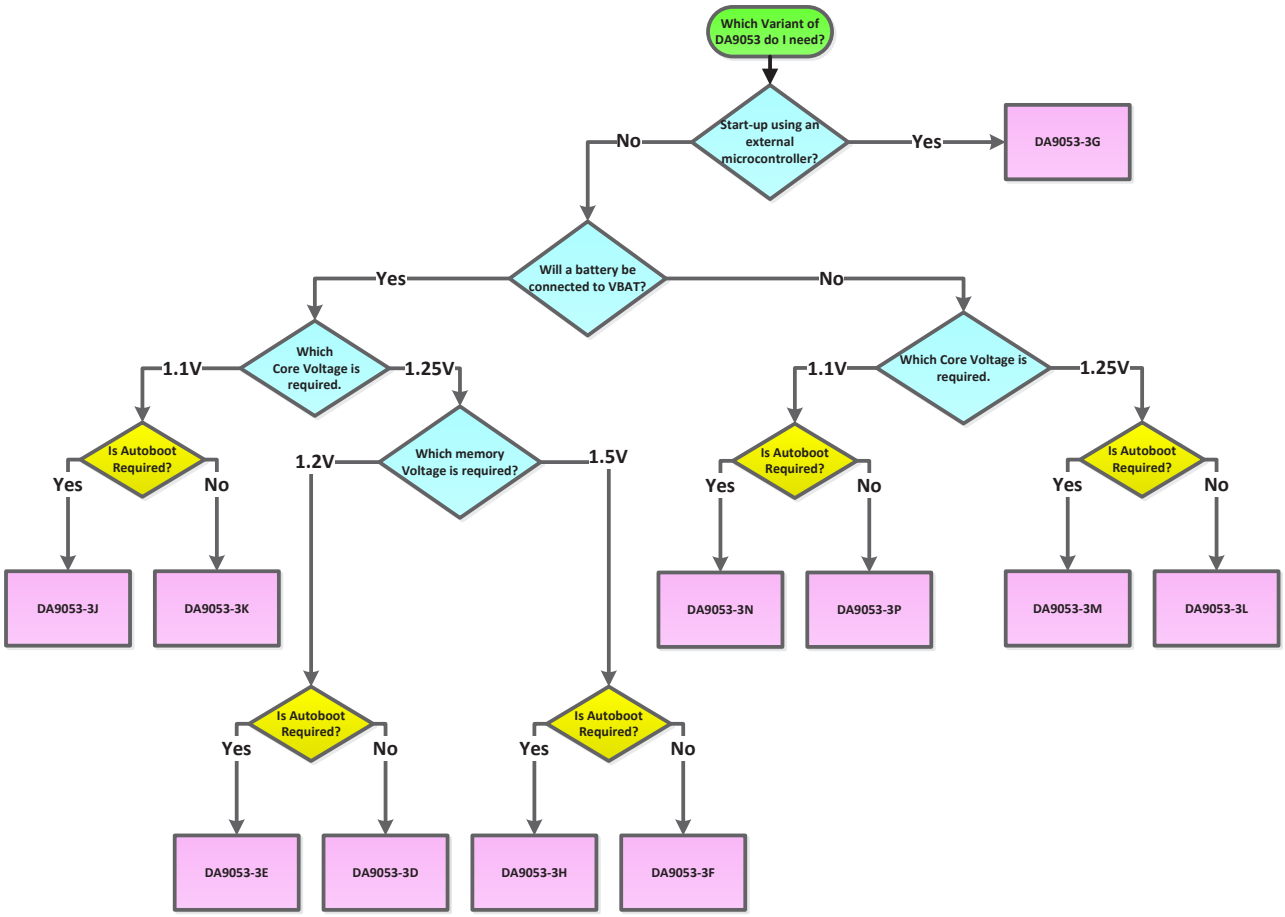
DA9053 Standard variant selection aid

Variant Features					Package availability (T&R codes shown**)		
Variant	Memory voltage	Auto-boot	Defined Sequence	Core Voltage	11x11 Automotive	11x11 Extended Temperature	7x7 Extended Temperature
DA9053-3D	1.20v LPDDR2	N	Y	1.25v		DA9053-3DHA2	DA9053-3DC52
DA9053-3E	1.20v LPDDR2	Y	Y	1.25v		DA9053-3EHA2	DA9053-3EC52
DA9053-3F	1.50v DDR3	N	Y	1.25v		DA9053-3FHA2	DA9053-3FC52
DA9053-3G	Set by external µController	Y	N	Set by external µController		DA9053-3GHA2	DA9053-3GC52
DA9053-3H	1.50v DDR3	Y	Y	1.25v		DA9053-3HHA2	DA9053-3HC52
DA9053-3J	1.50v DDR3	Y	Y	1.1v	DA9053-3JHA2-A	DA9053-3JHA2	
DA9053-3K	1.50v DDR3	N	Y	1.1v	DA9053-3KHA2-A	DA9053-3KHA2	
Optimised for batteryless operation							
DA9053-3L	1.50v DDR3	N	Y	1.25v		DA9053-3LHA2	DA9053-3LC52
DA9053-3M	1.50v DDR3	Y	Y	1.25v		DA9053-3MHA2	DA9053-3MC52
DA9053-3N	1.50v DDR3	Y	Y	1.1v	DA9053-3NHA2-A	DA9053-3NHA2	DA9053-3NC52
DA9053-3P	1.50v DDR3	N	Y	1.1v	DA9053-3PHA2-A	DA9053-3PHA2	DA9053-3PC52

Notes:

- ** for 11x11 trays replace HA2 with HA1, for 7x7 trays replace C52 with C51

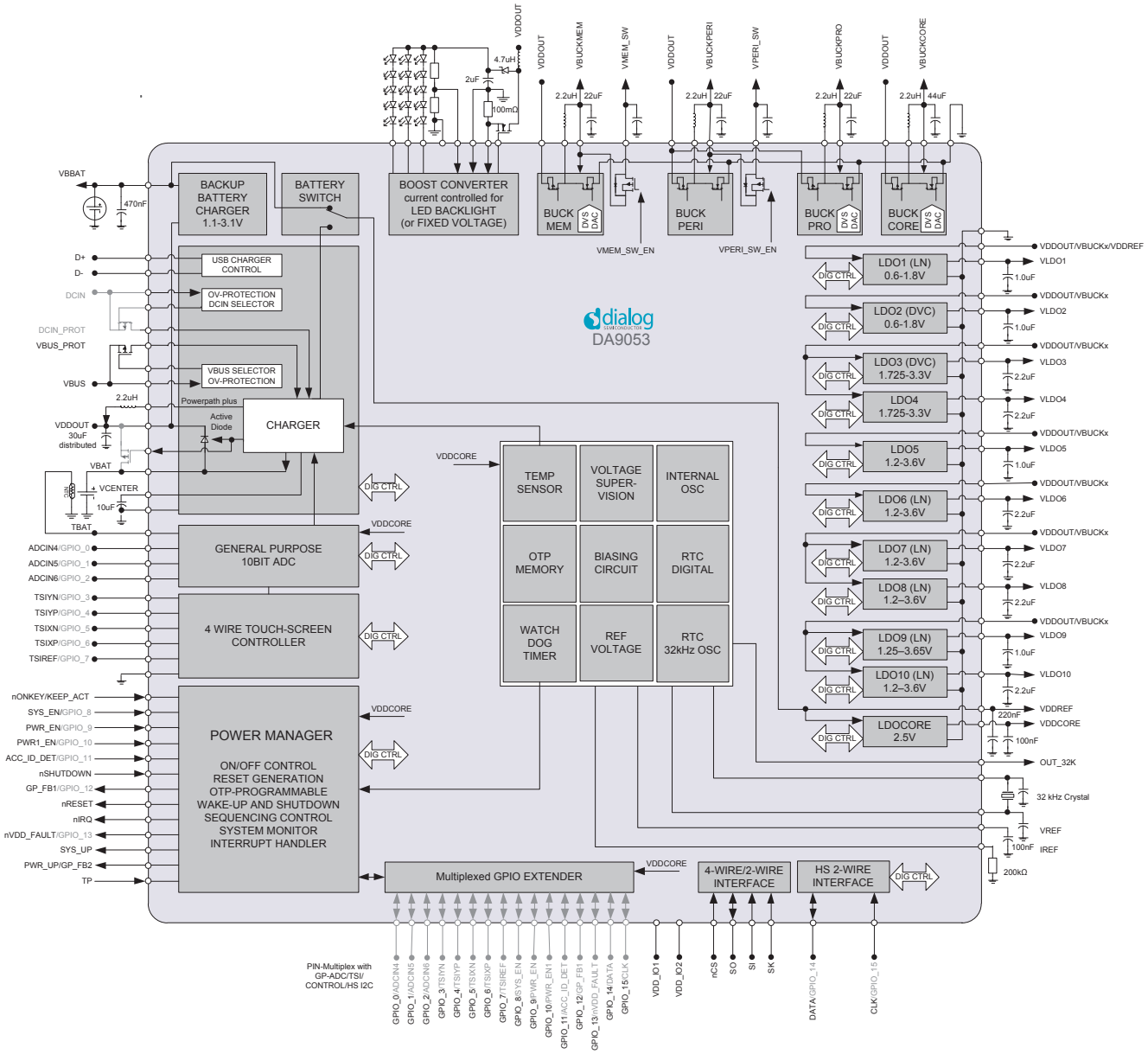
Regulator	Supplied pins	Supplied voltage	Supplied max. current	External Component	Notes
BUCKCORE	VBUCKCORE	0.5 – 2.075V ±3% accuracy	2000mA	2.2uH/47uF	DVC, 2MHz, 25mV steps, DVC ramp with controlled slew rate; pull-down resistor switch off
BUCKPRO	VBUCKPRO	0.5 – 2.075V ±3% accuracy	1000mA	2.2uH/22uF	DVC, 2MHz, 25mV steps, DVC ramp with controlled slew rate, , pull-down resistor switch off, common supply with BUCKPERI
BUCKMEM	VBUCKMEM; VMEM_SW	0.95 – 2.5V ±3% accuracy	1000mA	2.2uH/22uF	DVC, 2MHz, 25mV steps, DVC ramp with controlled slew rate; 2nd output with sequencer controllable switch, pull-down resistor switch off,
BUCKPERI	VBUCKPERI VPERI_SW	0.95 - 2.5V ±3% accuracy	1000mA	2.2uH/22uF	2MHz, 25mV steps 2nd output with sequencer controllable switch, common supply with BUCKPRO
BOOST	Ext. FET	5 to 25V, regulated via current feedback	50mA	4.7uH	Current controlled boost converter for 3 strings of up to 6 serial white LEDs. Over voltage protection via a voltage feedback pin.
LDO1	VLDO1	0.6 – 1.8V ±3% accuracy	40mA	1.0uF	High PSSR, low noise LDO, 50mV steps, pull-down resistor switch off
LDO2	VLDO2	0.6 – 1.8V ±3% accuracy	100mA	1.0uF	DVC, digital LDO, 25mV steps, DVC ramp with controlled slew rate, pull-down resistor switch off
LDO3	VLDO3	1.725 – 3.3V ±3% accuracy	200mA	2.2uF	DVC, digital LDO, 25mV steps, DVC with controlled slew rate, common supply with LDO4
LDO4	VLDO4	1.725 – 3.3V ±3% accuracy	150mA	2.2uF	Digital LDO, 25mV steps, optional HW control from GPI1, common supply with LDO3
LDO5	VLDO5	1.2 – 3.6V ±3% accuracy	100mA	1.0uF	Digital LDO, 50mV steps, pull-down resistor switch off, optional HW control from GPI2,
LDO6	VLDO6	1.2 – 3.6V ±3% accuracy	150mA	2.2uF	High PSRR, low noise, 50mV steps
LDO7	VLDO7	1.2 – 3.6V ±3% accuracy	200mA	2.2uF	High PSRR, low noise, 50mV steps, common supply with LDO8
LDO8	VLDO8	1.2 – 3.6V ±3% accuracy	200mA	2.2uF	High PSRR, low noise, 50mV steps, common supply with LDO7
LDO9	VLDO9	1.25 – 3.6V ±1% accuracy	100mA	1.0uF	High PSRR, low noise, 50mV steps, OTP trimmed, optional HW control from GPI12, common supply with LDO10
LDO10	VLDO10	1.2 – 3.6V ±3% accuracy	250mA	2.2uF	High PSRR, low noise, 50mV steps, common supply with LDO9
BACKUP	VBBAT	1.1 – 3.1V	6mA	470nF	100/200mV steps, configurable current limit between 100 and 6000uA, reverse current protection
LDOCORE	Internal PMIC supply	2.5V ±2% accuracy	4mA	100nF	Not for external use



Notes:

- After Start-up ,voltages and current limits may need to be modified by system software to configure for optimum performance with customer designs.
- GPIO pins will be configured to be in a safe state based on the Freescale designs
- Auto-boot devices start up automatically when power is applied
- Charging will be enabled by default at 4.1v @ 300mA, 60mA pre-charge, Charging automatically enabled if a Tbat resistor is detected, ADC set for 10k NTC
- The charger Buck is configured for 1800mA for DCIN and either 500mA or 100mA for VBUS. The CHG_USB_ILIM bit is set so that the state of pin D- with select either 100mA or 500mA. D- low will give 100mA setting. D- high will give a 500mA. D- can also be connected to a logical output from the USB phy to perform real USB detection
- The Charger is set with a 60 minute timeout and a 200mV drop before re-starting charging. These settings should allow charging to start and as soon as the host is alive the correct settings for the system should be applied
- All parts will now support Suspend resume mode operation if software and hardware allows
- The variant number is stored in GP_ID_0 (R133)
- The 3G variant enables a single LDO at first power up to enable the use of an extern PIC or micro controller to configure the full flexibility of the DA9053. This is intended for use in systems where a single fixed configuration is not optimal.

DA9053 Block Diagram



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