Off-Line Digital Power Controller for LED Driver with High Power Factor and Low-Ripple Current

1 Description

The iW3622 is a high performance, single-stage AC/DC power controller for LED luminaires with power factor (PF) correction. The device uses digital control technology to build unique control in PWM flyback/buck-boost power supplies to achieve high power factor while minimizing the LED current ripple. This distinctive control approach enables the capability for users to make trade-offs between the PF and LED current ripple in a single-stage design. It can achieve excellent LED current regulation over line and load variation, without the need for secondary feedback circuit. The built-in temperature sensor along with control logic can automatically adjust output current in real-time without visible flicker during the process. Alternatively, the external NTC thermistor is placed close to the hot spots in a design to provide thermal protection in the similar pattern by derating LED current. The iW3622 operates in quasi-resonant mode to provide high efficiency along with a number of key built-in protection features while minimizing the external component count, simplifying EMI design, and lowering the total bill of material cost. It also eliminates the need for loop compensation components while maintaining stability over all operating conditions.

Dialog's innovative proprietary technology maximizes the iW3622 performance in a tiny SOT-23 package. The iW3622 offers two multi-function pins allowing users to configure PF and LED current derating as required with no cost or size impact, thereby providing design flexibility. In addition to providing the temperature sensing via an NTC resistor, the MULTI pin also enables active start-up scheme to achieve the shortest possible start-up time without sacrificing active efficiency.

2 Features

- All-in-one non-dimmable low-cost off-line LED driver (isolated and non-isolated applications)
- Supports universal input voltage range ($90V_{AC}$ to $277V_{AC}$) and output power up to 45W
- High power factor (PF) with low current-ripple control technology
- User-configurable power factor setting (> 0.7 to > 0.95)
- Able to achieve low THD (< 20%)
- User-configurable internal or external over-temperature protection (OTP) with temperature-current derating
- Tight LED current regulation (±5%) across line and load, and within primary inductance tolerance (±20%)
- Isolated design without optocoupler
- Stabilized LED current-ripple control without visible shimmer or flicker
- Active start-up scheme enables fastest possible start-up
- 72kHz nominal PWM switching frequency with quasi-resonant operation
- ***EZ-EMI***™ design enhances manufacturability
- Built-in single-point fault protection features: LED open-/short-circuit protection and over-current protection
- No audible noise over entire operating range

3 Applications

- Solid-state LED lighting
- LED lighting ballast

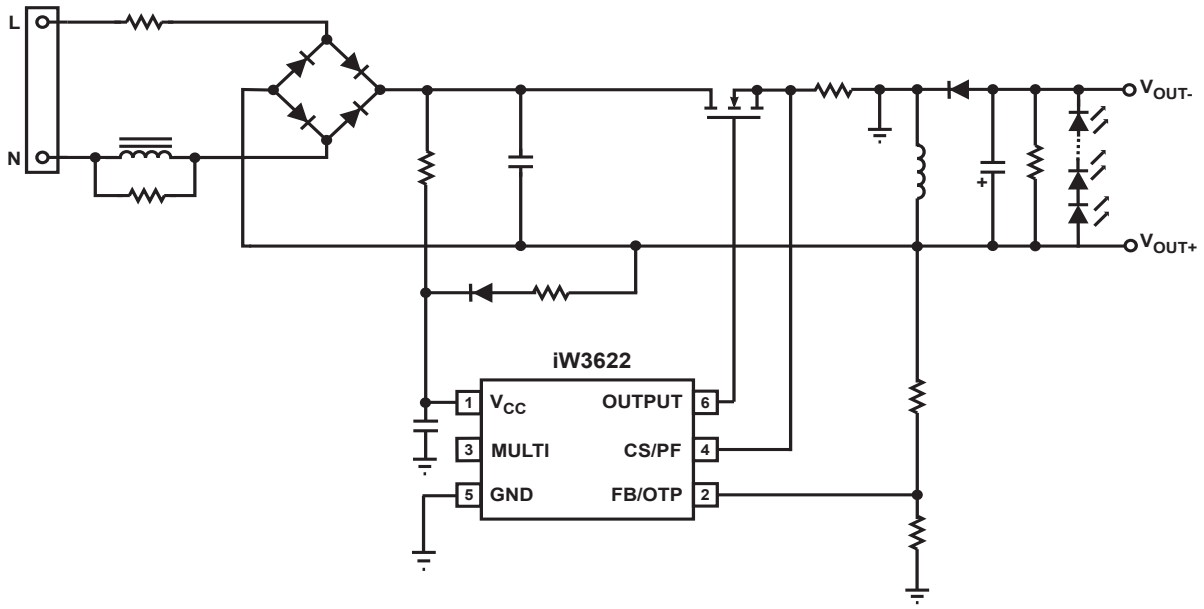


Figure 3.1 : iW3622 Typical Application Circuit (Non-Isolated Buck-Boost Application)

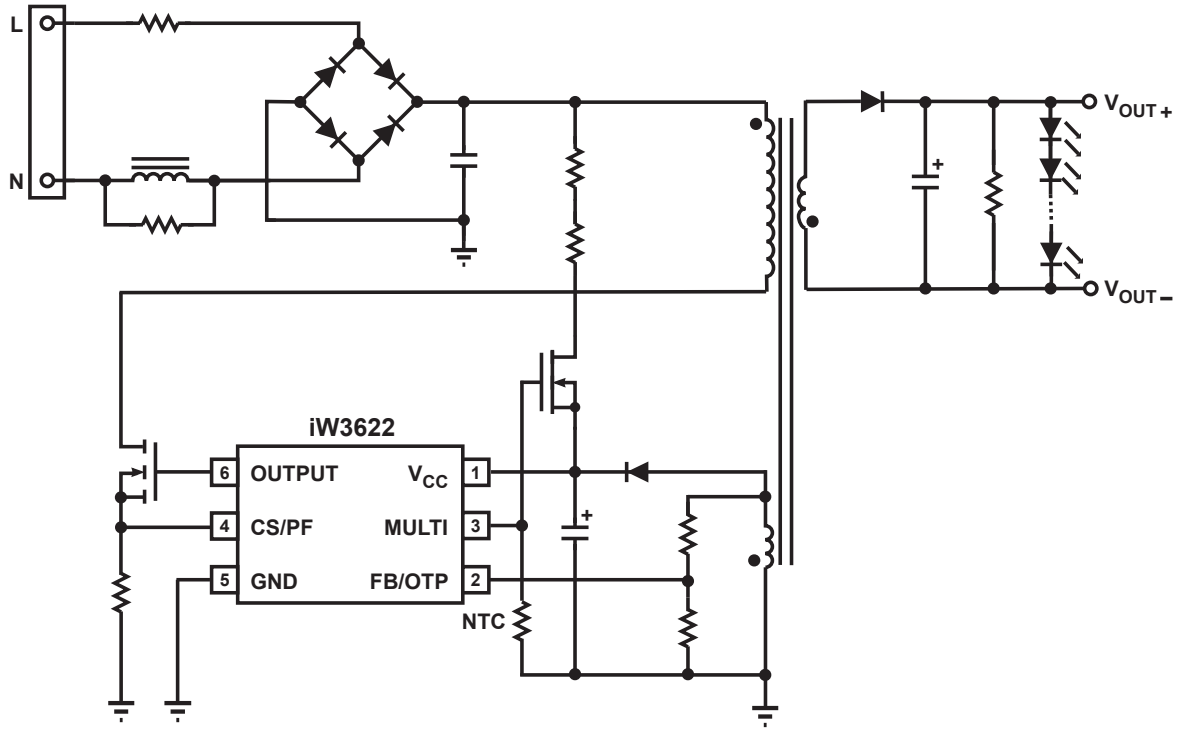


Figure 3.2 : iW3622 Typical Application Circuit (Isolated Flyback Application Using Active Start-up Device)

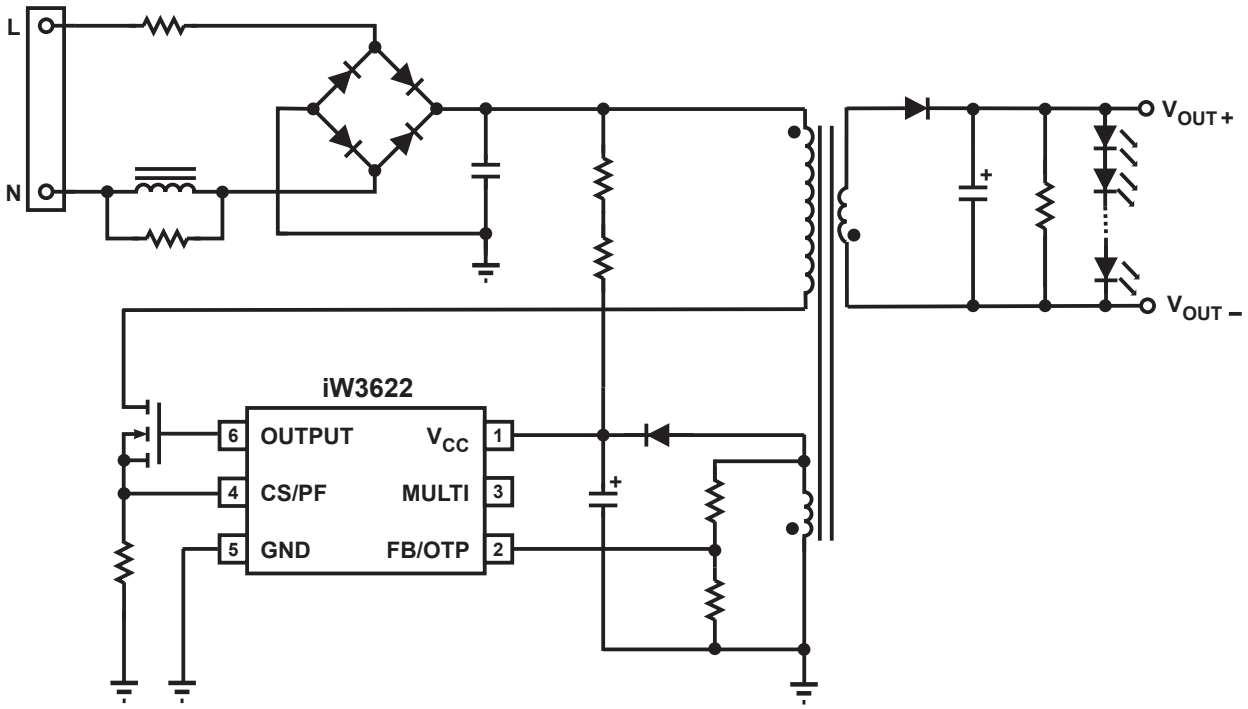


Figure 3.3 : iW3622 Typical Application Circuit (Isolated Flyback Application without Using Active Start-up Device)

4 Pinout Description

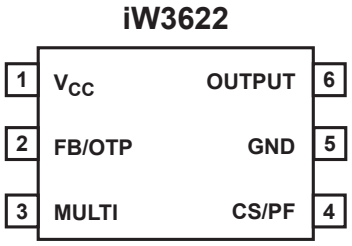


Figure 4.1 : 6-Lead SOT23 Package

Pin Number	Pin Name	Type	Pin Description
1	V_{CC}	Power Input	Power supply for control logic and MOSFET drive.
2	FB/OTP	Analog Input	Multi-function pin. Used for internal or external OTP current derating configuration at the beginning of start-up and to provide output voltage sense for primary regulation during normal operation.
3	MULTI	Output	Multi-function pin. Used to control active start-up device and for external temperature sensing via an NTC resistor.
4	CS/PF	Analog Input	Multi-function pin. Used for PF configuration at the beginning of start-up and to provide primary current sense for cycle-by-cycle peak current control and limit during normal operation.
5	GND	Ground	Ground.
6	OUTPUT	Output	Gate drive for external MOSFET switch.

5 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded. For maximum safe operating conditions, refer to Electrical Characteristics in Section 6.

Parameter	Symbol	Value	Units
DC supply voltage range (pin 1, I_{CC} = 20mA max)	V_{CC}	-0.3 to 18.0	V
Continuous DC supply current at V_{CC} pin (V_{CC} = 15V)	I_{CC}	20	mA
MULTI (pin 3)		-0.3 to 18.0	V
OUTPUT (pin 6)		-0.3 to 18.0	V
FB/OTP input (pin 2, $I_{FB/OTP} \leq$ 10mA)		-0.7 to 4.0	V
CS/PF input (pin 4)		-0.3 to 4.0	V
Maximum junction temperature	T_{JMAX}	150	°C
Operating junction temperature	T_{JOPT}	-40 to 150	°C
Storage temperature	T_{STG}	-65 to 150	°C
Thermal resistance junction-to-ambient	θ_{JA}	190	°C/W
ESD rating per JEDEC JS-001-2017		±2,000	V
Latch-up test per JESD78E		±100	mA

6 Electrical Characteristics

V_{CC} = 12V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
FB/OTP SECTION (Pin 2)						
Input leakage current	I_{BVS}	FB/OTP = 2V			1	µA
Nominal voltage threshold	$FB_{(NOM)}$	T_A = 25°C, negative edge	1.521	1.536	1.551	V
Output OVP threshold	$FB_{(OVP)}$	T_A = 25°C, negative edge		1.613		V
CS/PF SECTION (Pin 4)						
Overcurrent threshold	V_{OCP}			1.15		V
CS/PF regulation upper limit (Note 1)	$V_{IPK(HIGH)}$			1.00		V
CS/PF regulation lower limit (Note 1)	$V_{IPK(LOW)}$			0.25		V
Input leakage current	I_{LK}	CS/PF = 1.0V			1	µA
OUTPUT SECTION (Pin 6)						
Driver pull-down ON-resistance	$R_{DS(ON)PD}$			11		Ω
Driver pull-up ON-resistance	$R_{DS(ON)PU}$			16		Ω
Switching frequency (Note 2)	f_{SW}			72		kHz
V_{CC} SECTION (Pin 1)						
Maximum operating voltage (Note 1)	$V_{CC(MAX)}$				17	V
Start-up threshold	$V_{CC(ST)}$	V_{CC} rising		14.5		V
Undervoltage lockout threshold	$V_{CC(UVL)}$	V_{CC} falling		6.5		V
Start-up current	$I_{IN(ST)}$	V_{CC} = 10V		1.0		µA
Quiescent current	I_{CCQ}	V_{CC} = 14V, without driver switching		2.1		mA
Zener breakdown voltage	V_{ZB}	Zener current = 5mA T_A = 25°C		17.5		V
MULTI SECTION (Pin 3)						
Maximum operating voltage (Note 1)	$V_{MULTI(MAX)}$				17	V
NTC resistor current source (Note 3)	I_{OTP}			100		µA

Notes:

Note 1: These parameters are not 100% tested. They are guaranteed by design and characterization. Refer to Section 9.0 for operation details.

Note 2: Operating frequency varies based on the operating conditions. For further information, refer to Section 9.8.

Note 3: For product option with NTC OTP derating function only. This current is disabled for the other product option.

7 Typical Performance Characteristics

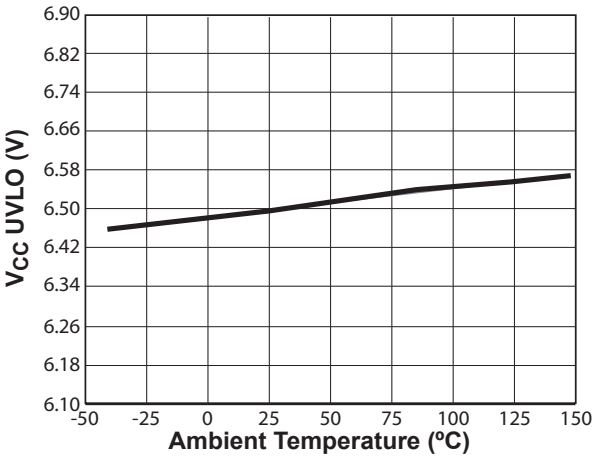


Figure 7.1 : V_{CC} UVLO vs. Temperature

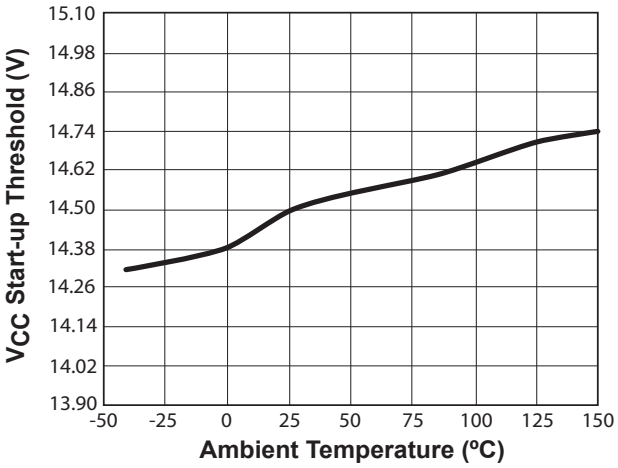


Figure 7.2 : Start-up Threshold vs. Temperature

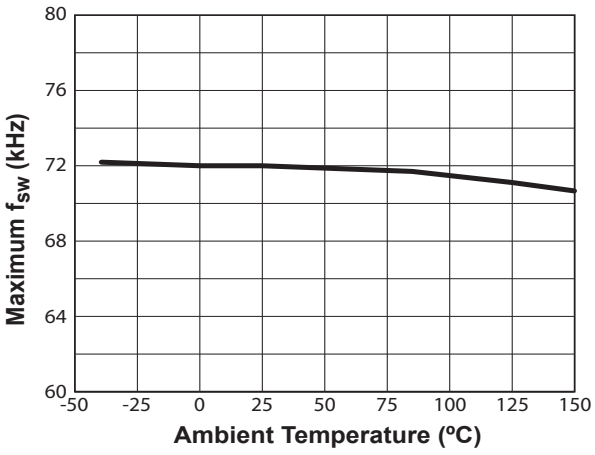


Figure 7.3 : Switching Frequency vs. Temperature

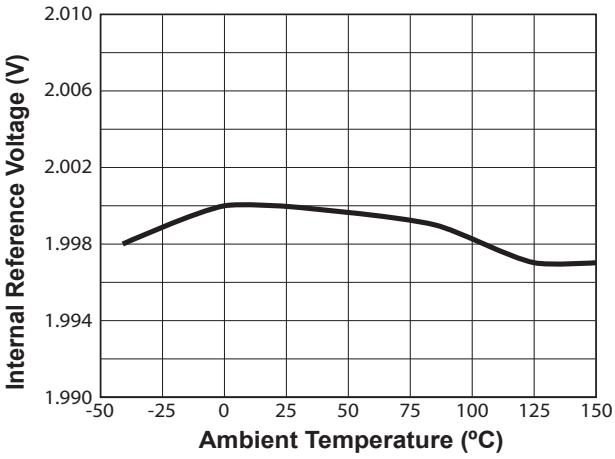


Figure 7.4 : Internal Reference vs. Temperature

Notes:

Note 1. Operating frequency varies based on the operating conditions; see Section 9.8 for more details.

8 Functional Block Diagram

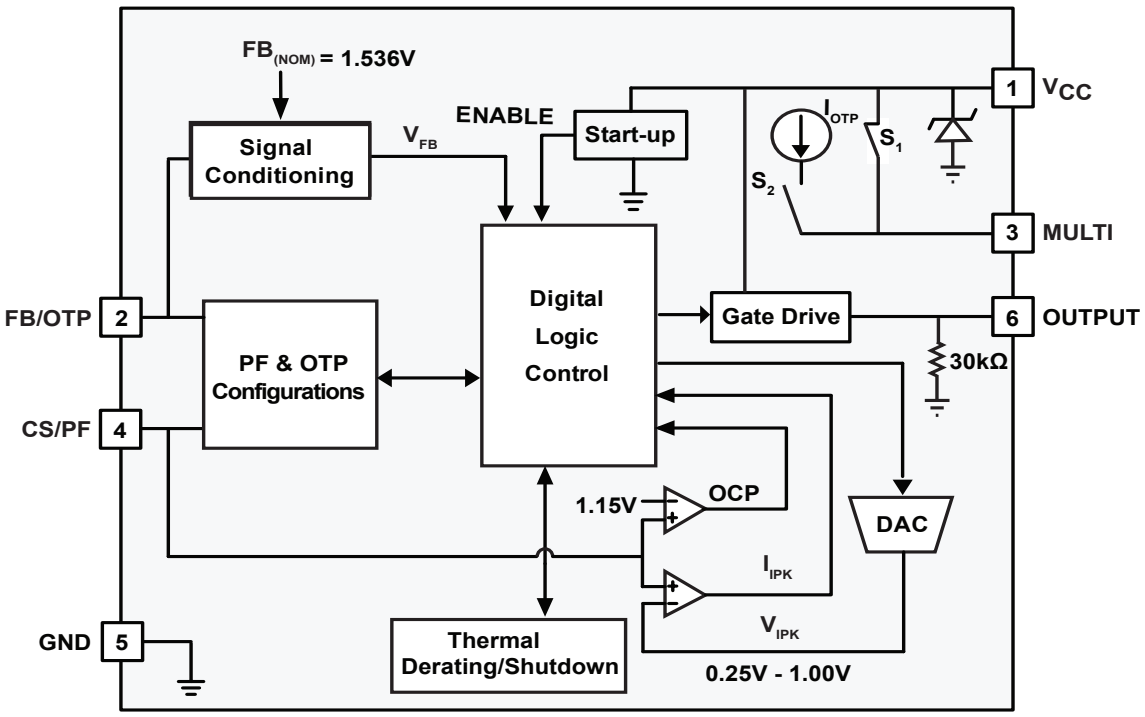


Figure 8.1 : iW3622 Functional Block Diagram

9 Theory of Operation

The iW3622 is a digital power controller dedicated for single-stage off-line LED driver with power factor correction. The device uses a new, proprietary primary-side control technology to eliminate the opto-isolated feedback and secondary regulation circuits required in traditional designs. This results in a low-cost small-size solution for LED lighting applications. The iW3622 uses a unique control approach in PWM flyback/buck-boost power supplies to achieve high power factor meanwhile minimizing LED current ripple. Furthermore, Dialog's digital control technology enables tight output current regulation, user-programmability to allow for making trade-offs between PF and LED current ripple, as well as full-featured circuit protection with primary-side control.

Referring to the block diagram in Figure 8.1, the iW3622 has CS/PF and FB/OTP pins for two-fold functions. At the beginning of start-up, a fixed current source flows out of the two pins alternatively, generating voltage levels proportional to resistance values from the pins to GND, which are then identified by the controller to set the requirement for PF and OTP respectively. During normal operation, the digital logic control block generates the switching on-time and off-time information based on the output voltage and current feedback signal and provides commands to control the external MOSFET. The CS/PF is an analog input configured to sense the primary current in a voltage form. In order to achieve the peak current mode control and cycle-by-cycle current limit, the internal V_{IPK} reference voltage sets the threshold for the CS/PF to compare with, and it varies in the range of 0.25V (typical) to 1.00V (typical) under different line and load conditions. With intelligent control approach, the iW3622 realizes high power factor correction with minimal output current ripple.

The iW3622 operates in quasi-resonant mode to provide high efficiency and simplify EMI design. In addition, the iW3622 incorporates a number of key built-in protection features, including LED short-circuit and open protections, over-current protection, and moreover, a distinctive temperature-current derating function in an attempt to maximize LED current under safe operating condition before initiating thermal shutdown. Using Dialog's state-of-the-art primary-feedback technology, the iW3622 removes the need for secondary feedback circuit while achieving excellent line and load regulation. Furthermore, the iW3622 eliminates the need for loop compensation components while maintaining stability over all operating conditions.

9.1 Pin Detail

Pin 1 – V_{CC}

Power supply for the controller during normal operation. The controller starts up when V_{CC} reaches 14.5V (typical) and shuts down when the V_{CC} voltage drops below 6.5V (typical) respectively. A decoupling capacitor of 0.1µF or so should be connected between the V_{CC} pin and GND.

Pin 2 – FB /OTP

Used to configure OTP setting at the beginning of start-up, and sense output during normal operation for output current regulation.

Pin 3 – MULTI

Multi-function pin. For NTC OTP derating enabled product option, connecting this pin to the gate of depletion NFET and connecting an NTC resistor between this pin and GND (See Figure 3.2) can control active start-up device and at the same time provide external temperature sensing. During startup, this pin voltage follows V_{CC} voltage to keep the depletion NFET conducting. After V_{CC} is charged above the start-up threshold $V_{CC(ST)}$, an internal current source of 100µA passes through the NTC resistor, generating a voltage low enough (3.3V maximum) to cut off the depletion NFET, meanwhile the voltage at this pin also reflects the NTC resistor temperature, which is used to provide OTP derating function during normal operation.

For the internal OTP derating enabled product option, a resistor of high resistance (e.g. 1MΩ) is recommended to connect from this pin to GND, to ensure the depletion NFET can be reliably turned off after start-up.

In case where the depletion NFET is not used, this pin can be left unconnected for both product options (see Figure 3.1).

It is not recommended to use NTC function without using the depletion NFET, since it requires low start-up resistors to generate enough V_{CC} charging current (after deducting the current to the NTC resistor). The depletion NFET can eliminate the loss on the resistors during normal operation.

Pin 4 – CS/PF

Used to configure PF setting at the beginning of start-up, and sense primary current during normal operation for cycle-by-cycle peak current control and limit.

Pin 5 – GND

Ground.

Pin 6 – OUTPUT

Gate drive for the external power FET switch.

9.2 Active Start-up and Adaptively Controlled Soft-Start

The iW3622 features a proprietary soft-start scheme to achieve fast build-up of output voltage and smooth ramp-up of LED current for a variety of output conditions including output voltage up to 100V above. In addition, the active start-up scheme enables shortest possible turn-on delay without sacrificing operating efficiency.

Refer to Figure 8.1 for the block diagram and Figure 3.2 for the active start-up circuit using external depletion NFET. Prior to start-up, the internal ENABLE signal is low, and the MULTI pin voltage is initially at zero-volt. The depletion NFET is turned on, and V_{CC} starts to ramp up. If the depletion NFET is selected with its threshold less than -1V, then V_{CC} can ramp up to 1V, when the internal switch S_1 is turned on. Consequently, the MULTI pin voltage closely follows the V_{CC} pin voltage, and the depletion NFET remains conducting, allowing the start-up current continuously to charge the V_{CC} bypass capacitor, as shown in Figure 9.1. When the V_{CC} bypass capacitor is charged to a voltage higher than the start-up threshold $V_{CC(ST)}$, the ENABLE signal becomes active and the iW3622 begins to perform PF and OTP configurations (See Section 9.3) followed by initial OTP check (See Section 9.13 and 9.14). Afterwards, the iW3622 commences soft-start function. The whole soft-start process can break down into several stages based on the output voltage levels, which is indirectly sensed by FB/OTP signal at the primary side. At different stages, the iW3622 adaptively controls the switching frequency and primary-side peak current such that the output voltage can always build up very fast at the early stages before LEDs light up, and smoothly transition to the desired regulation current level, meanwhile meeting the power factor requirement at steady-state operation.

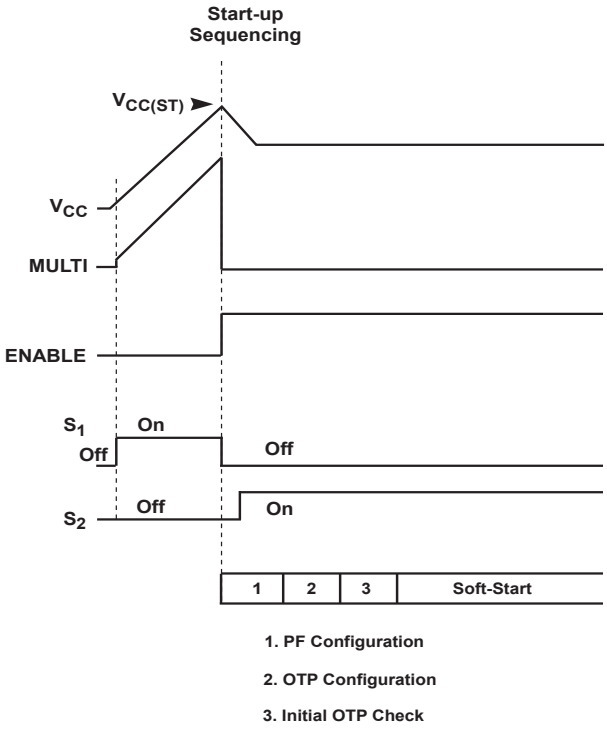


Figure 9.1 : Start-up Sequencing Diagram

While the ENABLE signal initiates the soft-start process, it turns off the switch S_1, and after a few µs or so it turns on switch S_2 to allow internal 100µA current passing through the NTC resistor, which generates a voltage less than 3.3V (maximum clamped voltage) to cut off the depletion NFET, thus minimizing the no-load standby power consumption and improving active operating efficiency.

If at any time the V_{CC} voltage drops below undervoltage lockout (UVLO) threshold $V_{CC(UVL)}$ then the iW3622 goes to shutdown. At this time the ENABLE signal becomes low, and S_1 is turned on, then the V_{CC} capacitor begins to charge up again towards the start-up threshold to initiate a new soft-start process.

In applications where the active start-up is not needed, the start-up resistor can be directly connected to the V_{CC} pin without using the active start-up device, and the MULTI pin can be left unconnected. Refer to Figure 3.1 for the application circuit.

9.3 PF and OTP Configurations

The iW3622 incorporates an innovative approach to allow users to configure PF and OTP current derating selections externally. In the iW3622, power factor can be set to four levels externally in order to trade off with LED current ripple, as shown in Table 9.1. In addition, for the over-temperature protection, depending on whether it is internal or external, either the temperature at which the device starts to derate LED current or the derating step-size can also be set at the configuration stage.

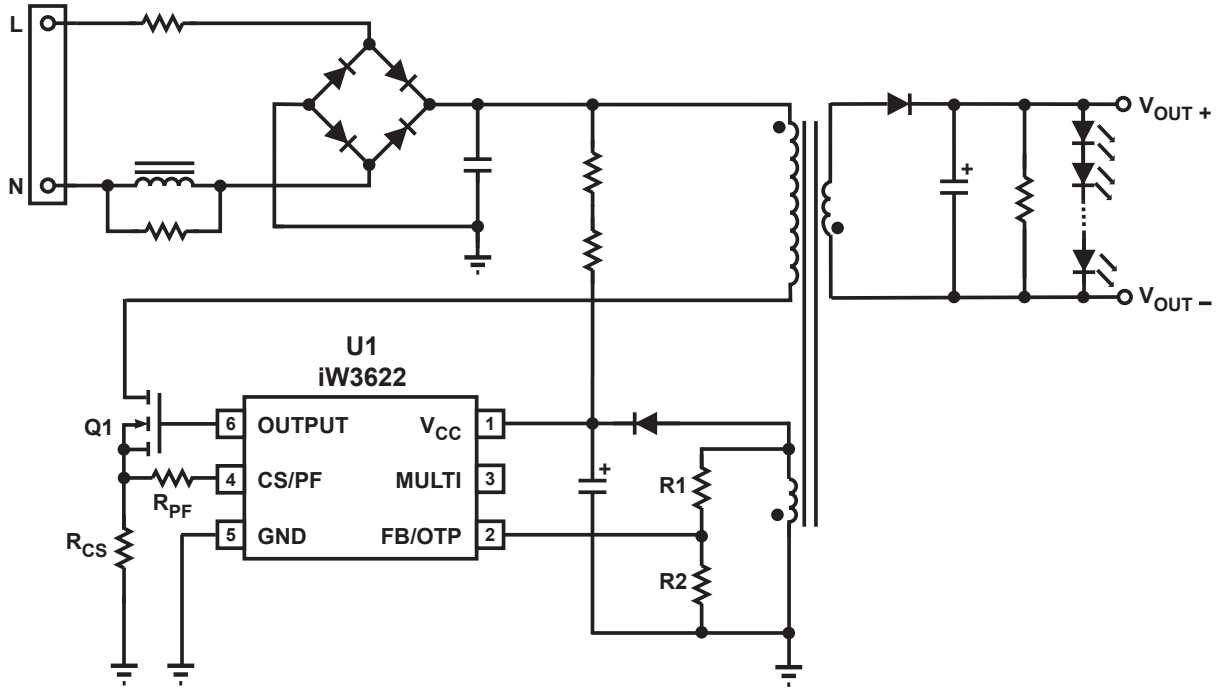


Figure 9.2 : Typical Application Circuit Highlighting Configuration Resistors

The configurations of PF and OTP derating are only performed once after the ENABLE signal becomes active, and completed before the soft-start commences. The configurations involve CS/PF and FB/OTP pins and some resistors connected to the pins. Figure 9.2 shows the schematic highlighting the resistors used for configurations. During PF configuration, the iW3622 does not send out any drive signal at OUTPUT pin, and the switch Q1 remains in off-state. A fixed current flows out of CS/PF pin, which generates a voltage proportional to the resistance value of R_{PF} and R_{CS} (in series). The internal digital control block identifies the resistance value between CS/PF pin to ground, and then sets the control algorithm accordingly. Table 9.1 lists the resistance range of R_{PF} for configuring four-level of PF.

In applications, the selection of R_{PF} and R_{CS} is straight-forward. R_{CS} is usually small and its resistance is negligible compared to R_{PF} in determining PF level during configuration. However, it directly sets output current, whereas R_{PF} does not play a role (See Section 9.5). Therefore, the values of R_{PF} and R_{CS} can be determined separately.

Following the completion of configuring PF, the iW3622 enters the stage of configuring OTP derating selection. During this stage, switch Q1 still remains in off-state, and the fixed current flows out of FB/OTP pin and generates a voltage proportional to the paralleled resistance of R1 and R2, since the bias winding is virtually shorted. Consequently, the paralleled resistance of R1 and R2 is identified and used to set the OTP derating levels. Meanwhile, during normal operation, the FB/OTP pin reflects output voltage in real-time. The ratio of R1 to R2 sets nominal output voltage, which represents the voltage level the iW3622 attempts to regulate to during constant voltage operation. Based on the two equations, R1 and R2 can be readily derived.

The iW3622 provides 3-level OTP derating selections. Table 9.2 lists the resistance range of paralleled R1 and R2 for each configuration level. Note, the OTP level has different meaning for the external NTC-based and internal junction-based OTP derating. For the NTC-based OTP derating, the OTP level corresponds to different step-size of OTP derating. For the internal-based OTP derating, it corresponds to the temperature at which the iW3622 starts to derate output current. Refer to Sections 9.13 and 9.14 for details.

In practice, for both PF and OTP configurations, it is recommended that the resistance be selected in the middle of the range where possible.

After completing PF and OTP configurations, the iW3622 performs an initial OTP check, and it initiates a soft-start process if the junction temperature is below 130°C (typical) for product options with internal OTP protection, or the MULTI pin voltage is above 0.84V for product options with external OTP protection.

PF Level	1	2	3	4
R_{PF} Range* (kΩ)	0 - 0.88	1.36 – 3.00	3.87 – 5.60	6.95 – 20
Resulting PF**	> 0.9	> 0.95	> 0.7	< 0.7

* R_{CS} is usually very small (a few Ohms or less), and can be neglected compared to R_{PF} in consideration.

** The data are from typical designs. Level 4 is intended to mitigate LED line-frequency ripple current with big input bulk capacitance. Level 1 is recommended for better current regulation and current ripple while still satisfying PF/THD requirements.

Table 9.1: Recommended resistance range to set power factor (PF) level

	OTP Level	1	2	3
	Paralleled R1 and R2 Range (kΩ)	1.80 – 2.25	2.97 – 3.78	4.78 – 20
NTC OTP Derating	Derating Step-Size	5%	7.5%	10%
Internal OTP Derating	The temperature at which the iW3622 starts to derate output current	100°C	110°C	120°C

Table 9.2: Recommended resistance range for over-temperature protection (OTP) selection

9.4 Understanding Primary Feedback

Figure 9.3 illustrates a simplified flyback converter (a similar concept also applies to the buck-boost converter). When the switch Q1 conducts during $t_{ON}(t)$, the current $i_g(t)$ is directly drawn from rectified sinusoid $v_g(t)$. The energy $E_g(t)$ is stored in the magnetizing inductance L_M. The rectifying diode D1 is reverse biased and the load current I_O is supplied by the secondary capacitor C_O. When Q1 turns off, D1 conducts and the stored energy in the inductor is delivered to the output.

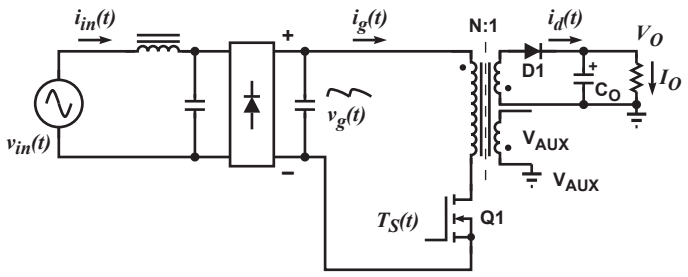


Figure 9.3 : Simplified Flyback Converter

In order to tightly regulate the output voltage, the information about the output voltage and load current need to be accurately sensed. In the DCM flyback converter, this information can be read via the auxiliary winding or the primary magnetizing inductance (L_M). During the Q1 on-time, the load current is supplied from the output filter capacitor C_O.

The voltage across L_M is $v_g(t)$, assuming the voltage dropped across Q1 is zero. The current in Q1 ramps up linearly at a rate of:

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_M} \qquad (9.1)$$

At the end of on-time, the current has ramped up to:

$$i_{g\_peak}(t) = \frac{v_g(t) \times t_{ON}}{L_M} \qquad (9.2)$$

This current represents a stored energy of:

$$E_g = \frac{L_M}{2} \times i_{g\_peak}(t)^2 \qquad (9.3)$$

When Q1 turns off at t_O, $i_g(t)$ in L_M forces a reversal of polarities on all windings. Ignoring the communication-time caused by the leakage inductance L_K at the instant of turn-off t_O, the primary current transfers to the secondary at a peak amplitude of:

$$i_d(t) = \frac{N_P}{N_S} \times i_{g\_peak}(t) \qquad (9.4)$$

Assuming the secondary winding is master, and the auxiliary winding is slave,

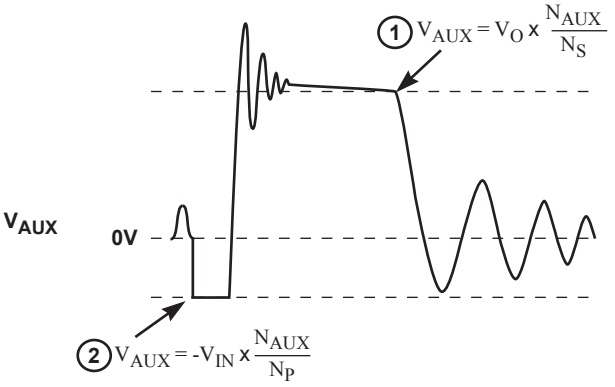


Figure 9.4 : Auxiliary Voltage Waveforms

The auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}}{N_S}(V_O + \Delta V) \qquad (9.5)$$

and reflects the output voltage as shown in Figure 9.4.

The voltage at the load differs from the secondary voltage by a diode drop and IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage is a fixed ΔV. Furthermore, if the voltage can be read when the secondary current is small, ΔV is also small. With the iW3622, ΔV can be ignored.

The real-time waveform analyzer in the iW3622 reads this information cycle by cycle. The part then generates a feedback voltage V_{FB}. The V_{FB} signal precisely represents the output voltage under most conditions and is used to regulate the output voltage.

9.5 Constant Current Operation

The iW3622 employs a patented primary-side-only technology to regulate output current. It senses the load current indirectly through the primary current. The primary current is detected by the CS/PF pin through a resistor from the MOSFET source to ground.

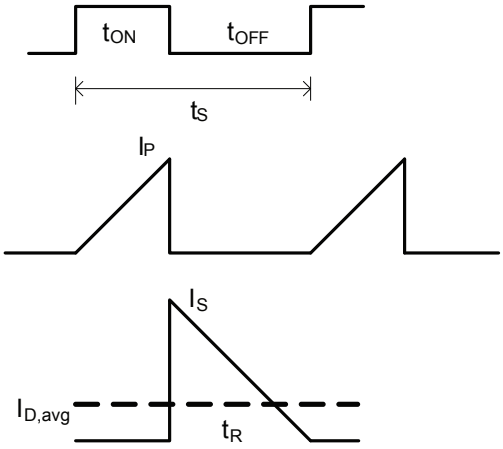


Figure 9.5 : Constant Current Operation

The cycle-by-cycle averaged current of the secondary diode current is determined by:

$$I_{D,avg} = \frac{1}{2} \times N_{PS} \times \frac{V_{IPK}}{R_{CS}} \times \frac{t_R}{t_S} \qquad (9.6)$$

where, N_{PS} is transformer primary-to-secondary turns-ratio; R_{CS} is the resistance connecting from CS/PF pin to Ground.

In the iW3622, the current $I_{D,\,avg}$ is controlled on a cycle-by-cycle basis in order to achieve high PF and ensure good current regulation, while avoiding continuous conduction mode operation.

During constant current (CC) operation, the output voltage regulation is not guaranteed. The point 1 in Figure 9.4, which reflects output voltage is not regulated to $FB_{(NOM)}$ (i.e. 1.536V). For LED applications, where current regulation is critical, design needs to ensure the point 1 is well below $FB_{(NOM)}$ with some margin.

9.6 Constant Voltage Operation

The iW3622 also incorporates a loose constant voltage (CV) operation, which mainly provides a cushion for LED open protection. In the iW3622, when input voltage has small ripple content because of adopting large input capacitor (e.g. selecting PF level to 4), the output voltage can remain fairly constant by regulating the point 1 as indicated in Figure 9.4 (1.536V typically). In the case of other PF level selections, the input voltage has large ripple content. Under this condition, the averaged output voltage can stay constant, however, a good PF/THD may not be guaranteed.

During constant voltage operation, the iW3622 may operate in pulse-width-modulation (PWM) mode or pulse-frequency-modulation (PFM) mode, depending on load conditions. In particular, the iW3622 allows the switching frequency to drop as low as 275Hz at PFM mode, which helps system stay regulated at very light load condition, thus improving active operating efficiency by using large pre-load resistor.

Figure 9.6 shows power envelope for the iW3622. After soft-start is completed, the digital control block measures the output conditions. It determines output power levels and adjusts the control system to operate either in CV mode or CC mode.

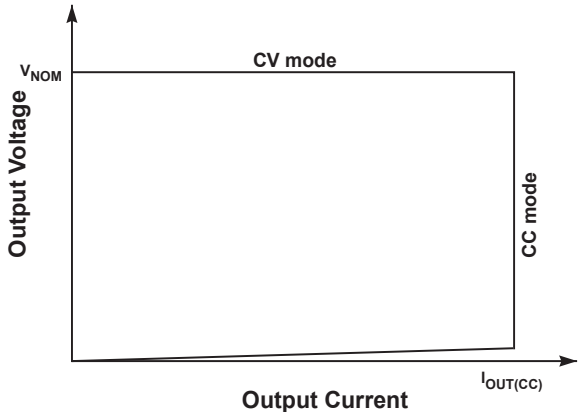


Figure 9.6 : Power Envelope

For LED applications, care is needed to select R1 and R2 (in Figure 9.2), such that CV voltage is above the targeting LED string voltage and the iW3622 can thus run in CC mode for good current regulation and high PF.

9.7 LED Current Line Regulation

The iW3622 also provides a way to tune LED current regulation across line voltages. In Figure 9.7, the resistor R_{PF} used to configure power factor setting can also be used to compensate for LED current difference over line voltages. To tune the current, one capacitor C_{CMP} may be needed in order to generate a proper delay formed by R_{PF} and C_{CMP}, which leads to a gradual increment in LED current as line voltage increases.

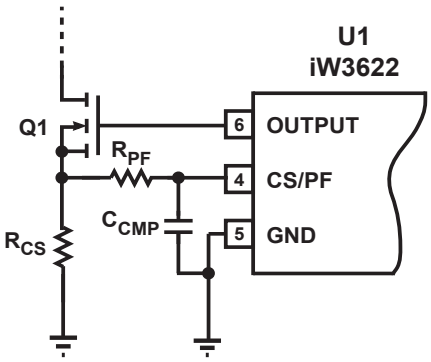


Figure 9.7 : Compensation for LED Current

9.8 Variable Frequency Operation Mode

During each of the switching cycles, the falling edge of FB/OTP is checked. If the falling edge of FB/OTP is not detected, the off-time is extended until the falling edge of FB/OTP is detected. This results in the variable switching frequency operation. In particular, for constant current operation, the maximum switching frequency is below 72kHz for PF levels of 2 to 4; however, for PF level 1, during the portion of high instantaneous input voltage, the switching frequency can go above 72kHz. Additionally, in constant voltage operation, the switching frequency in PFM mode can be reduced as low as 275Hz at very light load to improve operating efficiency.

In the iW3622, the maximum allowed transformer reset time is 110µs. When the transformer reset time reaches 100µs, the iW3622 shuts off.

9.9 Quasi-Resonant Switching

The iW3622 also incorporates a unique proprietary quasi-resonant switching scheme that achieves valley-mode turn on for every switching cycle. In valley mode switching, the MOSFET switch is turned on at the point where the resonant voltage across the drain and source of the MOSFET is at its lowest point (see Figure 9.8). By switching at the lowest V_{DS}, the switching loss is minimized.

Turning on at the lowest V_{DS} generates lowest dV/dt, thus valley mode switching can also reduce EMI. Due to the nature of quasi-resonant switching, the actual switching frequency can vary slightly cycle by cycle, providing the additional benefit of reducing EMI.

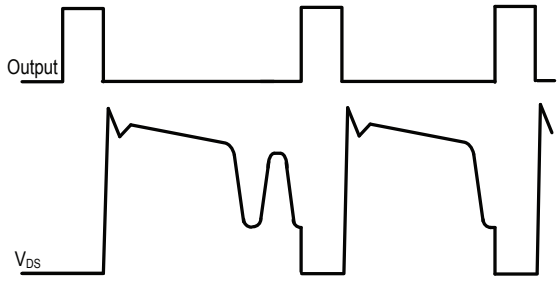


Figure 9.8 : Valley Mode Switching

9.10 Internal Loop Compensation

The iW3622 incorporates an internal Digital Error Amplifier with no requirement for external loop compensation. For a typical power supply design, the loop stability is guaranteed to provide at least 45º of phase margin and -20dB of gain margin.

9.11 LED Open and Short Protections

The constant voltage operation in the iW3622 provides protection against LED open fault. During normal operation, the iW3622 operates in CC mode with the output voltage below the nominal voltage set by $FB_{(NOM)}$. After LED is open, the output voltage is pushed higher momentarily. Depending on the output capacitor and LED operating current, system may gradually settle down and stay regulated at constant voltage operation at no-load condition. Or, if the output voltage overshoot exceeds the output OVP threshold set by $FB_{(OVP)}$ in Section 6, the iW3622 shuts down.

LED short fault is detected via FB/OTP pin. When the point 1 in Figure 9.4 is below 115mV for several consecutive cycles, the iW3622 shuts down.

When any of these faults are met the IC remains biased to discharge the V_{CC} supply. Once V_{CC} drops below UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting start-up until the fault condition is removed.

9.12 PCL, OCP and SRS Protection

Peak-current limit (PCL), over-current protection (OCP) and sense-resistor-short protection (SRSP) are features built into the iW3622. With the CS/PF pin the iW3622 is able to monitor the peak primary current. This allows for cycle-by-cycle peak current control and limit. When the peak primary current multiplied by the CS/PF resistor is

greater than 1.15V, over-current is detected and the IC immediately turns off the output driver until the next cycle. The output driver sends out a switching pulse in the next cycle, and the switching pulse continues if the OCP threshold is not reached; or, the switching pulse turns off again if the OCP threshold is reached. If the OCP occurs for several consecutive switching cycles, the iW3622 shuts down.

If the CS/PF resistor is shorted there is a potential danger that over-current condition may not be detected. Thus, the IC is designed to detect this sense-resistor-short fault during start-up and shut down immediately. The V_{CC} is discharged since the IC remains biased. Once V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting to start-up, but does not fully start-up until the fault condition is removed.

9.13 Internal OTP and Current-Derating

The iW3622 incorporates a distinctive internal over-temperature protection (OTP) with current-derating function. Before the soft-start process is initiated, the part first checks the junction temperature. If the junction temperature is above 130°C, then the system does not start up. Once the part starts up, the thermal shutdown temperature becomes 150°C. However, during normal operation, before the junction temperature reaches 150°C, the part firstly derates output current in the predetermined steps in an attempt to reach thermal equilibrium before thermal shutdown kicks in. In this way, the part stays in a safe operation meanwhile maximizing output current.

Figure 9.9 shows output current derating function. In this example, the LED current starts to derate output current when the junction temperature hits 100°C and continues to derate the current if it hits next derating temperature thresholds such as 110°C, 120°C, 130°C. For each derating, the output current drop is roughly 7% of the nominal operating current. In addition, each derating step consists of a couple of small steps taking place in several seconds. In this way, the output current drops gradually, so that there is no visual observation of any flicker during current derating process.

In the iW3622's derating function, a 10°C hysteresis is built in for each derating step. For example, after the junction temperature hits 100°C, the output current drops by roughly 7%. Afterwards, if the junction temperature is stabilized in the range from 90°C to 110°C (with both temperatures excluded), no action takes place; however if the junction temperature drops below 90°C, then output current starts to ramp up in an opposite way as derating to reach previous level of output curent.

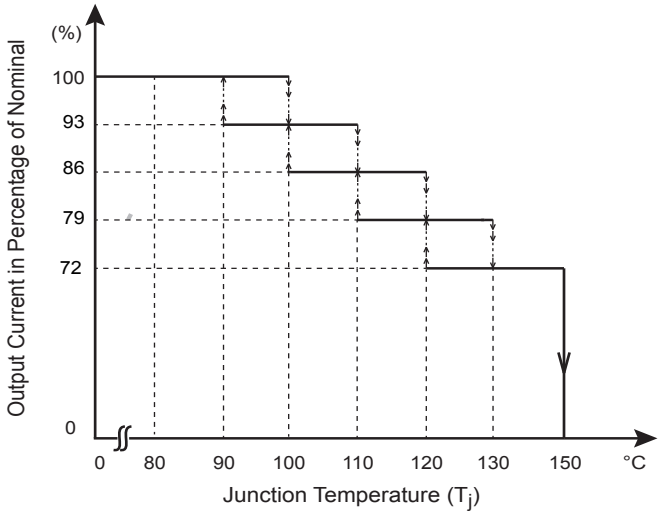


Figure 9.9 : Internal OTP Thermal Derating

For different applications, there may be a need to derate output current starting at different temperature. This can be done in the iW3622 by configuring it to three different levels via FB/OTP pin. Refer to Section 9.3 for details.

9.14 External OTP and Current-Derating

Alternatively, the iW3622 also has a product option that uses an NTC resistor to sense external temperature and provide similar current-derating function, as shown in Figure 9.10. During normal operation, the internal current source of 100µA passes through the NTC resistor and generates a voltage, proportional to NTC resistance. As the NTC resistance varies as a function of temperature at which it is exposed to, the resulting voltages across NTC resistor reflect different temperatures. In Figure 9.10, the numbers in the abscissa represent the voltages across the NTC resistor, via which, the external temperature information can be extracted for a given NTC resistor.

The operation of external OTP and current derating is similar to that of the internal OTP derating in Section 9.13. The iW3622 starts to derate output current when the voltage across the NTC resistor hits corresponding thresholds. Similarly, the iW3622 retains hysteresis for each derating, and each derating step-size is determined during the configuration stage, as shown in Table 9.2. Note the device shuts down when the NTC resistor voltage is below 0.54V, and it can only start up when the voltage is above 0.84V.

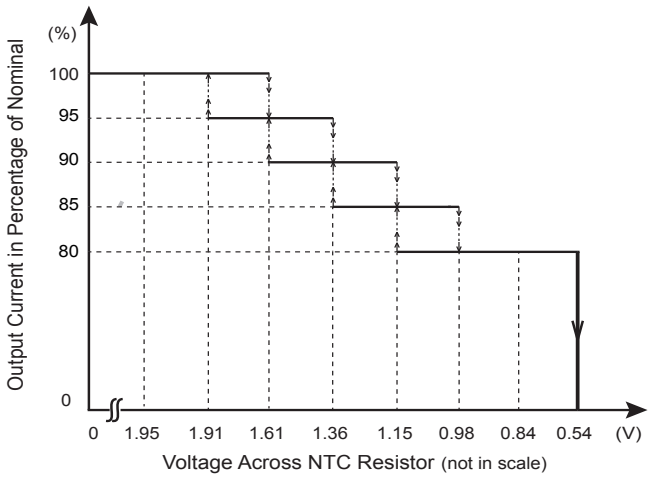
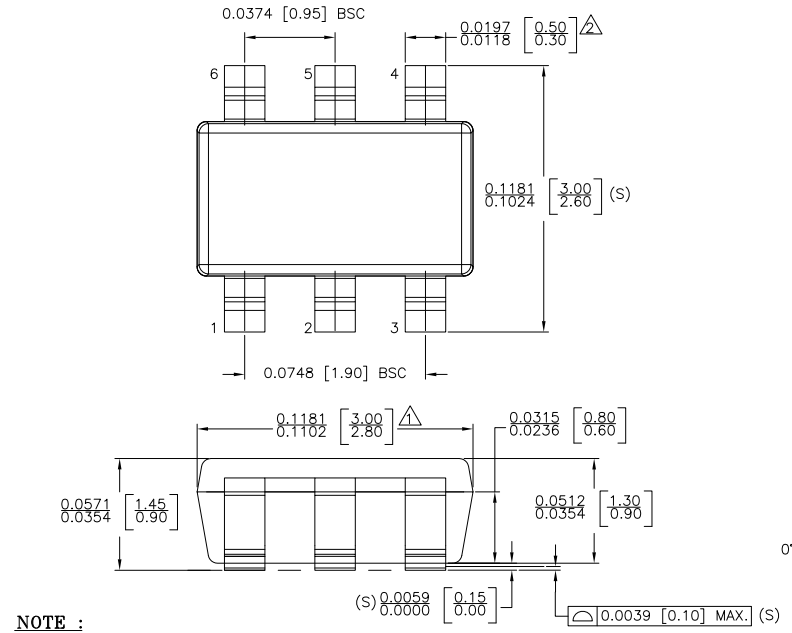
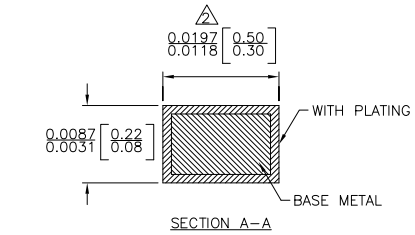
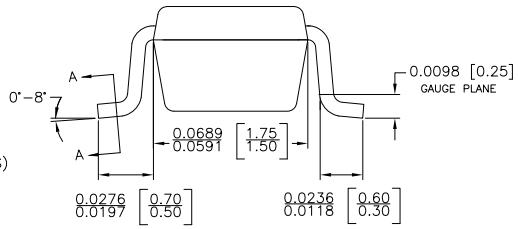


Figure 9.10 : External OTP Thermal Derating

10 Physical Dimensions





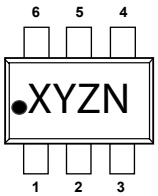


NOTE :

1. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.127 MM PER SIDE.
2. DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.127 MM PER SIDE.
3. DIE IS FACING UP FOR MOLD.DIE IS FACING DOWN FOR TRIM/FORM.
4. THIS PART IS COMPLIANT WITH EIAJ SPECIFICATION SC74A AND JEDEC SPECIFICATION MO–178AB.
5. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERISTIC.(S)
6. CONTROLLING DIMENSIONS IN INCHES. [mm]

STATUS: RELEASED	SCALE: DO NOT SCALE
TERMINAL FINISH: 100% Sn or NiPdAu (PPF)	
TITLE: 6 SOT23 PACKAGE OUTLINE	
REV: A	REVISION NOTE: NEW DRAWING — DATE: 02–MAR–2015

SOT23-6 devices are marked with a 4-digit code. Orientation of Pin 1 is shown below:



11 Ordering Information

Part Number	Description	Package	Description
iW3622-00	Internal OTP derating, 72kHz switching frequency	SOT-23	Tape & Reel[1]
iW3622-01	NTC OTP derating, 72kHz switching frequency	SOT-23	Tape & Reel[1]

Note 1: Tape & Reel packing quantity is 3,000/reel. Minimum packing quantity is 3,000.

Off-Line Digital Power Controller for LED Driver with High Power Factor and Low-Ripple Current

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