DIGITRON™ Semiconductors

High-reliability discrete products
and engineering services since 1977

IRFF130

N- CHANNEL MOSFET

FEATURES

- Available as “HR” (high reliability) screened per MIL-PRF-19500, JANTX level. Add “HR” suffix to base part number.
- Available as non-RoHS (Sn/Pb plating), standard, and as RoHS by adding “-PBF” suffix.

MAXIMUM RATINGS.

Rating	Symbol	Value	Unit
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to +150	°C
Thermal Resistance Junction To Case	$R_{\theta JC}$	5.0	°C/W
Total Power Dissipation @ T_A = 25°C **Derate above 25°C** (1)	P_D	0.8 25	W mW/°C
Drain Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current @ T_C = +25°C (2)	I_{D1}	8.0	A
Drain Current @ T_C = +100°C (2)	I_{D2}	5.0	A
Off State Current(Peak Total Value) (3)	I_{DM}	32	A(pk)
Source Current	I_S	8.0	A

Note 1: Derate linearly 0.2W/°C for T_C > +25°C

Note 2: The following formula derives the maximim theoretic I_D limit. I_D is also limited by poackage and internal wires and may be limited due to pin diameter.

$$I_D = \sqrt{\frac{T_{J(max)} - T_C}{R_{\theta JC} \times R_{DS(on)} @ T_{J(max)}}}$$

Note 3: I_{DM} = 4 x I_{D1} as calculated in Note 2

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage V_{GS} = 0V, I_D = 1.0mA	$V_{(BR)DSS}$	100	-	V
Gate-Source Voltage (Threshold) $V_{DS} \geq V_{GS}$. I_D = 0.25mA $V_{DS} \geq V_{GS}$. I_D = 0.25mA, T_J = +125°C $V_{DS} \geq V_{GS}$. I_D = 0.25mA, T_J = -55°C	 $V_{GS(th)1}$ $V_{GS(th)2}$ $V_{GS(th)3}$	 2.0 1.0 -	 4.0 - 5.0	V
Gate Current V_{GS} = ±20V, V_{DS} = 0V V_{GS} = ±20V, V_{DS} = 0V, T_J = +125°C	 I_{GSS1} I_{GSS2}	 - -	 ±100 ±200	nA
Drain Current V_{GS} = 0V, V_{DS} = 80V	I_{DSS1}	-	25	µA
Drain Current V_{GS} = 0V, V_{DS} = 80V, T_J = +125°C	I_{DSS2}	-	0.25	mA
Forward Transconductance V_{DS} = 15V, I_{D2} = 5.0A	G_{fs}	3.0	-	S
Static Drain-Source On-State Resistance V_{GS} = 10V, I_D = 5.0A pulsed	$r_{DS(on)1}$	-	0.18	Ω
Static Drain-Source On-State Resistance V_{GS} = 10V, I_D = 8.0A pulsed	$r_{DS(on)2}$	-	0.195	Ω
Static Drain-Source On-State Resistance T_J = 125°C V_{GS} = 10V, I_D = 5.0A pulsed	$r_{DS(on)1}$	-	0.35	Ω
Diode Forward Voltage V_{GS} = 0V, I_D = 8.0A pulsed	V_{SD}	-	1.5	V

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
DYNAMIC CHARACTERISTICS				
On-State Gate Charge V_{GS} = 10V, I_D = 8.0A, V_{DS} = 50V	$Q_{g(on)}$	-	28.51	nC
Gate to Source Charge V_{GS} = 10V, I_D = 8.0A, V_{DS} = 50V	Q_g	-	6.34	nC
Gate to Drain Charge V_{GS} = 10V, I_D = 8.0A, V_{DS} = 50V	Q_{gd}	-	16.59	nC
SWITCHING CHARACTERISTICS				
Turn-On Delay Time I_D = 8.0A, V_{GS} = +10V. R_G = 7.5Ω, V_{DD} = 30V	$t_{d(on)}$	-	30	ns
Rinse Time I_D = 8.0A, V_{GS} = +10V. R_G = 7.5Ω, V_{DD} = 30V	t_r	-	75	ns
Turn-off Delay Time0 I_D = 8.0A, V_{GS} = +10V. R_G = 7.5Ω, V_{DD} = 30V	$t_{d(off)}$	-	40	ns
Fall Time I_D = 8.0A, V_{GS} = +10V. R_G = 7.5Ω, V_{DD} = 30V	t_f	-	45	ns
Diode Reverse Recovery Time Di/dt ≤ 100A/µs, V_{DD} = ≤ 50V, I_F = 8.0A	t_{rr}	-	300	ns

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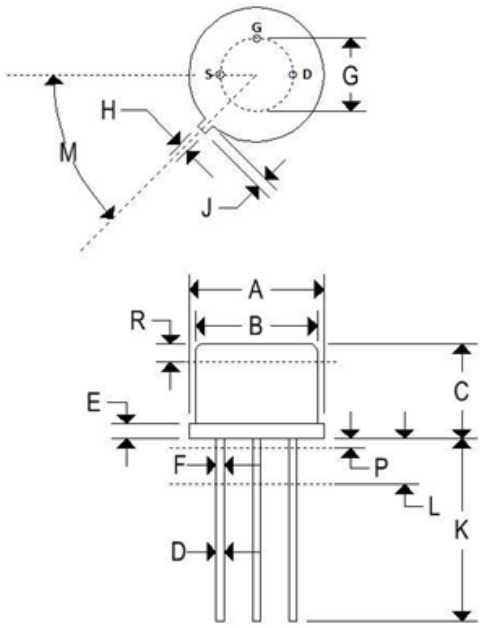
MECHANICAL CHARACTERISTICS

Case:	TO-205 low-profile
Marking:	Alpha-numeric
Pin out:	See below



	TO-205 LOW PROFILE			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.350	0.370	8.890	9.400
B	0.315	0.335	8.000	8.510
C	-	0.180	-	4.57
D	0.016	0.021	0.406	0.533
E	0.009	0.125	0.2269	3.180
F	0.016	0.019	0.406	0.533
G	0.190	0.210	4.830	5.33
H	0.028	0.034	0.711	0.864
J	0.029	0.040	0.737	1.020
K	0.500	-	12.700	-
L	0.250	-	6.350	-
M	45° NOM		45° NOM	
P	-	0.050	-	1.270
Q	90° NOM		90° NOM	
R	0.100	-	2.540	-

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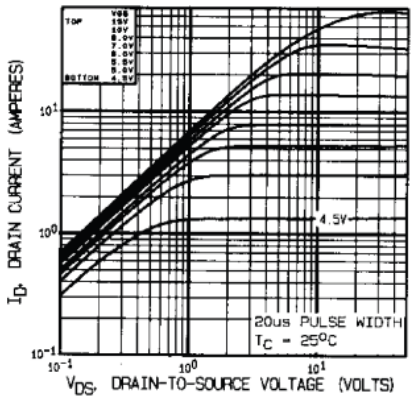

Fig 1. Typical Output Characteristics

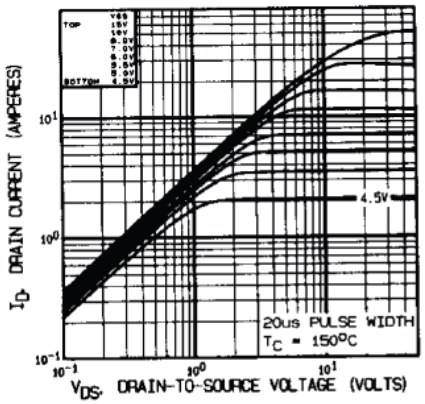

Fig 2. Typical Output Characteristics

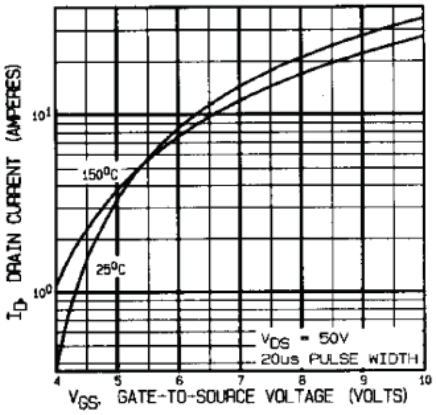

Fig 3. Typical Transfer Characteristics

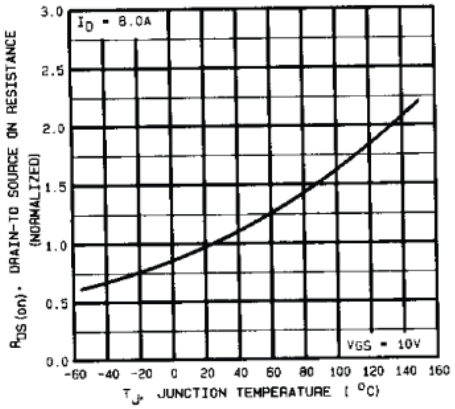

Fig 4. Normalized On-Resistance Vs. Temperature

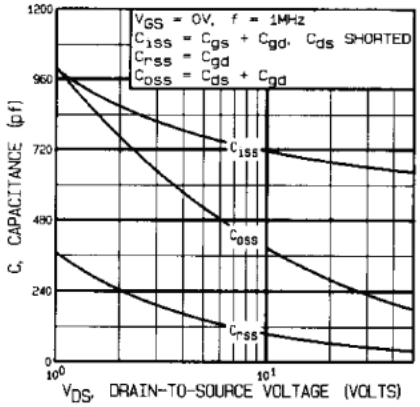

Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

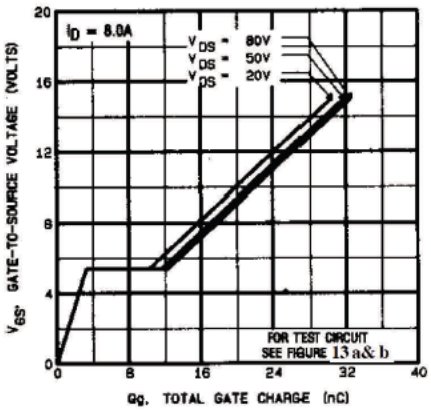

Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

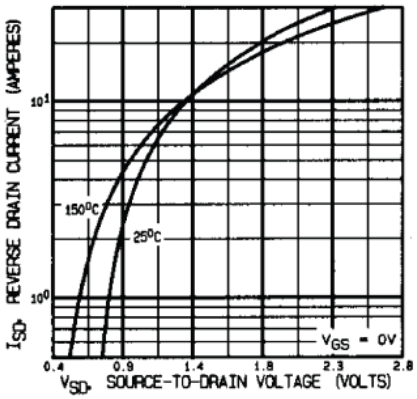

Fig 7. Typical Source-Drain Diode

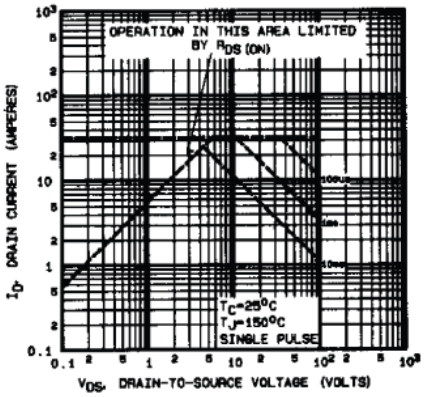

Fig 8. Maximum Safe Operating Area

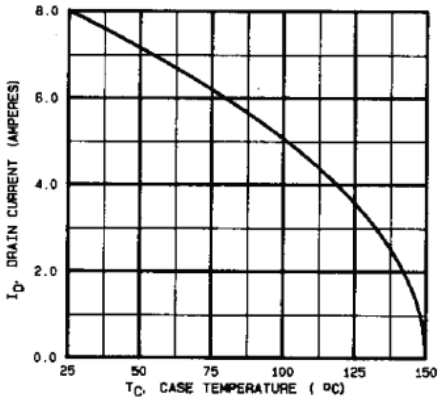

Fig 9. Maximum Drain Current Vs. Case Temperature

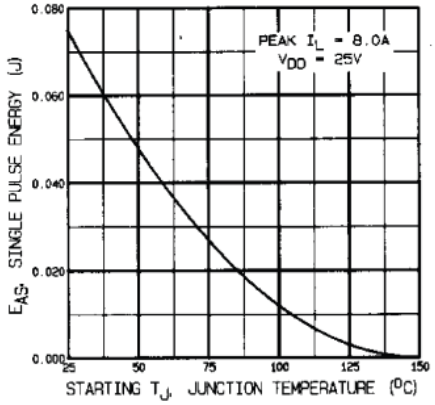

Fig 10. Maximum Avalanche Energy Vs. Drain Current

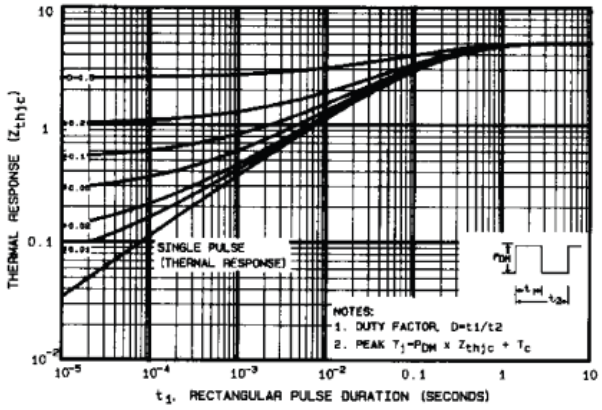

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

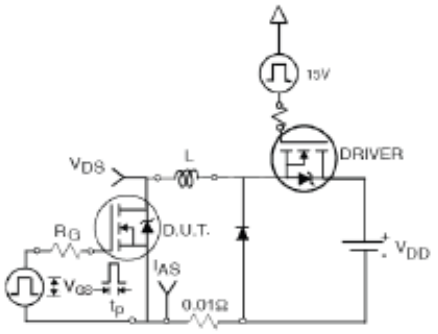

Fig 12a. Unclamped Inductive Test Circuit

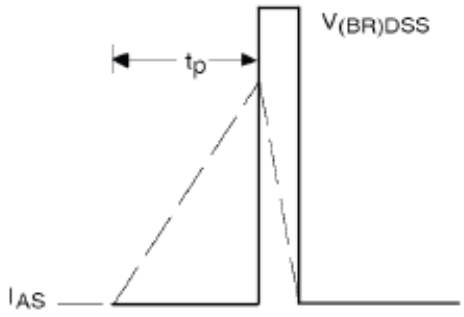

Fig 12b. Unclamped Inductive Waveforms

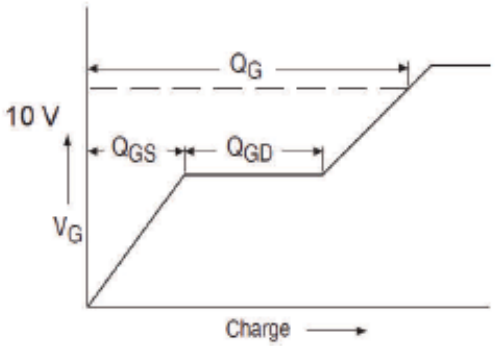

Fig 13a. Gate Charge Waveform

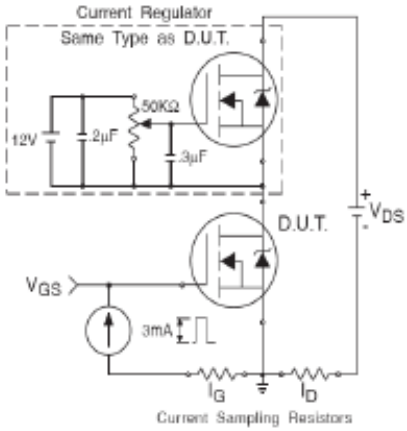

Fig 13b. Gate Charge Test Circuit

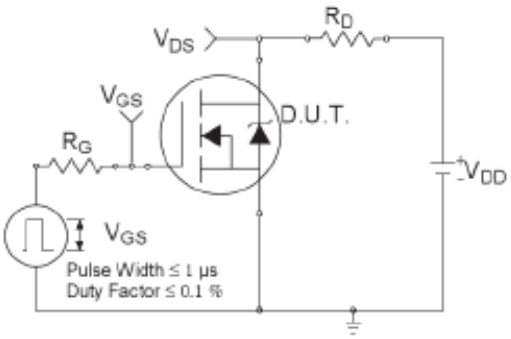

Fig 14a. Switching Time Test Circuit

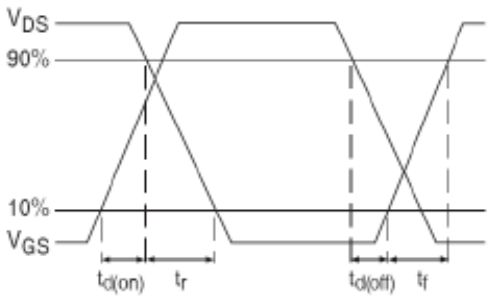

Fig 14b. Switching Time Waveforms