The documentation and process conversion measures necessary to comply with this document shall be completed by 27 November 2013.

INCH-POUND

MIL-PRF-19500/512K
27 August 2013
SUPERSEDING
MIL-PRF-19500/512J
23 April 2010

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, PNP, SILICON, SWITCHING,
TYPES 2N4029, 2N4033, 2N4033UA, 2N4033UB, JAN, JANTX, JANTXV, JANS,
JANSM, JANSD, JANSP, JANSL, JANSR, JANSF, JANSG, JANSH, JANKC2N4033, AND JANHC2N4033

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for PNP silicon transistors designed for use in high speed switching and driver applications. Four levels of product assurance are provided for each encapsulated device type and two levels of product assurance for each unencapsulated specified as in MIL-PRF-19500. Provisions for radiation hardness assurance (RHA) to eight radiation levels is provided for JANS product assurance levels. RHA level designators “M”, “D”, “P“, “L”, “R”, “F’, “G”, and “H” are appended to the device prefix to identify devices, which have passed RHA requirements.

1.2 Physical dimensions. See figure 1 (TO-18), figure 2 (TO-39), figures 3 and 4 (surface mount), and figures 5 and 6 (JANKC and JANHC) herein.

* 1.3 Maximum ratings, unless otherwise specified T_A = +25°C.

V_{CBO}	V_{CEO}	V_{EBO}	I_C	T_J and T_{STG}
V dc	V dc	V dc	A dc	°C
80	80	5.0	1.0	-65 to +200

Types	P_T T_A = +25°C (1) (2)	P_T T_C = +25°C (1) (2)	P_T $T_{SP(IS)}$ = +25°C (1) (2)	$R_{\theta JA}$ (2) (3)	$R_{\theta JC}$ (2) (3)	$R_{\theta JSP(IS)}$ (2) (3)	$R_{\theta JSP(AM)}$ (2) (3)
	W	W	W	°C/W	°C/W	°C/W	°C/W
2N4033	0.800	4	N/A	195	40	N/A	N/A
2N4029	0.500	1	N/A	325	* 150	N/A	N/A
2N4033UA	0.500	N/A	1.5	325	N/A	110	40
2N4033UB	(4) 0.500	N/A	1.5	325	N/A	90	N/A

(1) For derating, see figures 7, 8, 9, 10, and 11.
(2) See 3.3.
(3) For thermal impedance curves, see figures 12, 13, 14, 15, 16, 17, and 18.
* (4) For non-thermal conductive PCB or unknown PCB surface mount conditions in free air, substitute figures 8 and 16 for the UB package and use $R_{\theta JA}$.

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil . Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil .

1.4 Primary electrical characteristics, unless otherwise specified T_A = +25°C.

Limits	h_{FE1} V_{CE} = 5.0 V dc I_C = 100 μA dc	h_{FE2} V_{CE} = 5.0 V dc I_C = 100 mA dc	h_{FE3} V_{CE} = 5.0 V dc I_C = 500 mA dc	h_{FE4} V_{CE} = 5.0 V dc I_C = 1.0 A dc	$\|h_{fe}\|$ f = 100 MHz V_{CE} = 10 V dc I_C = 50 mA dc
Min	50	100	70	25	1.5
Max		300			6.0

Limits	$V_{CE(SAT)2}$ I_C = 500 mA dc I_B = 50 mA dc	C_{obo} V_{CB} = 10 V dc I_E = 0 100 kHz ≤ f ≤ 1 MHz	t_d	t_r	t_s	t_f
	V dc	pF	ns	ns	ns	ns
Min						
Max	0.5	20	15	25	175	35

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS-

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

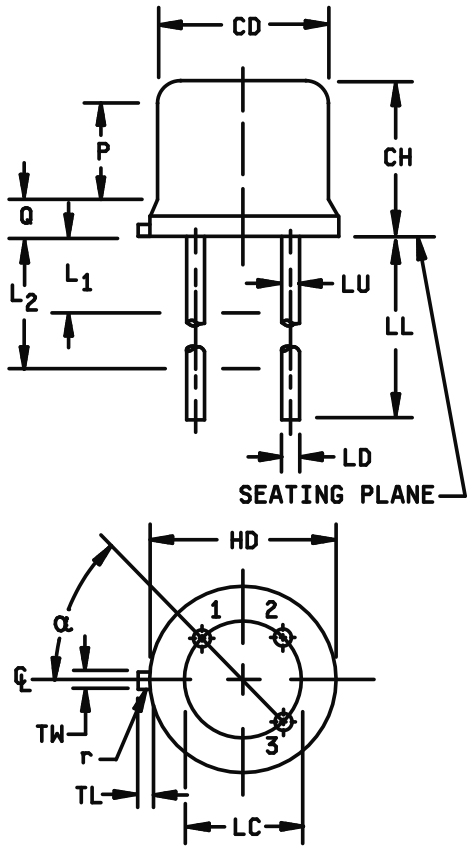
DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://quicksearch.dla.mil or https://assist.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		6
LD	.016	.021	0.41	0.53	7, 8
LL	.500	.750	12.70	19.05	7, 8, 12
LU	.016	.019	0.41	0.48	7, 8
L_1		.050		1.27	7. 8
L_2	.250		6.35		7, 8
Q		.040		1.02	5
TL	.028	.048	0.71	1.22	3, 4
TW	.036	.046	0.91	1.17	3
R		.010		0.25	10
P	.100		2.54		
α	45°TP		45°TP		6

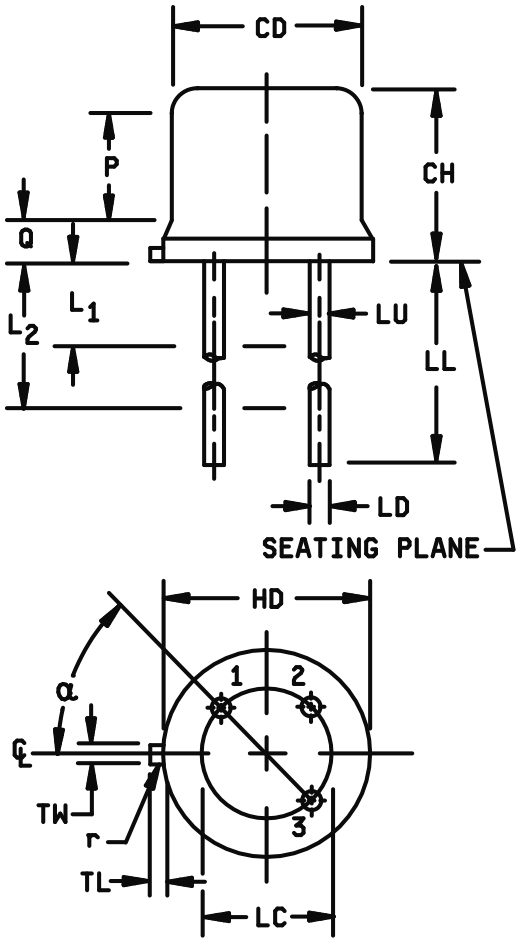


NOTES:

1. Dimensions are in inches.
2. Millimeters equivalents are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of .011 (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 –0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods.
7. Dimension LU applies between L_1 and L_2. Dimension LD applies between L_2 and minimum. Diameter is uncontrolled in L_1 and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to θx symbology.
12. For “L” suffix devices, dimension LL is 1.50 (38.10 mm) minimum, 1.75 (44.45 mm) maximum.

FIGURE 1. Physical dimensions (type 2N4029) (TO-18).

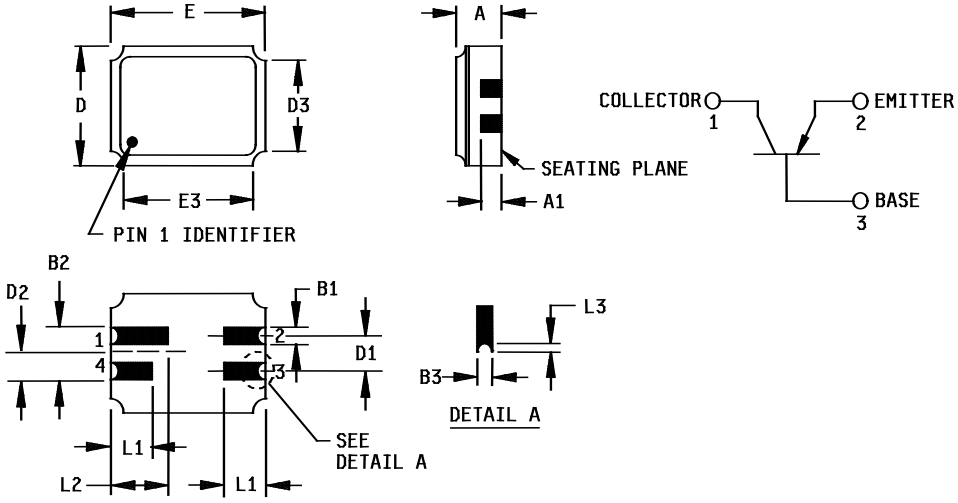
Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		6
LD	.016	.021	0.41	0.53	7, 8
LL	.500	.750	12.70	19.05	7, 8, 12
LU	.016	.019	0.41	0.48	7, 8
L_1		.050		1.27	7, 8
L_2	.250		6.35		7, 8
Q		.050		1.27	5
TL	.029	.045	0.74	1.14	3, 4
TW	.028	.034	0.71	0.86	3
R		.010		0.25	10
P	.100		2.54		
α	45°TP		45°TP		6



NOTES:

1. Dimensions are in inches.
2. Millimeters equivalents are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of .011 (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods.
7. Dimension LU applies between L_1 and L_2. Dimension LD applies between L_2 and minimum. Diameter is uncontrolled in L_1 and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to θx symbology.
12. For “L” suffix devices, dimension LL is 1.50 (38.10 mm) minimum, 1.75 (44.45 mm) maximum.

FIGURE 2. Physical dimensions (type 2N4033) (TO-39).



Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A	.061	.075	1.55	1.91	3
A_1	.029	.041	0.74	1.04	
B_1	.022	.028	0.56	0.71	
B_2	.075 REF		1.91 REF		
B_3	.006	.022	0.15	0.56	5
D	.145	.155	3.68	3.9	
D_1	.045	.055	1.14	1.39	

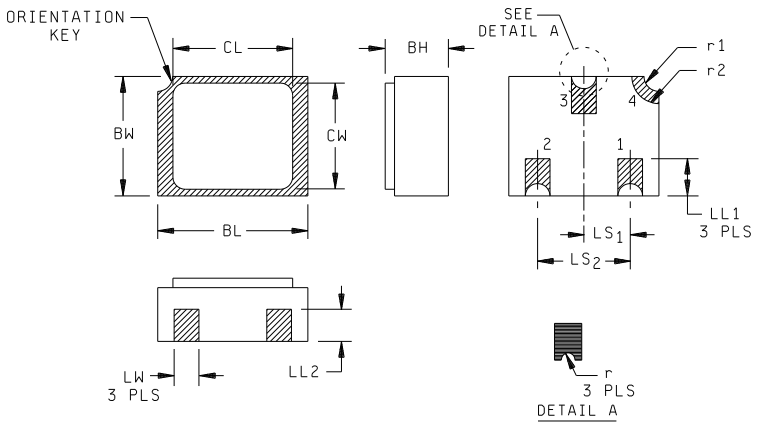
Ltr	Dimensions				Notes
	Inches		Millimeter		
	Min	Max	Min	Max	
D_2	.0375 BSC		0.952 BSC		
D_3		.155		3.94	
E	.215	.225	5.46	5.72	
E_3		.225		5.72	
L_1	.032	.048	0.81	1.22	
L_2	.072	.088	1.83	2.24	
L_3	.003		0.08		5

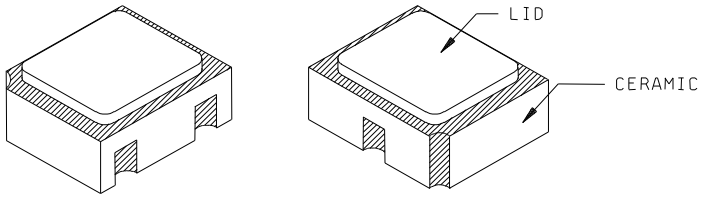
NOTES:

1. Dimensions are in inches.
2. Millimeters equivalents are given for general information only.
3. Dimension “A” controls the overall package thickness. When a window lid is used, dimension “A” must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
4. The corner shape (square, notch, radius, etc.) may vary at the manufacturer’s option, from that shown on the drawing.

* 5. Dimensions “B3” minimum and “L3” minimum and the appropriately castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimension “B3” maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.

* FIGURE 3. Physical dimensions, surface mount (UA version).



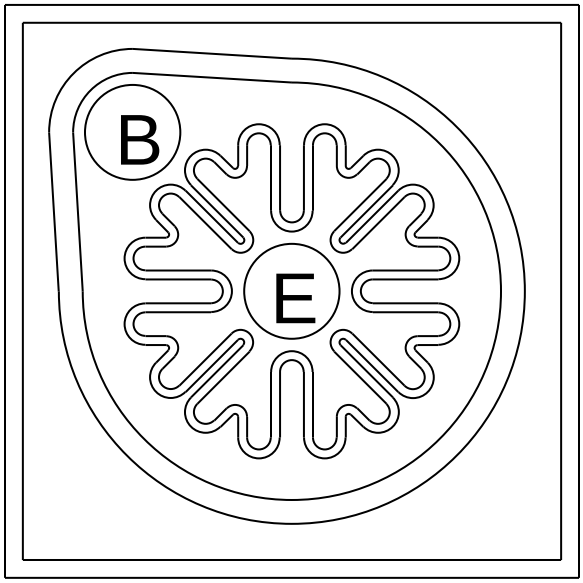


Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BH	.046	.056	1.17	1.42	
BL	.115	.128	2.92	3.25	
BW	.085	.108	2.16	2.74	
CL		.128		3.25	
CW		.108		2.74	
LL1	.022	.038	0.56	0.97	
LL2	.017	.035	0.43	0.89	

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
LS_1	.036	.040	0.91	1.02	
LS_2	.071	.079	1.80	2.01	
LW	.016	.024	0.41	0.61	
r		.008		.203	
r1		.012		.305	
r2		.022		.559	

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas
4. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

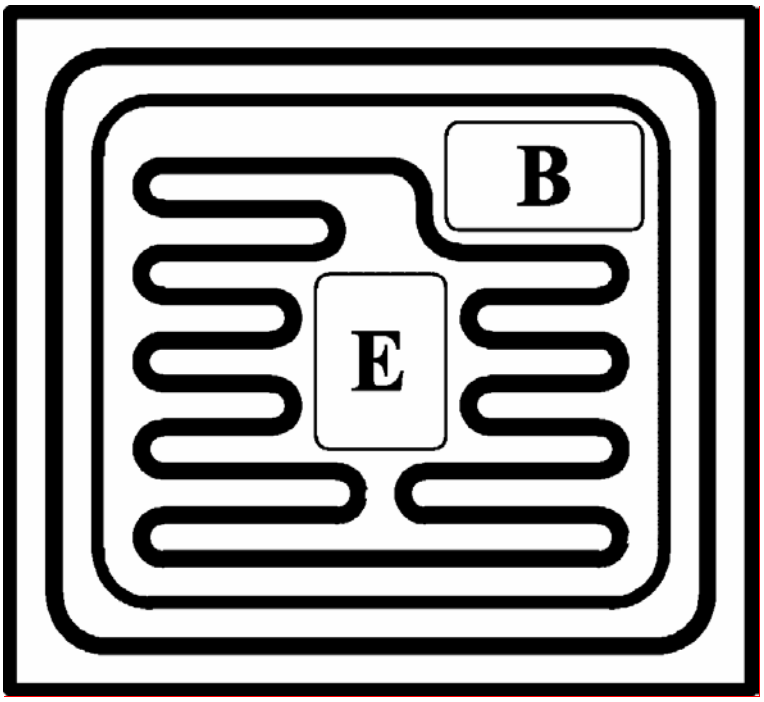
FIGURE 4. Physical dimensions, surface mount UB version.



NOTES:

Die size:	.030 x .030 inch (0.762 x 0.762 mm).
Die thickness:	.008 ±.0016 inch (0.2032 ±0.04064 mm).
Base pad:	.005 inch diameter (0.127 mm).
Emitter pad:	.005 inch diameter (0.127 mm).
Back metal:	Gold, 6,500 ±1,950 Å.
Top metal:	Aluminum, 22,500 ±2,500 Å.
Back side:	Collector.
Glassivation:	SiO_2, 7,500 ±1,500 Å.

FIGURE 5. JANHC and JANKC (A-version) die dimensions.



1. Chip size.....024 x .026 inch ±.002 inch (0.61 x 0.66 millimeters).
2. Chip thickness.....010 ±.0015 inch nominal (0.254 x 0.038 millimeters).
3. Top metal.....Aluminum 15,000 Å minimum, 18,000 Å nominal.
4. Back metal.....Gold 3,500 Å minimum, 5,000 Å nominal.
5. Backside.....Collector.
6. Bonding pad.....B = .004 x .006 inch (0.102 x 0.152 millimeters).
   E = .004 x .0055 inch (0.102 x 0.140 millimeters).

FIGURE 6. JANHC and JANKC (B-version) die dimensions.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

PCB ..... Printed circuit board.
$R_{\theta JA}$ ..... Thermal resistance junction to ambient.
$R_{\theta JC}$ ..... Thermal resistance junction to case.
$R_{\theta JSP(IS)}$..... Thermal resistance junction to solder pads (infinite sink mount to PCB).
$T_{SP(AM)}$ ..... Temperature of solder pads (adhesive mount to PCB).
$T_{SP(IS)}$..... Temperature of solder pads (infinite sink mount to PCB).
UA, UB..... Surface mount case outlines.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figures 1, 2, 3, 4, 5, and 6 herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500. The radiation hardened designator M, D, P, L, R, F, G, or H shall immediately precede (or replace) the device “2N” identifier (depending upon degree of abbreviation required).

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4, table I and table II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (list applicable JAN levels). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
(1) (2) 3c	Thermal impedance method 3131 of MIL-STD-750 (see 4.3.3).	Thermal impedance method 3131 of MIL-STD-750 (see 4.3.3).
9	I_{CBO2} and h_{FE2}	Not applicable
11	I_{CBO2} and h_{FE2} ΔI_{CBO2} = 100 percent or 5 nA, whichever is greater; Δh_{FE2} = ±15 percent change from initial value.	I_{CBO2} and h_{FE2}
12	See 4.3.1	See 4.3.1
13	Subgroups 2 and 3 of table I herein; ΔI_{CBO2} = +100 percent of initial value or 5 nA, whichever is greater. Δh_{FE2} = ±15 percent change from initial value.	Subgroup 2 of table I herein; ΔI_{CBO2} = +100 percent of initial value or 5 nA, whichever is greater. Δh_{FE2} = ±15 percent change from initial value.

* (1) Thermal impedance limits ($Z_{\theta JX}$) shall not exceed figures 12, 13, 14, 15, 16, 17, and 18.
* (2) Shall be performed anytime after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = 10 - 30 V dc. Power shall be applied to achieve T_J = +135°C minimum using a minimum P_D = 75 percent of P_T maximum rated as defined in 1.3. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J, and mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval. Use method 3100 of MIL-STD-750 to measure T_J.

4.3.2 Screening (JANHC and JANKC). Screening of JANHC and JANKC die shall be in accordance with MIL-PRF-19500, "Discrete Semiconductor Die/Chip Lot Acceptance". Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed on each die in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD} (and V_C where appropriate). Measured delay time (t_{MD}) = 70 μs maximum. See table III, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of subgroups 1 and 2 of table I herein, inspection only (table E-VIb, group B, subgroup 1 is not required to be performed since solderability and resistance to solvents testing is performed in table I, subgroup 1 herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-Via (JANS) of MIL-PRF-19500 and 4.4.2.1. Electrical measurements (end-points) requirements shall be in accordance with table I, subgroup 2. Delta requirements shall be in accordance with 4.5.2, delta requirements only apply to subgroups B4 and B5. See 4.4.2.2 for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) for JAN, JANTX, and JANTXV shall be in accordance with group A, subgroup 2. Delta requirements shall be in accordance with 4.5.2 and shall be after each step in 4.4.2.2.

4.4.2.1 Group B inspection (JANS), table E-VIa of MIL-PRF-19500.

Subgroup	Method	Condition
B4	1037	V_{CB} = 10 V dc, 2,000 cycles, adjust device current, or power, to achieve a minimum ΔT_J of +100°C.
B5	1027	V_{CB} = 10 V dc; $P_D \geq$ 100 percent of maximum rated P_T (see 1.3). (NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.) Option 1: 96 hours minimum sample size in accordance with MIL-PRF-19500, table E-VIa, adjust T_A or P_D to achieve T_J = +275°C minimum. Option 2: 216 hours minimum, sample size = 45, c = 0; adjust T_A or P_D to achieve a T_J = +225°C minimum.

4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failures mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

Step	Method	Condition
1	1026	Steady-state life: 1,000 hours minimum, V_{CB} = 10 V dc, power shall be applied to achieve T_J = +150°C minimum using a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
2	1048	Blocking life, T_A = +150°C, V_{CB} = 80 percent of rated voltage, 48 hours minimum. n = 45 devices, c = 0.
3	1032	High-temperature life (non-operating), t = 340 hours, T_A = +200°C. n = 22, c = 0.

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

a. For JAN, JANTX, and JANTXV, samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.

b. Shall be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and in 4.4.3.1 (JANS) and 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) shall be in accordance with table I, group A, subgroup 2 herein. Delta requirements shall be in accordance with 4.5.2; delta requirements only apply to subgroup C6.

4.4.3.1 Group C inspection (JANS), table E-VII of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E; (not applicable for UA and UB devices).
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3) and in accordance with thermal impedance curves. See 4.3.3.
C6	1026	1,000 hours at V_{CB} = 10 V dc; power shall be applied to achieve T_J = +150°C minimum and a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3 n = 45, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.

4.4.3.2 Group C inspection (JAN, JANTX, and JANTXV), table E-VII of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E; not applicable for UA and UB devices.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3 and 4.3.3) and in accordance with thermal impedance curves.
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests herein for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

* 4.4.4 Group D inspection. Conformance inspection for hardness assured JANS and JANTXV types shall include the group D tests specified in table II herein. These tests shall be performed as required in accordance with MIL-PRF-19500 and method 1019 of MIL-STD-750, for total ionizing dose or method 1017 of MIL-STD-750 for neutron fluence as applicable (see 6.2.e herein), except group D, subgroup 2 may be performed separate from other subgroups. Alternate package options may also be substituted for the testing provided there is no adverse effect to the fluence profile.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein; delta measurements shall be in accordance with the applicable steps of 4.5.2.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Delta requirements. Delta requirements shall be as follows:

Step	Inspection	MIL-STD-750		Symbol	Limit	Unit
		Method	Conditions			
1.	Collector-base cutoff current	3036	Bias condition D, V_{CB} = 60 V dc	ΔI_{CB02}	100 percent of initial value or 5 nA dc, whichever is greater.	
2.	Forward current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 100 mA dc; pulsed see 4.5.1	Δh_{FE2}	±25 percent change from initial reading.	

4.5.3 Collector-base time constant. This parameter may be determined by applying an rf signal voltage of 1.0 volt (rms) across the collector-base terminals and measuring the ac voltage drop (V_{eb}) with a high-impedance rf voltmeter across the emitter-base terminals. With f = 79.8 MHz used for the 1.0 volt signal, the following computation applies:

$$r'_b , C_{c(ps)} = 2 \times V_{eb} \text{ (millivolts)}$$

* TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1 2/						
Visual and mechanical examination 3/	2071					
Solderability 3/ 4/	2026	n = 15 leads, c = 0				
Resistance to solvents 3/ 4/ 5/	1022	n = 15 devices, c = 0				
Temp cycling 3/ 4/	1051	Test condition C, 25 cycles, n = 22 devices, c = 0				
Hermetic seal 4/ 6/ Fine leak Gross leak	1071	n = 22 devices, c = 0				
Electrical measurements 4/		Table I, subgroup 2				
Bond strength 3/ 4/	2037	Precondition T_A = +250°C at t = 24 hours or T_A = +300°C at t = 2 hours; n = 11 wires, c = 0				
Decap internal visual (design verification) 4/	2075	n = 4 devices, c = 0				
Subgroup 2						
Thermal impedance	3131	See 4.3.3	$Z_{\theta JX}$			°C/W
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 80 V dc; pulsed (see 4.5.1)	I_{CBO1}		10	µA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 5 V dc	I_{EBO1}		10	µA dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 60 V dc	I_{CBO2}		10	nA dc
Collector to emitter cutoff current	3041	Bias condition A; V_{BE} = 2.0 V dc; V_{CE} = 60 V dc	I_{CEX1}		25	nA dc
Base emitter cutoff current	3061	Bias condition D; V_{BE} = 3.0 V dc	I_{EBO2}		25	nA dc
Forward-current transfer ratio	3076	V_{CE} = 5.0 V dc; I_C = 100 µA dc	h_{FE1}	50		
* Forward-current transfer ratio	3076	V_{CE} = 5.0 V dc; I_C = 100 mA dc pulsed (see 4.5.1)	h_{FE2}	100	300	
Forward-current transfer ratio	3076	V_{CE} = 5.0 V dc; I_C = 500 mA dc; pulsed (see 4.5.1)	h_{FE3}	70		
Forward-current transfer ratio	3076	V_{CE} = 5.0 V dc; I_C = 1.0 A dc; pulsed (see 4.5.1)	h_{FE4}	25		

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 2 – Continued						
Collector - emitter saturated voltage	3071	I_C = 150 mA dc; I_B = 15 mA dc; pulsed (see 4.5.1)	$V_{CE(SAT)1}$		0.15	V dc
Collector - emitter saturated voltage	3071	I_C = 500 mA dc; I_B = 50 mA dc; pulsed (see 4.5.1)	$V_{CE(SAT)2}$		0.50	V dc
Collector - emitter saturated voltage	3071	I_C = 1.0 A dc; I_B = 100 mA dc; pulsed (see 4.5.1)	$V_{CE(SAT)3}$		1.0	V dc
Base – emitter saturated voltage	3066	Test condition A; I_C = 150 mA dc; I_B = 15 mA dc pulsed (see 4.5.1)	$V_{BE(SAT)1}$		0.9	V dc
Base - emitter saturated voltage	3066	Test condition A; I_C = 500 mA dc; I_B = 50 mA dc; pulsed (see 4.5.1)	$V_{BE(SAT)2}$		1.2	V dc
Subgroup 3						
High-temperature operation:		T_A = +150°C				
Collector -base cutoff current	3036	Bias condition D; V_{CB} = 60 V dc	I_{CBO3}		25	µA dc
Low-temperature operation:		T_A = -55°C				
Forward-current transfer ratio	3076	V_{CE} = 5.0 V dc; I_C = 500 mA dc; pulsed (see 4.5.1)	h_{FE5}	30		
Subgroup 4						
Magnitude of common emitter small-signal short-circuit forward-current transfer ratio	3306	V_{CE} = 10 V dc; I_C = 50 mA dc; f = 100 MHz	$\lvert h_{fe} \rvert$	1.5	6.0	
Open circuit output capacitance	3236	V_{CB} = 10 V dc; I_E = 0; 100 kHz ≤ f ≤ 1 MHz	C_{obo}		20	pF
Input capacitance (output open-circuited)	3240	V_{EB} = 0.5 V dc; I_C = 0; 100 kHz ≤ f ≤ 1 MHz	C_{ibo}		80	pF

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 4 – Continued						
Pulse response						
On-time	3251	Test condition A; I_C = 500 mA dc; I_{B1} = 50 mA dc; (see figure 19)	t_d		15	ns
Rise time	3251	Test condition A; I_C = 500 mA dc; I_{B1} = 50 mA dc; (see figure 19)	t_r		25	ns
Storage time	3251	Test condition A; I_C = 500 mA dc; I_{B1} = 50 mA dc; (see figure 20)	t_s		175	ns
Fall time	3251	Test condition A; I_C = 500 mA dc; I_{B1} = 50 mA dc; (see figure 20)	t_f		35	ns
Subgroups 5, 6, and 7						
Not applicable						

1/ For sampling plan see MIL-PRF-19500.
2/ For resubmission of failed test in subgroup 1 of table I, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.
3/ Separate samples may be used.
4/ Not required for JANS devices.
5/ Not required for laser marked devices.
6/ This hermetic seal test is an end-point to temp-cycling in addition to electrical measurements.

TABLE II. Group D inspection.

Inspection 1/ 2/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1 3/						
Neutron irradiation	1017	Neutron exposure V_{CES} = 0 V				
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 80 V dc; pulsed (see 4.5.1)	I_{CBO1}		20	µA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 5 V dc	I_{EBO1}		20	µA dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 60 V dc	I_{CBO2}		20	nA dc
Collector to emitter cutoff current	3041	Bias condition A; V_{BE} = 2.0 V dc; V_{CE} = 60 V	I_{CEX1}		50	nA dc
Base emitter cutoff current	3061	Bias condition D; V_{EB} = 3 V dc	I_{EBO2}		50	nA dc
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 100 µA dc	[h_{FE1}] 4/	[25]		
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 100 mA dc	[h_{FE2}] 4/	[50]	300	
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 500 mA dc; pulsed (see 4.5.1)	[h_{FE3}] 4/	[35]		
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 1 A dc; pulsed (see 4.5.1)	[h_{FE4}] 4/	[12]		
Collector-emitter saturation voltage	3071	I_C = 150 mA dc; I_B = 15 mA dc; pulsed (see 4.5.1)	$V_{CE(sat)1}$		.18	V dc
Collector-emitter saturation voltage	3071	I_C = 500 mA dc; I_B = 50 mA dc; pulsed (see 4.5.1)	$V_{CE(sat)2}$		.58	V dc
Collector-emitter saturation voltage	3071	Ic = 1 A dc; I_B = 100 mA dc; pulsed (see 4.5.1)	$V_{CE(sat)3}$		1.15	V dc
Base-emitter saturation voltage	3066	Test condition A; I_C = 150 mA dc; I_B = 15 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)1}$		1.1	V dc
Base-emitter saturation voltage	3066	Test condition A; I_C = 500 mA dc; I_B = 50 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)2}$		1.5	V dc

See footnotes at end of table.

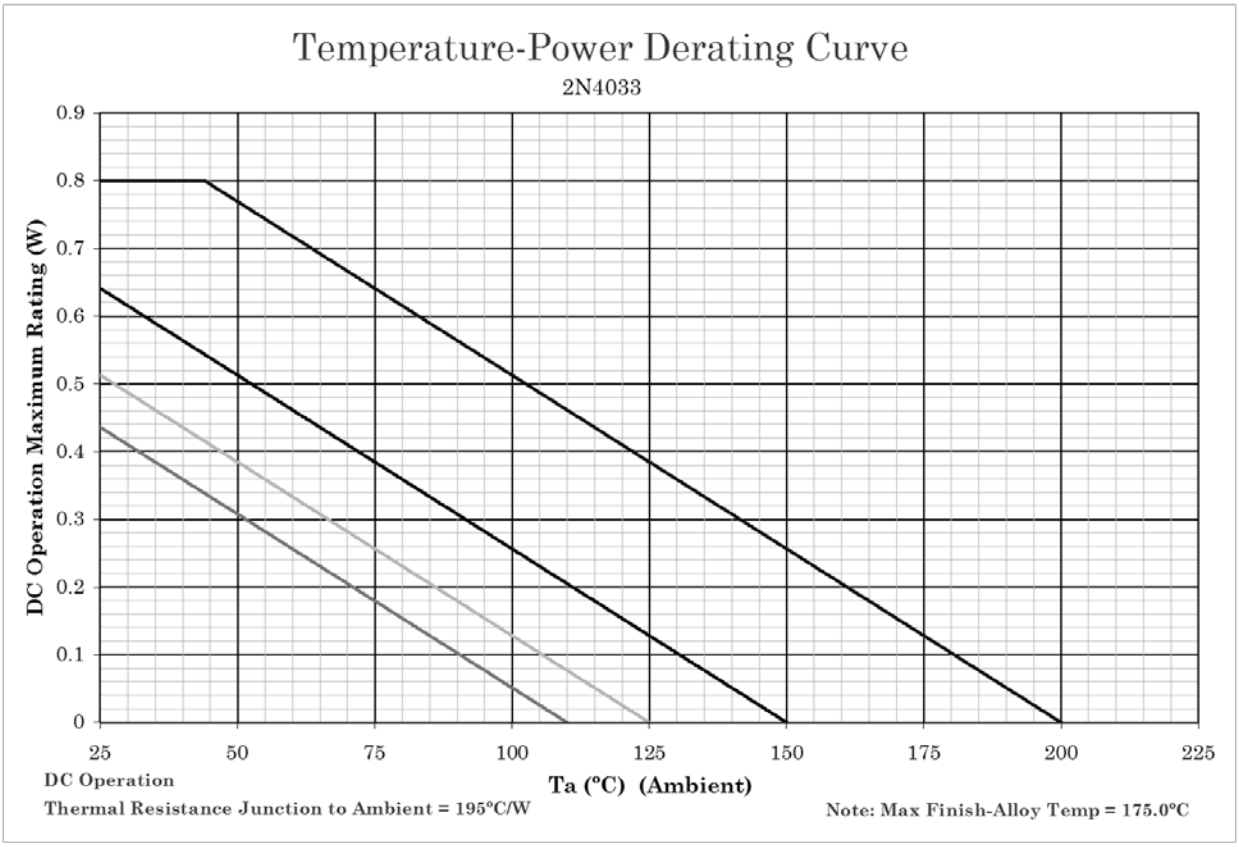
TABLE II. Group D inspection - Continued.

Inspection 1/ 2/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2						
Total dose irradiation	1019	Gamma exposure V_{CES} = 64 V Condition A				
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 80 V dc; pulsed (see 4.5.1)	I_{CBO1}		20	µA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 5 V dc	I_{EBO1}		20	µA dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 60 V dc	I_{CBO2}		20	nA dc
Collector to emitter cutoff current	3041	Bias condition A; V_{BE} = 2.0 V dc; V_{CE} = 60 V	I_{CEX1}		50	nA dc
Base emitter cutoff current	3061	Bias condition D; V_{EB} = 3 V dc	I_{EBO2}		50	nA dc
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 100 µA dc	$[h_{FE1}]$ 4/	[25]		
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 100 mA dc	$[h_{FE2}]$ 4/	[50]	300	
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 500 mA dc; pulsed (see 4.5.1)	$[h_{FE3}]$ 4/	[35]		
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 1 A dc; pulsed (see 4.5.1)	$[h_{FE4}]$ 4/	[12]		
Collector-emitter saturation voltage	3071	I_C = 150 mA dc; I_B = 15 mA dc; pulsed (see 4.5.1)	$V_{CE(sat)1}$		.18	V dc
Collector-emitter saturation voltage	3071	I_C = 500 mA dc; I_B = 50 mA dc; pulsed (see 4.5.1)	$V_{CE(sat)2}$		.58	V dc
Collector-emitter saturation voltage	3071	Ic = 1 A dc; I_B = 100 mA dc; pulsed (see 4.5.1)	$V_{CE(sat)3}$		1.15	V dc
Base-emitter saturation voltage	3066	Test condition A; I_C = 150 mA dc; I_B = 15 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)1}$		1.1	V dc
Base-emitter saturation voltage	3066	Test condition A; I_C = 500 mA dc; I_B = 50 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)2}$		1.5	V dc

1/ Tests to be performed on all devices receiving radiation exposure.
2/ For sampling plan, see MIL-PRF-19500.
3/ See 6.2.e herein.
4/ See method 1019 of MIL-STD-750 for how to determine $[h_{FE}]$ by first calculating the delta $(1/h_{FE})$ from the pre- and post-radiation h_{FE}. Notice the $[h_{FE}]$ is not the same as h_{FE} and cannot be measured directly. The $[h_{FE}]$ value can never exceed the pre-radiation minimum h_{FE} that it is based upon.

* TABLE III. Group E inspection (all quality levels) - for qualification or re-qualification only.

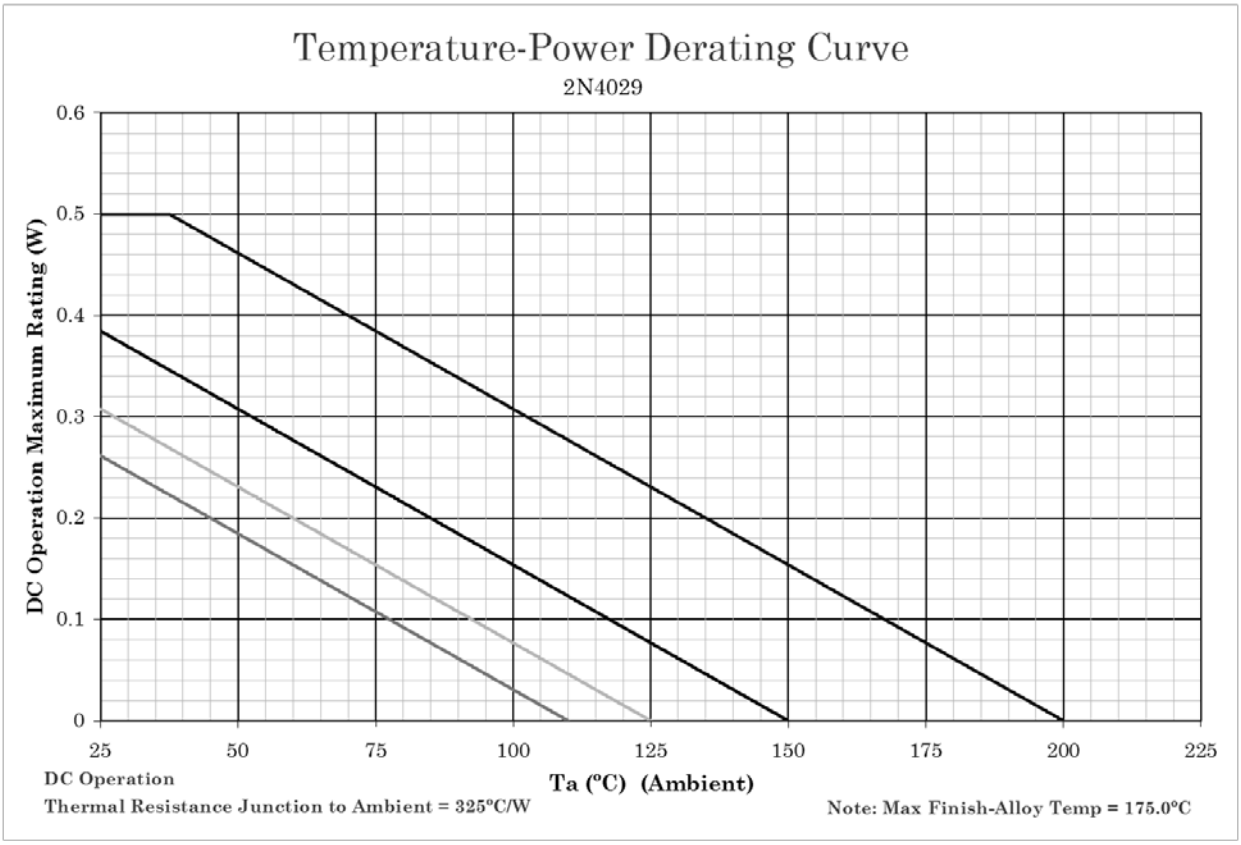
Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles.	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2 and 4.5.2 herein.	
Subgroup 2			45 devices c = 0
Intermittent life	1037	Intermittent operation life: V_{CB} = 10 V dc, 6,000 cycles. Adjust device current, or power, to achieve a minimum ΔT_J of +100°C.	
Electrical measurements		See table I, subgroup 2 and 4.5.2 herein.	
Subgroup 4			
Thermal resistance	3131	$R_{\theta JSP(IS)}$ can be calculated but shall be measured once in the same package with a similar die size to confirm calculations (may apply to multiple specification sheets). $R_{\theta JSP(AM)}$ need be calculated only.	15 devices, c = 0
Thermal impedance curves		See MIL-PRF-19500, table E-IX, group E, subgroup 4.	
Subgroup 5			
Not applicable			
Subgroup 6			11 devices
ESD	1020		
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition B.	



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq$, 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

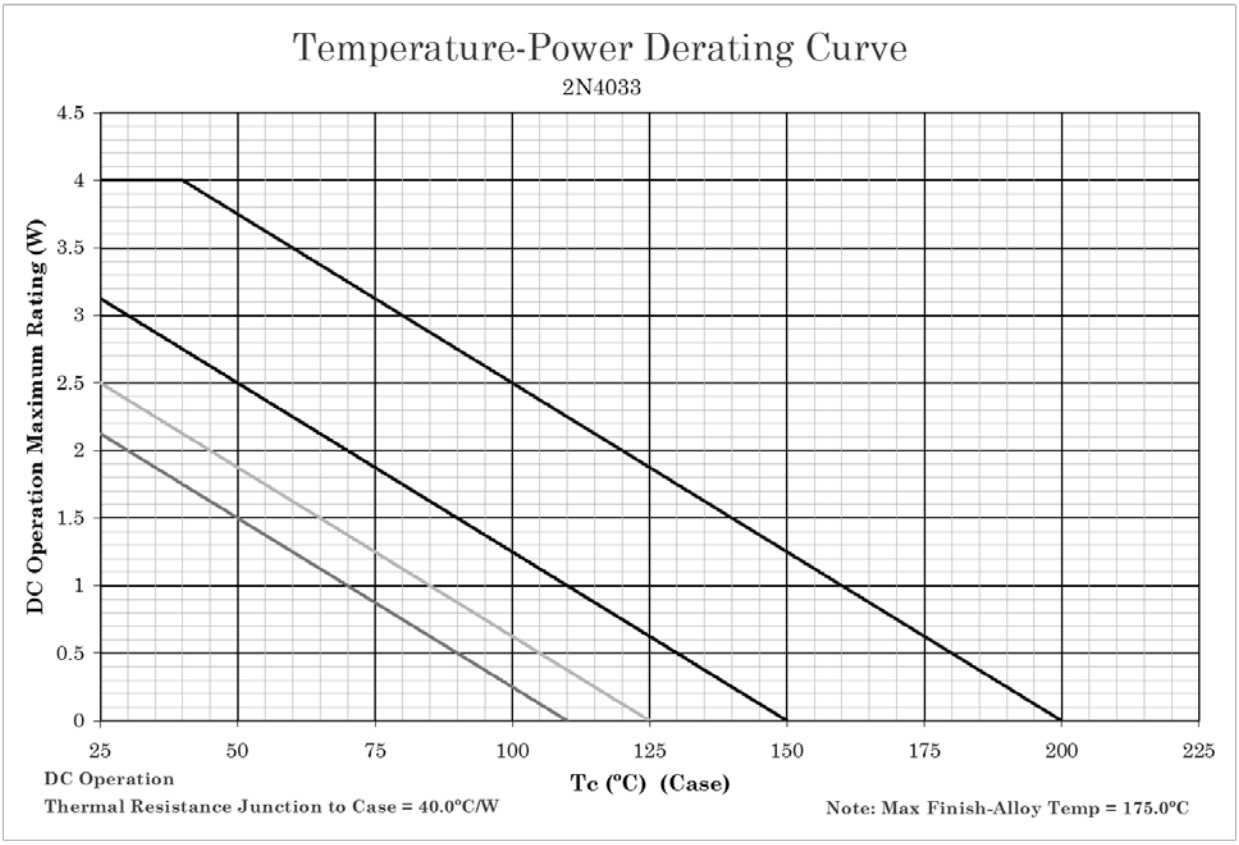
FIGURE 7. Derating for 2N4033 ($R_{\theta JA}$) (TO-39).



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq$, 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

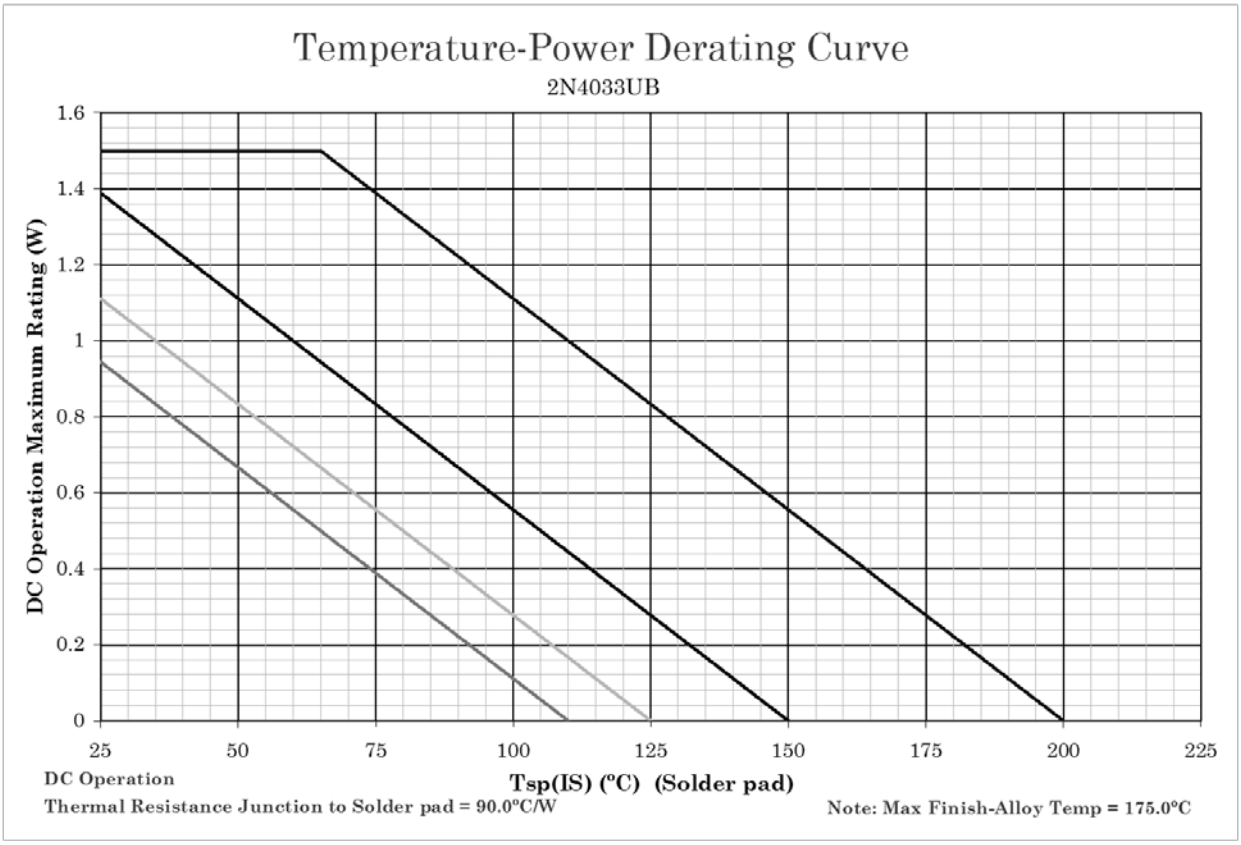
FIGURE 8. Derating for 2N4029 ($R_{\theta JA}$) (TO-18), leads .125 inch (3.17 mm).



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

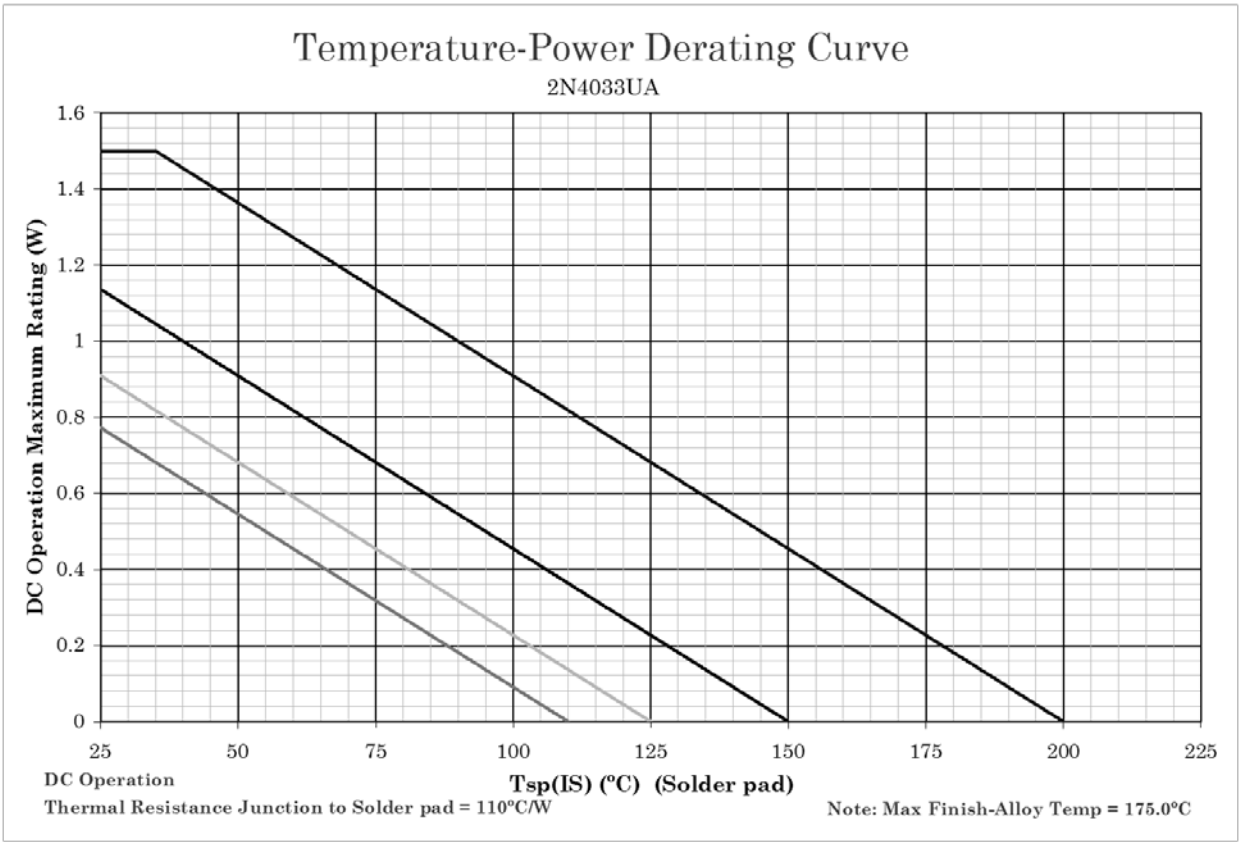
FIGURE 9. Derating for 2N4033 ($R_{\theta JC}$) (TO-39).



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 10. Derating for 2N4033UB ($R_{\theta JSP(IS)}$), infinite sink 3-points.



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 11. Derating for 2N4033UA ($R_{\theta JSP(IS)}$).

Maximum Thermal Impedance

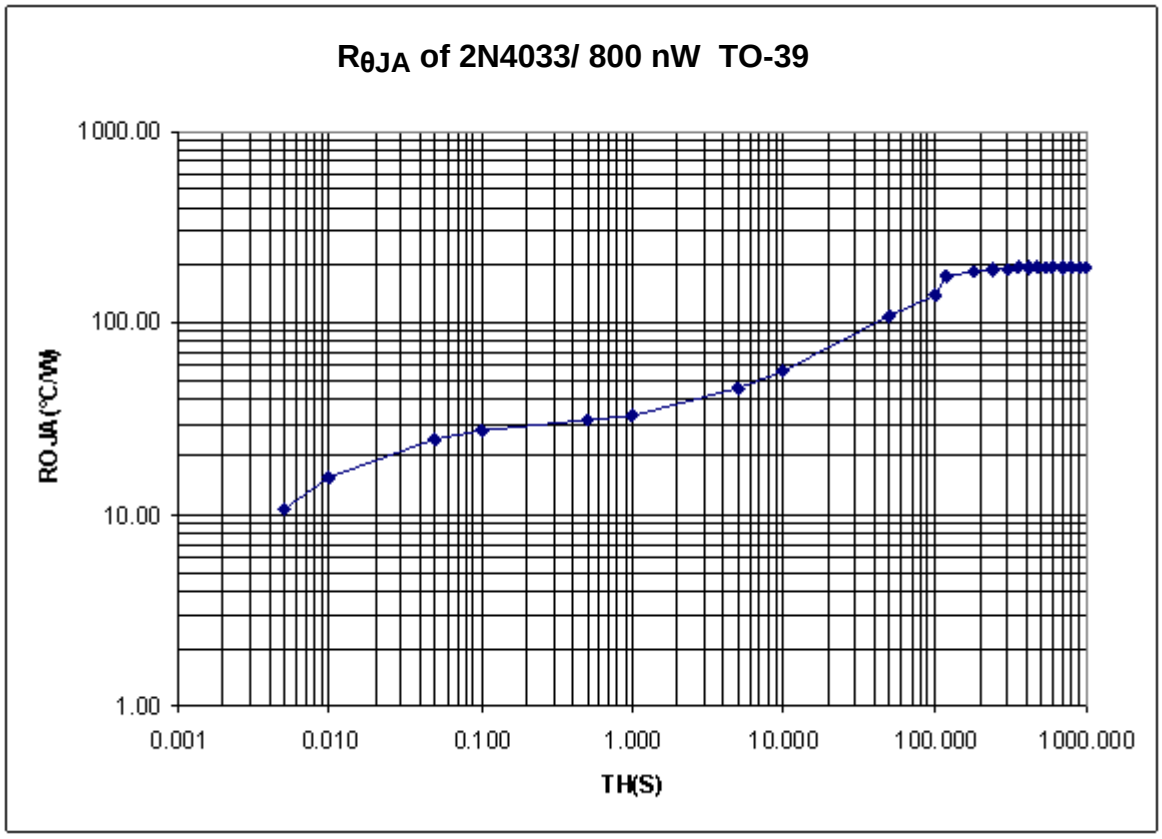


FIGURE 12. Thermal impedance graph ($R_{\theta JA}$) for 2N4033 (TO-39).

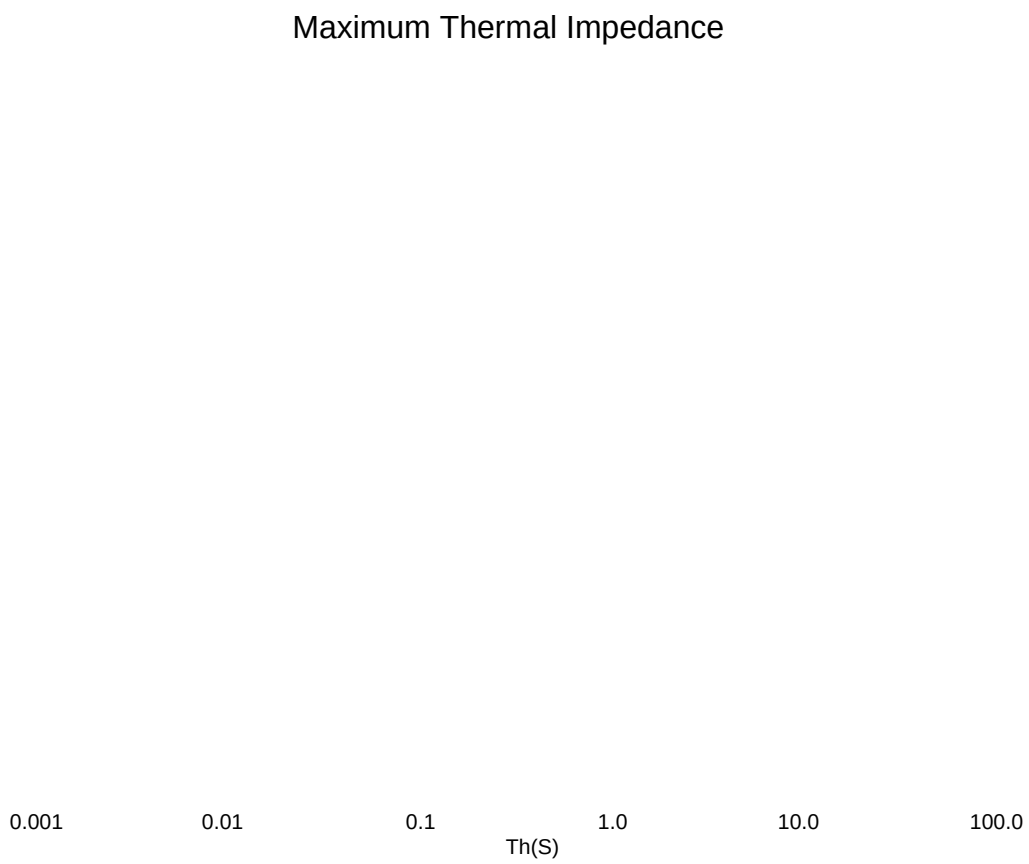


FIGURE 13. Thermal impedance graph ($R_{\theta JC}$) for 2N4033 (TO-39).

Maximum Thermal Impedance

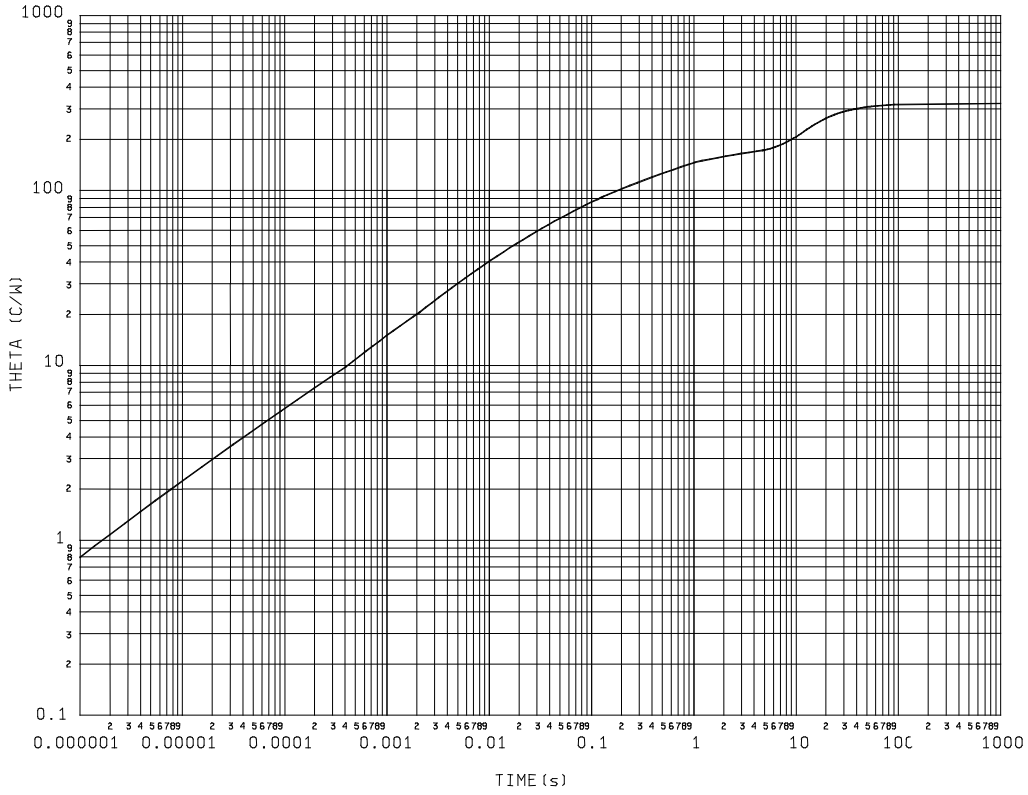
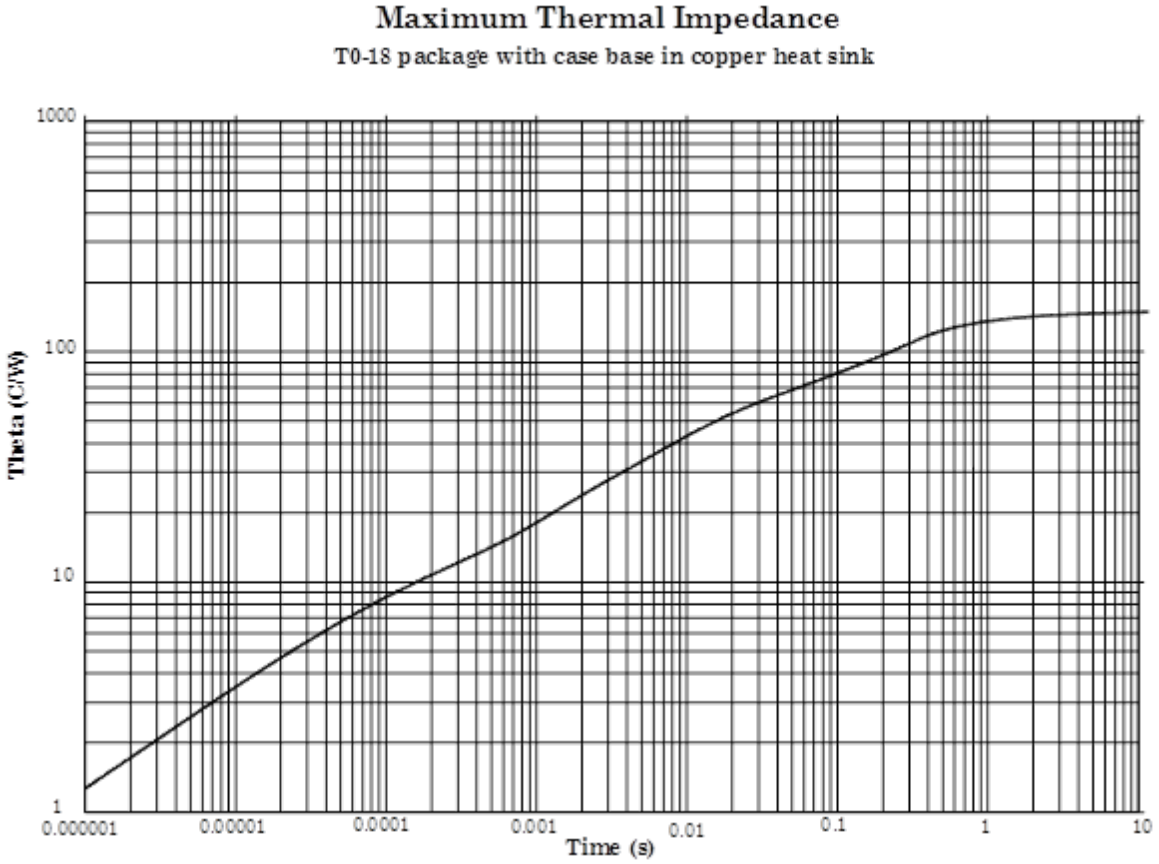


FIGURE 14. Thermal impedance graph ($R_{\theta JA}$) for 2N4029 (TO-18).



$R_{\theta JC}$ = 150°C/W

* FIGURE 15. Thermal impedance graph ($R_{\theta JC}$) for 2N4029 (TO-18).

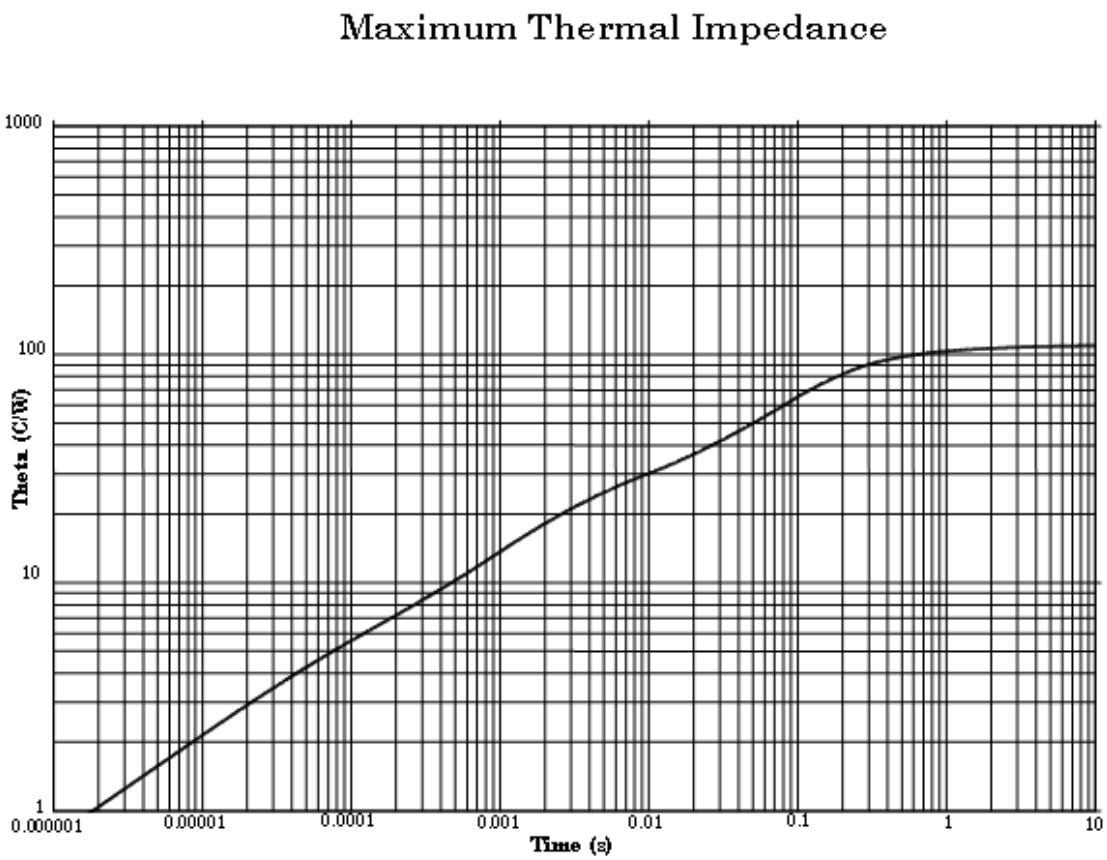
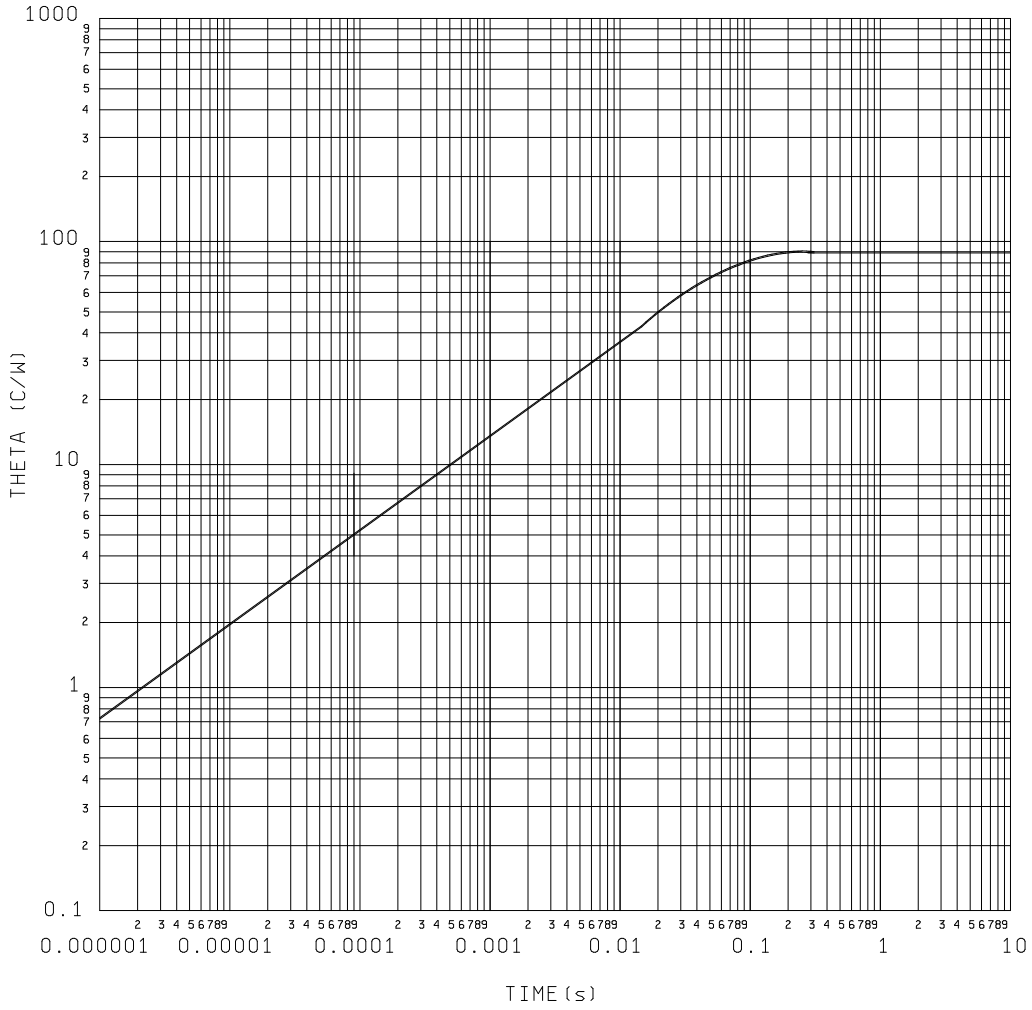


FIGURE 16. Thermal impedance graph ($R_{\theta JSP(IS)}$) for 2N4033 (UA).

Maximum Thermal Impedance

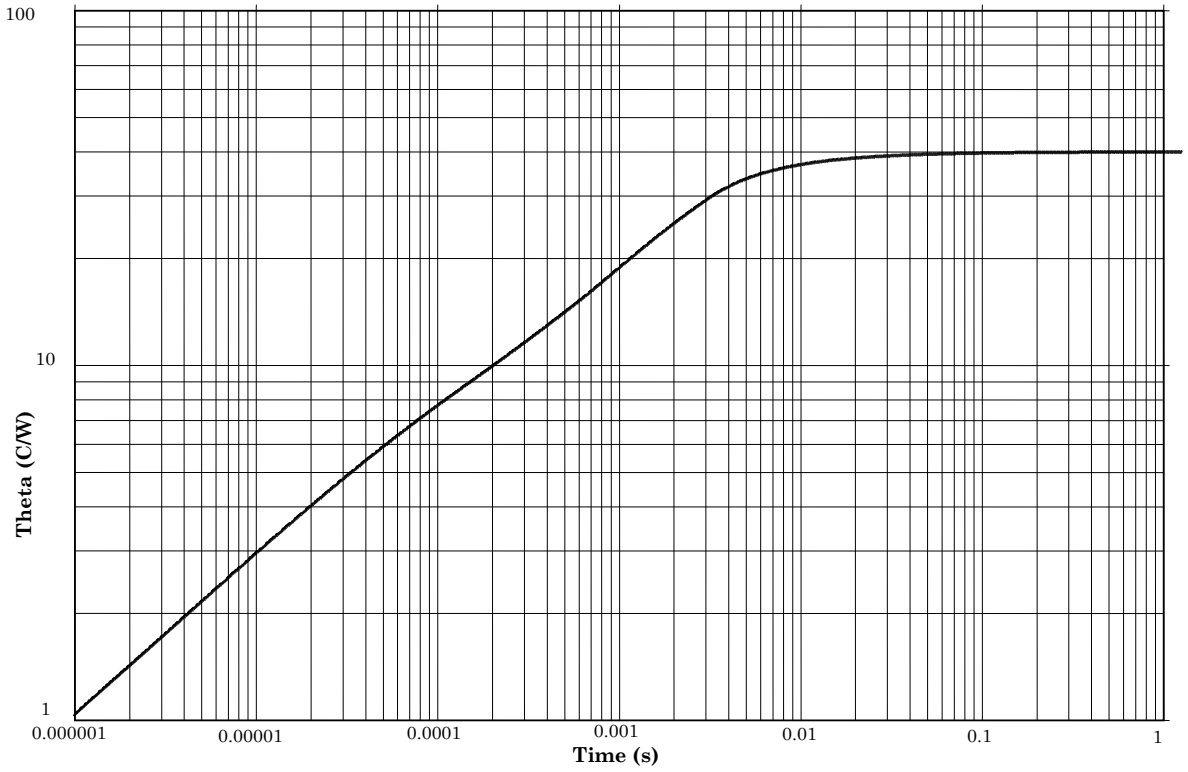


Ceramic UB package soldered to PCB 3 points solder pad (infinite sink to PCB).

$R_{\theta JSP(IS)}$ = 90°C/W

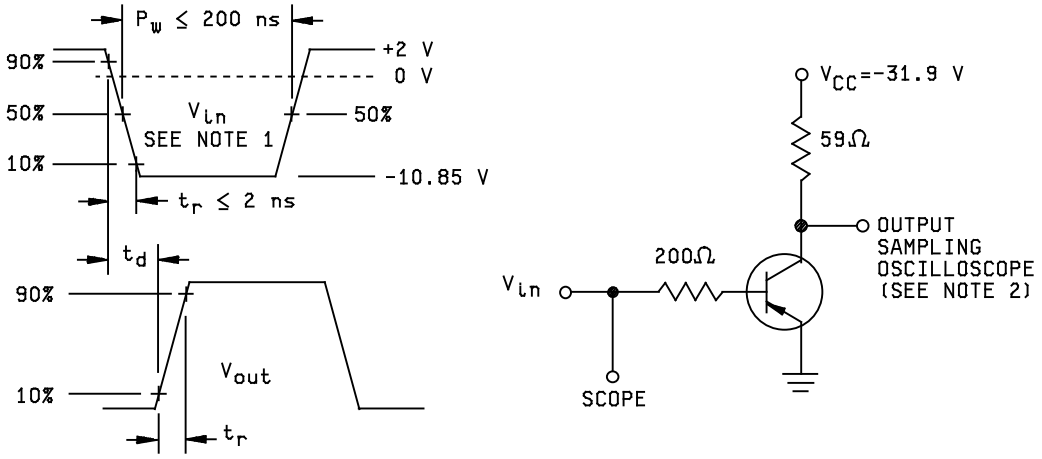
FIGURE 17. Thermal impedance graph ($R_{\theta JSP(IS)}$) for 2N4029 (UB).

Maximum Thermal Impedance



2N4033UA 4 point solder pad (adhesive mount to PCB), $R_{\theta JSP(AM)}$ = 40°C/W

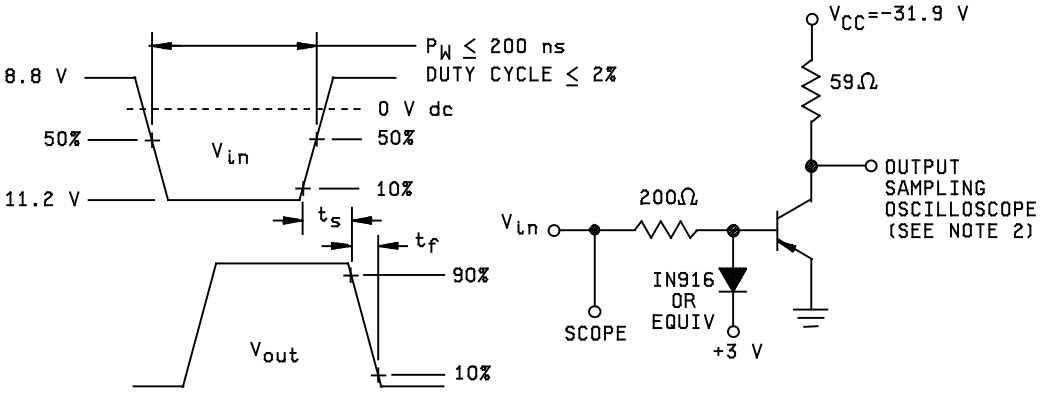
FIGURE 18. Thermal impedance graph $R_{\theta JSP(AM)}$ for 2N4033UA.



NOTES:

1. The rise time (t_r) of the applied pulse shall be ≤ 2.0 ns, duty cycle ≤ 2 percent, and the generator source Z shall be 50 Ω.
2. Sampling oscilloscope: Z_{IN} ≥ 100 kΩ; C_{in} ≤ 12 pF, rise time(t_r) ≤ 5 ns.

FIGURE 19. Delay and rise time, test circuit.



NOTES:

1. The rise time (t_r) of the applied pulse shall be ≤ 20 ns, duty cycle ≤ 2 percent, and the generator source impedance shall be 50Ω.
2. Sampling oscilloscope: Z_{IN} ≥ 100 kΩ; C_{in} ≤ 12 pF, rise time (t_r) ≤ 5 ns.

FIGURE 20. Storage and fall time, test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. Product assurance level and type designator.

e. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it must be specified in the contract.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: /VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil . An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

6.4. Suppliers of JANHC and JANKC die. The qualified JANHC and JANKC suppliers with the applicable letter version (example JANHCA2N4033) will be identified on the QML.

Die ordering information		
PIN	Manufacturer	
	34156	43611
2N4033	JANHCA2N4033 JANKCA2N4033	JANHCB2N4033 JANKCB2N4033

6.5 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
DLA - CC

Review activities:
Army - AV, MI
Air Force - 19, 71, 99

Preparing activity:
DLA - CC

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* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil .