

Crystal to LVPECL Clock Generator

Features

- One LVPECL output pair
- Selectable frequency multiplication: x 2.5 or x 5
- External crystal frequency: 25.0 MHz
- Output frequency: 62.5 MHz or 125 MHz
- Low RMS phase jitter at 125 MHz, using 25 MHz crystal (1.875 MHz to 20 MHz): 0.4 ps (typical)
- Phase noise at 125 MHz (typical):

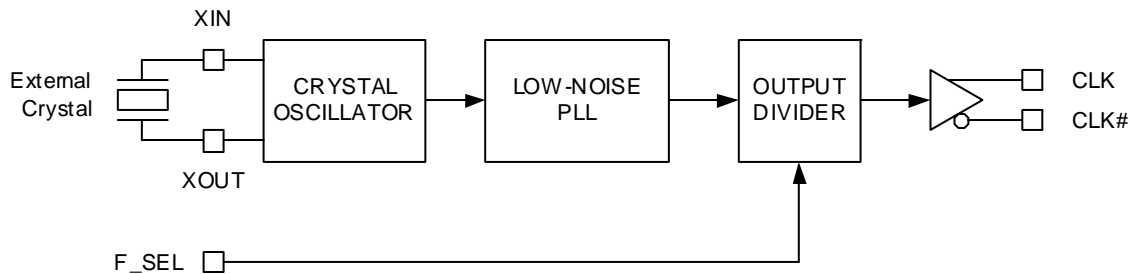
Offset	Noise Power
1 kHz	-117 dBc/Hz
10 kHz	-126 dBc/Hz
100 kHz	-131 dBc/Hz
1 MHz	-131 dBc/Hz

- Pb-free 8-pin TSSOP package
- Supply voltage: 3.3 V or 2.5 V
- Commercial and Industrial temperature range

Functional Description

The CY2XP22 is a PLL (Phase Locked Loop) based high performance clock generator that uses an external reference crystal. It is specifically targeted at FibreChannel and Gigabit Ethernet applications. It produces a selectable output frequency that is 2.5 or 5 times the crystal frequency. With a 25 MHz crystal, the user can select either a 62.5 MHz or 125 MHz output. It uses Cypress's low noise VCO technology to achieve less than 1 ps typical RMS phase jitter. The CY2XP22 has a crystal oscillator interface input and one LVPECL output pair.

Logic Block Diagram



Contents

Pinouts	3	Ordering Information	10
Pin Definitions	3	Ordering Code Definitions	10
Frequency Table	3	Package Drawing and Dimensions	11
Absolute Maximum Conditions	4	Acronyms	12
Operating Conditions	4	Document Conventions	12
DC Electrical Characteristics	5	Units of Measure	12
AC Electrical Characteristics	6	Document History Page	13
Recommended Crystal Specifications	6	Sales, Solutions, and Legal Information	14
Parameter Measurements	7	Worldwide Sales and Design Support	14
Application Information	9	Products	14
Power Supply Filtering Techniques	9	PSoC® Solutions	14
Termination for LVPECL Output	9	Cypress Developer Community	14
Crystal Interface	9	Technical Support	14

Pinouts

Figure 1. 8-pin TSSOP pinout



Pin Definitions

8-pin TSSOP

Pin Number	Pin Name	I/O Type	Description
1, 8	VDD	Power	3.3 V or 2.5 V power supply
2	VSS	Power	Ground
3, 4	XOUT, XIN	XTAL output and input	Parallel resonant crystal interface
5	F_SEL	CMOS input	Frequency Select: see Frequency Table
6,7	CLK#, CLK	LVPECL output	Differential clock output

Frequency Table

Inputs		PLL Multiplier Value	Output Frequency (MHz)
Crystal Frequency (MHz)	F_SEL		
25	0	5	125
	1	2.5	62.5

Absolute Maximum Conditions

Parameter	Description	Conditions	Min	Max	Unit
V _{DD}	Supply Voltage		-0.5	4.4	V
V _{IN} ^[1]	Input Voltage, DC	Relative to V _{SS}	-0.5	V _{DD} + 0.5	V
T _S	Temperature, Storage	Non operating	-65	150	°C
T _J	Temperature, Junction		-	135	°C
ESD _{HBM}	ESD Protection, Human Body Model	JEDEC STD 22-A114-B	2000	-	V
UL-94	Flammability Rating	At 1/8 in.	V-0		
Θ _{JA} ^[2]	Thermal Resistance, Junction to Ambient	0 m/s airflow	100		°C/W
		1 m/s airflow	91		
		2.5 m/s airflow	87		

Operating Conditions

Parameter	Description	Min	Max	Unit
V _{DD}	3.3 V Supply Voltage	3.135	3.465	V
	2.5 V Supply Voltage	2.375	2.625	V
T _A	Ambient Temperature, Commercial	0	70	°C
	Ambient Temperature, Industrial	-40	85	°C
T _{PU}	Power up time for all V _{DD} to reach minimum specified voltage (ensure power ramps is monotonic)	0.05	500	ms

Notes

1. The voltage on any input or IO pin cannot exceed the power pin during power up.
2. Simulated using Apache Sentinel TI software. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has 4-layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.

DC Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I _{DD}	Operating Supply Current with output unterminated	V _{DD} = 3.465 V, F _{OUT} = 125 MHz, output unterminated	–	–	125	mA
		V _{DD} = 2.625 V, F _{OUT} = 125 MHz, output unterminated	–	–	120	mA
I _{DDT}	Operating Supply Current with output terminated	V _{DD} = 3.465 V, F _{OUT} = 125 MHz, output terminated	–	–	150	mA
		V _{DD} = 2.625 V, F _{OUT} = 125 MHz, output terminated	–	–	145	mA
V _{OH}	LVPECL Output High Voltage	V _{DD} = 3.3 V or 2.5 V, R _{TERM} = 50 Ω to V _{DD} – 2.0 V	V _{DD} – 1.15	–	V _{DD} – 0.75	V
V _{OL}	LVPECL Output Low Voltage	V _{DD} = 3.3 V or 2.5 V, R _{TERM} = 50 Ω to V _{DD} – 2.0 V	V _{DD} – 2.0	–	V _{DD} – 1.625	V
V _{OD1}	LVPECL Peak-to-Peak Output Voltage Swing	V _{DD} = 3.3 V or 2.5 V, R _{TERM} = 50 Ω to V _{DD} – 2.0 V	600	–	1000	mV
V _{OD2}	LVPECL Output Voltage Swing (V _{OH} – V _{OL})	V _{DD} = 2.5 V, R _{TERM} = 50 Ω to V _{DD} – 1.5 V	500	–	1000	mV
V _{OCM}	LVPECL Output Common Mode Voltage (V _{OH} + V _{OL})/2	V _{DD} = 2.5 V, R _{TERM} = 50 Ω to V _{DD} – 1.5 V	1.2	–	–	V
V _{IH}	Input High Voltage, F_SEL		0.7 × V _{DD}	–	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage, F_SEL		–0.3	–	0.3 × V _{DD}	V
I _{IH}	Input High Current, F_SEL	F_SEL = V _{DD}	–	–	115	μA
I _{IL}	Input Low Current, F_SEL	F_SEL = V _{SS}	–50	–	–	μA
C _{IN} ^[3]	Input Capacitance, F_SEL		–	15	–	pF
C _{INX} ^[3]	Pin Capacitance, XIN & XOUT		–	4.5	–	pF

Note

3. Not 100% tested, guaranteed by design and characterization.

AC Electrical Characteristics

Parameter ^[4]	Description	Conditions	Min	Typ	Max	Unit
F _{OUT}	Output Frequency		62.5	–	125	MHz
T _R , T _F	Output Rise or Fall Time	20% to 80% of full output swing	–	0.5	1.0	ns
T _{Jitter(φ)}	RMS Phase Jitter (Random)	125 MHz, (1.875–20 MHz)	–	0.4	–	ps
T _{DC}	Output Duty Cycle	Measured at zero crossing point	48	50	52	%
T _{LOCK}	Startup Time	Time for CLK to reach valid frequency measured from the time V _{DD} = V _{DD(min.)}	–	–	5	ms
T _{LFS}	Re-lock Time	Time for CLK to reach valid frequency from F_SEL pin change	–	–	1	ms

Recommended Crystal Specifications

Parameter ^[5]	Description	Min	Max	Unit
Mode	Mode of Oscillation	Fundamental		
F	Frequency	25	25	MHz
ESR	Equivalent Series Resistance	–	50	Ω
C ₀	Shunt Capacitance	–	7	pF

Notes

4. Not 100% tested, guaranteed by design and characterization.
5. Characterized using an 18 pF parallel resonant crystal.

Parameter Measurements

Figure 2. 3.3 V Output Load AC Test Circuit

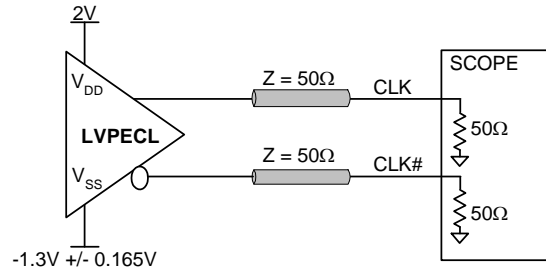


Figure 3. 2.5 V Output Load AC Test Circuit

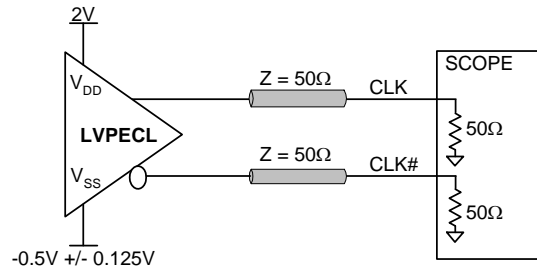


Figure 4. Output DC Parameters

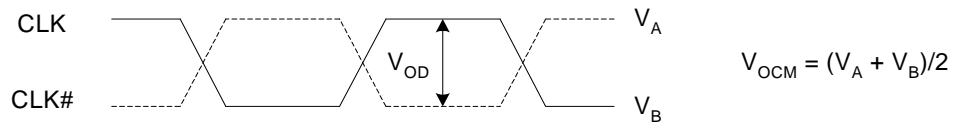
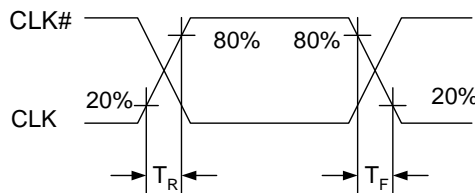


Figure 5. Output Rise and Fall Time



Parameter Measurements (continued)

Figure 6. RMS Phase Jitter

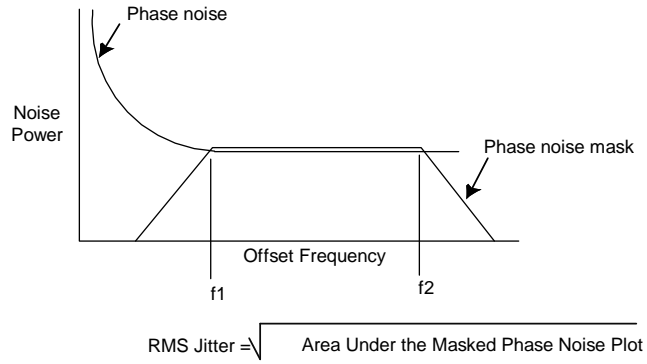
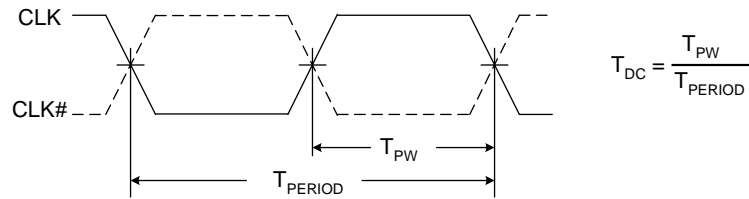


Figure 7. Output Duty Cycle

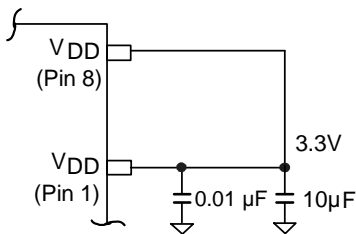


Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, noise at the power supply pins can degrade performance. To achieve optimum jitter performance, use good power supply isolation practices. Figure 8 illustrates a typical filtering scheme. Since all the current flows through pin 1, the resistance and inductance between this pin and the supply is minimized. A 0.01 or 0.1 μF ceramic chip capacitor is also located close to this pin to provide a short and low impedance AC path to ground. A 1 to 10 μF ceramic or tantalum capacitor is located in the general vicinity of this device and may be shared with other devices.

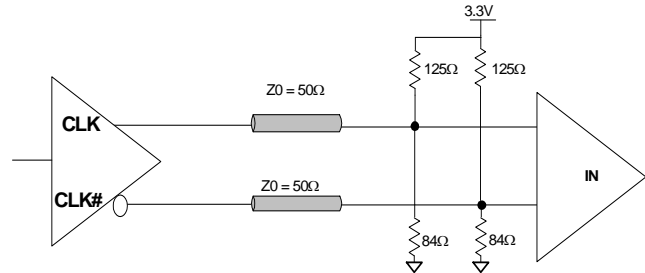
Figure 8. Power Supply Filtering



Termination for LVPECL Output

The CY2XP22 implements its LVPECL driver with a current steering design. For proper operation, it requires a 50 ohm dc termination on each of the two output signals. For 3.3 V operation, this data sheet specifies output levels for termination to $V_{DD} - 2.0\text{ V}$. This same termination voltage can also be used for $V_{DD} = 2.5\text{ V}$ operation, or it can be terminated to $V_{DD} - 1.5\text{ V}$. Note that it is also possible to terminate with 50 ohms to ground (V_{SS}), but the high and low signal levels differ from the data sheet values. Termination resistors are best located close to the destination device. To avoid reflections, trace characteristic impedance (Z_0) should match the termination impedance. Figure 9 shows a standard termination scheme.

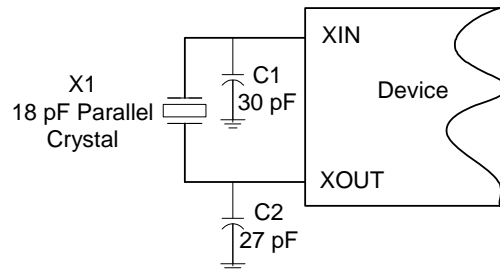
Figure 9. LVPECL Output Termination



Crystal Interface

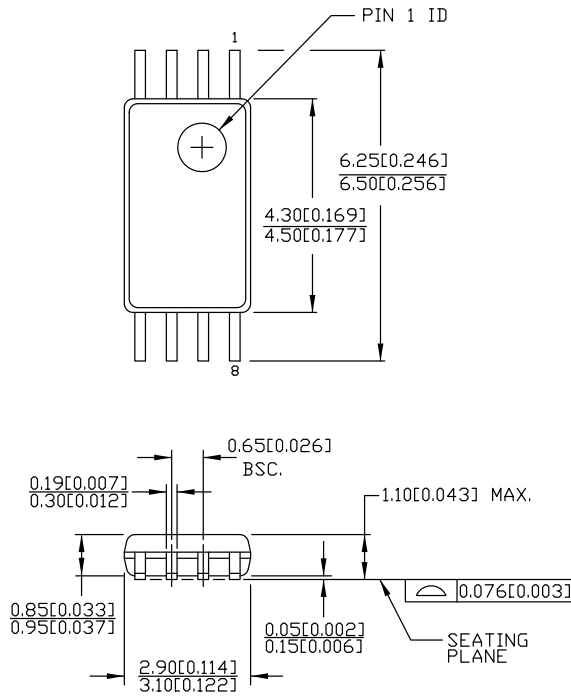
The CY2XP22 is characterized with 18 pF parallel resonant crystals. The capacitor values shown in Figure 10 are determined using a 25 MHz 18 pF parallel resonant crystal and are chosen to minimize the ppm error. Note that the optimal values for C1 and C2 depend on the parasitic trace capacitance and are thus layout dependent.

Figure 10. Crystal Input Interface



Package Drawing and Dimensions

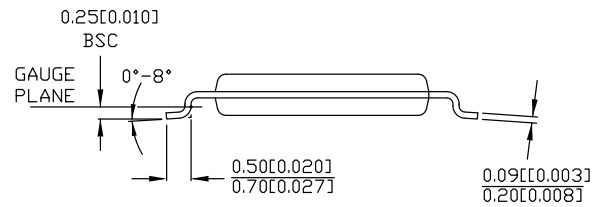
Figure 11. 8-pin TSSOP (4.40 mm Body) Package Outline, 51-85093



DIMENSIONS IN MM [INCHES] MIN. MAX.

REFERENCE JEDEC MO-153

PART #	
Z08.173	STANDARD PKG.
ZZ08.173	LEAD FREE PKG.



51-85093 *D

Acronyms

Acronym	Description
CLKOUT	Clock Output
CMOS	Complementary Metal Oxide Semiconductor
DPM	Die Pick Map
EPROM	Erasable Programmable Read Only Memory
LVDS	Low-Voltage Differential Signaling
LVPECL	Low-Voltage Positive Emitter Coupled Logic
NTSC	National Television System Committee
OE	Output Enable
PAL	Phase Alternate Line
PD	Power-Down
PLL	Phase Locked Loop
TTL	Transistor-Transistor Logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
μA	microampere
μs	microsecond
μV	microvolt
μVrms	microvolts root-mean-square
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
ppm	parts per million
V	volt

Document History Page

Document Title: CY2XP22, Crystal to LVPECL Clock Generator				
Document Number: 001-10229				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	506262	RGL	See ECN	New data sheet
*A	838060	RGL	See ECN	Changed status from Advance to Preliminary
*B	2700242	KVM / PYRS	04/30/2009	Reformatted Revised phase noise values Replaced VCC with VDD; VEE with VSS; updated pin names Removed pull-up resistor on F_SEL Corrected temperature range, added industrial temperature range Increased IDD from 120 / 100 mA to 150 / 140 mA Added CINX parameter, revised CIN parameter Revised LVPECL output specs Added thermal resistance information Changed VIL, VIH, IIL & IIH specs Revised suggested crystal load capacitor values
*C	2718898	WWZ	06/15/09	Minor ECN to post data sheet to external web
*D	2767298	KVM	09/22/09	Add I _{DD} spec for unterminated outputs Change parameter name for I _{DD} (terminated outputs) from I _{DD} to I _{DDT} Remove I _{DD} footnote about externally dissipated current Add footnote reference to C _{IN} and C _{INX} :not 100% tested Add max limit for T _R , T _F : 1.0 ns Change T _{LOCK} max from 10 ms to 5 ms Split out parameter T _{LFS} from T _{LOCK}
*E	2896121	KVM	03/19/2010	Updated Package Diagram (Figure 11)
*F	3219081	BASH	04/07/2011	Changed status from preliminary to final. Added ordering code definitions. Updated package diagram to *C. Added Acronyms, and Units of Measure. Template and style updates as per current Cypress standards.
*G	4336622	XHT	05/02/2014	spec 51-85093 – Changed revision from *C to *D. Updated in new template. Completing Sunset Review.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC[®] Solutions

[psoc.cypress.com/solutions](#)
[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

Technical Support

[cypress.com/go/support](#)

© Cypress Semiconductor Corporation, 2006-2014. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and/or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.