THIS SPEC IS OBSOLETE

Spec No.: 001-42225

Spec Title: CY28517 PCI EXPRESS CLOCK GENERATOR

Sunset Owner: Christopher Martin (CXQ)

Replaced by: NONE

CY28517

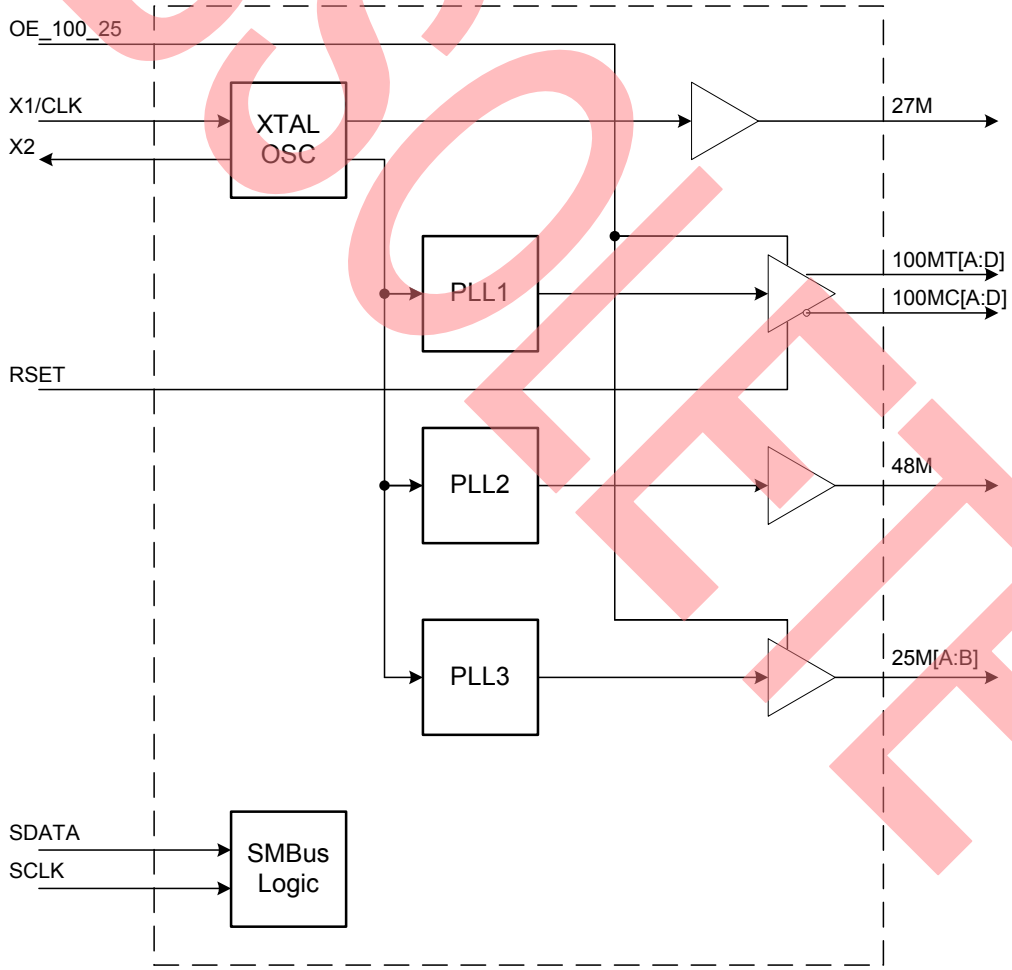
PCI Express Clock Generator

Features

- Four 100 MHz differential clocks
- 48 MHz clock
- Two 25 MHz clocks
- 27 MHz Reference Clock
- OE control per clock output
- Selectable drive strength per output
- Selectable, Triangle, and Lexmark profiles
- SMbus support with readback capabilities
- 3.3V power supply
- Packages are Pb free and ROHS compliant
- 28-pin TSSOP packages

100M	25M	27M	48M
x4	x2	x 1	x 1

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram - 28 Pin TSSOP

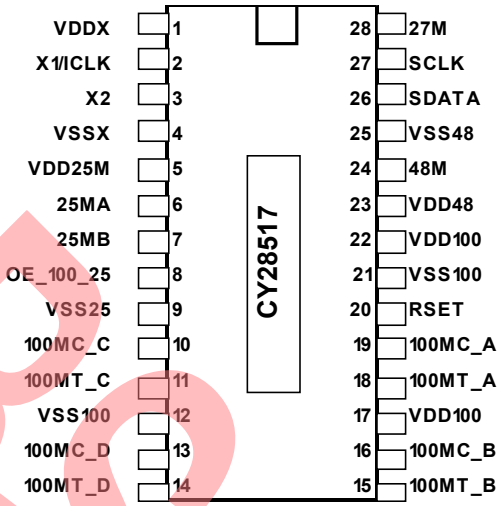


Table 1. Pin Definitions - 28 Pin TSSOP

Pin No.	Name	Type	Description
1	VDDX	PWR	**3.3V Power Supply for XTAL and REF**
2	X1/ICLK	I	**27 MHz Crystal Input/ Clock Input**
3	X2	O, SE	**27 MHz Crystal Output**
4	VSSX	PWR	**Ground for XTAL and REF**
5	VDD25	PWR	**3.3V Power Supply for 25 MHz Outputs**
6,7	25M[A:B]	O, SE	**25 MHz Clock**
8	OE_100_25	I, PD	**Input for Enabling/Disabling 25 MHz [A:B] and 100 MHz [A:D] Clock**. It is a high true signal and has an internal pull down resistor with value >100 KOhms.
9	VSS25	PWR	**Ground for 25 MHz Outputs**
10, 11, 13, 14, 15, 16, 18, 19	100MT/C[A:D]	O, DIF	**Differential 100 MHz Clocks** Intel Type-X buffer.
12, 21	VSS100	PWR	**Ground for 100 MHz Outputs**
17, 22	VDD100	PWR	**3.3V Power Supply for 100 MHz Outputs**
20	RSET	I	A Precision resistor is attached to this pin, which is connected to the internal current reference
23	VDD48	PWR	**3.3V Power Supply for 48 MHz Outputs**
24	48M	O, SE	**48 MHz Clock**
25	VSS25	PWR	**Ground for 48 MHz Outputs**
26	SDATA	IO	**SMBus Compatible SDATA**
27	SCLK	I	**SMBus Compatible SCLOCK**
28	27M	O, SE	**Reference Clock**. 3.3V 27 MHz clock output

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. This is a RAM based technology which does not keep its value when power is off or during a power transition.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write or read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 2*.

The block write and block read protocol is outlined in *Table 3* while *Table 4* on page 4 outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h) for write and 11010011(D3h) for read.

Table 2. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

Table 3. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8-bit '00000000' stands for block operation	11:18	Command Code – 8-bit '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 0 – 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
	Data Byte N/Slave Acknowledge...	39:46	Data byte from slave – 8 bits
	Data Byte N – 8 bits	47	Acknowledge
	Acknowledge from slave	48:55	Data byte from slave – 8 bits
	Stop	56	Acknowledge
			Data bytes from slave/Acknowledge
			Data byte N from slave – 8 bits
			Not Acknowledge
			Stop

Table 4. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '1xxxxxxx' stands for byte operation, bits[6:0] of bits[6:0] the command code represents the offset of the byte to be accessed	11:18	Command Code – 8 bits '1xxxxxxx' stands for byte operation, of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte from master – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29	Stop	28	Read = 1
		29	Acknowledge from slave
		30:37	Data byte from slave – 8 bits
		38	Not Acknowledge
		39	Stop

Control Registers

Byte 0:Control Register 0

Bit	@Pup	Name	Description
7	1	27M	27M Output Enable 0 = Disable (Hi-Z), 1 = Enable
6	1	48M	48M Output Enable 0 = Disable (Hi-Z), 1 = Enable
5	1	25M_B	25M_B Output Enable 0 = Disable (Hi-Z), 1 = Enable
4	1	25M_A	25M_A Output Enable 0 = Disable (Hi-Z), 1 = Enable
3	1	100M[T/C]D	100M[T/C]D Output Enable 0 = Disable (Hi-Z), 1 = Enable
2	1	100M[T/C]C	100M[T/C]C Output Enable 0 = Disable (Hi-Z), 1 = Enable
1	1	100M[T/C]B	100M[T/C]B Output Enable 0 = Disable (Hi-Z), 1 = Enable
0	1	100M[T/C]A	100M[T/C]A Output Enable 0 = Disable (Hi-Z), 1 = Enable

Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	1	100M_D_Drive Strength	Choose 100M[A;D] RSET Multiplier 0 - 2X, 1 - 6X
6	0	Reserved	Reserved, Set = 0
5	0	Reserved	Reserved, Set = 0
4	0	Reserved	Reserved, Set = 0
3	0	Reserved	Reserved, Set = 0

Byte 1: Control Register 1 (continued)

Bit	@Pup	Name	Description
2	0	Spread Control	
1	0		
0	0	100M Spread Enable	PLL1 Spread Spectrum Enable 0 = Spread off, 1 = Spread on

Bit2	Bit1	Spread Value
0	0	-0.35 Triangular
0	1	-0.50 Triangular
1	0	-0.35 Lexmark
1	1	-0.50 Lexmark

Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Byte 3: Control Register 3

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	1	Reserved	Reserved
6	1	Reserved	Reserved
5	1	Reserved	Reserved
4	1	Reserved	Reserved
3	1	Reserved	Reserved
2	1	VCO Frequency Control	Must set this bit to 0 after power up to ensure proper operation of the device
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Byte 6: Vendor ID Register

Bit	@Pup	Name	Description
7	0	Read Only	Revision Code Bit 3
6	0	Read Only	Revision Code Bit 2
5	0	Read Only	Revision Code Bit 1
4	0	Read Only	Revision Code Bit 0
3	1	Read Only	Vendor ID Bit 3
2	0	Read Only	Vendor ID Bit 2
1	0	Read Only	Vendor ID Bit 1
0	0	Read Only	Vendor ID Bit 0

Crystal Recommendations

The CY28517 requires a Parallel Resonance Crystal. Substituting a series resonance crystal causes the CY28517 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300 ppm frequency shift between series and parallel crystals due to incorrect loading.

Table 5. Crystal Recommendations

Frequency (Fund)	Cut	Load Cap	Eff Series Rest	Drive (Max)	Tolerance (Max)	Stability (Max)	Aging (Max)
27.00 MHz	Parallel	18 pF	30 Ohm	50 µW	30 ppm	10 ppm	5 ppm/Yr

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance of the crystal must be considered to calculate the appropriate capacitive loading (CL).

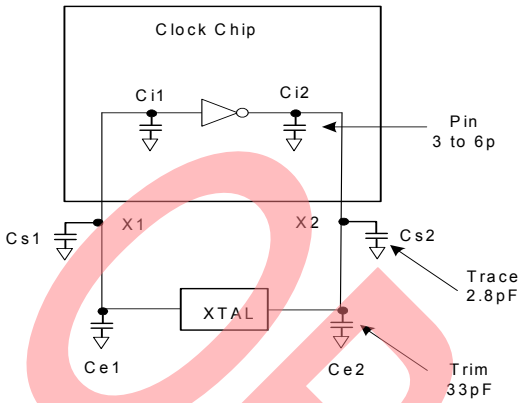
Figure 2 on page 7 shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It's a common misconception that load capacitors are in parallel with the crystal and must be approximately equal to the load capacitance of the crystal. This is not true.

Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading.

As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) must be calculated to provide equal capacitive loading on both sides.

Figure 2. Crystal Loading Example



Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 * CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL ..... Crystal load capacitance

CLe ..... Actual loading seen by crystal using standard value trim capacitors

Ce ..... External trim capacitors

Cs ..... Stray capacitance (terraced)

Ci ..... Internal capacitance

Output Enable

The Output Enable (OE_100_25) signal is active HIGH input used for clean stopping and starting the selected 100M and 25M outputs. To recognize as a valid assertion or deassertion, the signal is a debounced signal in that its state must remain unchanged during two consecutive rising edges of 25 MHz.

The assertion and deassertion of this signal is absolutely asynchronous.

Output Enable Deassertion

Upon deasserting the Output Enable pin (OE_100_25) all 100M/25M outputs are stopped after their next transition. The final state of all stopped 100M/25M signals is LOW.

Output Enable Assertion

All 100 MHz/25 MHz outputs that were stopped resumes normal operation in a glitch free manner. The maximum latency from the assertion to active outputs is between 2–6 clock periods of 100 MHz/25 MHz with all 100M/25M outputs resuming simultaneously.

Table 6. Output Enable Table

Output Enable	27M	48M	25M[A:B]	100MT/C[A:D]
0	On	On	Low	Hi-Z
1	On	On	On	On

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non-functional	–65	150	°C
T_A	Temperature, Operating Ambient	Functional	5	65	°C
T_J	Temperature, Junction	Functional	–	150	°C
T_{SOL}	Pb free Soldering Process Temperature		–	260	°C
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V
UL-94	Flammability Rating	At 1/8 in.	V–0		
MSL	Moisture Sensitivity Level		1		
Multiple Supplies: The voltage on any input or IO pin cannot exceed the power pin during power up. Power supply sequencing is NOT required.					

DC Electrical Specifications

Parameter	Description	Condition	Min	Max	Unit
VDD	3.3V Operating Voltage		3.0	3.6	V
V_{ILI2C}	Input Low Voltage	SDATA, SCLK	–	1.0	V
V_{IHI2C}	Input High Voltage	SDATA, SCLK	2.2	–	V
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.0	3.6	V
I_{IL}	Input Low Leakage Current	Except internal pull up resistors, $0 < V_{IN} < V_{DD}$	–5		µA
I_{IH}	Input High Leakage Current	Except internal pull down resistors, $0 < V_{IN} < V_{DD}$		5	µA
V_{OL}	Output Low Voltage	I_{OL} = 1 mA	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1 mA	2.4	–	V
I_{OZ}	High impedance Output Current		–10	10	µA
C_{IN}	Input Pin Capacitance		2	5	pF
C_{OUT}	Output Pin Capacitance		3	6	pF
L_{IN}	Pin Inductance		–	7	nH
V_{XIH}	Xin High Voltage		$0.7V_{DD}$	V_{DD}	V
V_{XIL}	Xin Low Voltage		0	$0.3V_{DD}$	V
$I_{DD3.3V}$	Dynamic Supply Current	At max load and freq per *Figure 4*	–	225	mA
$I_{PD3.3V}$	Power down Supply Current	Outputs disabled and no power applied to VDD25 and VDD100	–	60	mA

AC Electrical Specifications

Parameter	Description	Condition	Min	Typ.	Max	Unit
27M Output Characteristics						
F_{CLOCK}	Clock Frequency			27		MHz
T_{DC}	XIN Duty Cycle	The device operates reliably with input duty cycles up to 30/70 but the REF clock duty cycle is not within specification	45	–	55	%
T_{PERIOD}	XIN Period	When XIN is driven from an external clock source	37.0259	–	37.0481	ns
T_R / T_F	XIN Rise and Fall Times	Measured between 20% and 80% of V_{OD}	1	–	3	ns
T_{CCJ}	XIN Cycle to Cycle Jitter	Measured at 1.5V	–200	–	200	ps
L_{TJ}	Long term Jitter (peak-peak)	Measured at 1.5V with 10 µs delay	–250	–	250	ps
T_{LOCK}	Clock Stabilization from Power up		–	–	2	ms
V_{OH}	Voltage High	Math average	2.4	–	–	V
V_{OL}	Voltage Low	Math average	–	–	0.4	V
100M Output Characteristics						
F_{CLOCK}	Clock frequency		–	–	100	MHz
T_{PERIOD}	Clock period	Without spread and without jitter	10.000	–	–	ns
		Including +0.0, –0.5% spread and jitter	9.915	10.025	10.136	ns
T_{JCC}	Cycle to Cycle jitter	Peak value. Measured at crossing point with spread turned off	–85	–	85	ps
T_{JLT}	Long Term Jitter (p-p)	Measured at crossing point with 10 µs delay and spread turned off	–300	–	300	ps
SP_{range}	Spread range		–0.5	–	0.0	%
SP_{rate}	Spread rate		–	32		KHz
$SP_{profile}$	Spread profile		–	Trian-gular		

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min	Typ.	Max	Unit
T_{DC}	Duty Cycle	Measured at crossing point of the differential signal	45	–	55	%
T_R/T_F	Rise and Fall Times	Measured between 20% and 80% of the V_{OD}	175	–	700	ps
T_{RFM}	Rise/Fall Matching[1]	Determined as a fraction of $2*(T_R-T_F)/(T_R+T_F)$	–	–	20	%
V_{OX}	Crossing Point Voltage at 0.7V Swing		250	–	550	mV
ΔV_{OX}	Total Variation of V_{OX} over all edges		–	–	140	mV
V_{OH}	Voltage High[1]	Math average	600	710	850	mv
V_{OL}	Voltage Low[1]	Math average	–200	0.00	50	mv
T_{SKEW}	Output Skew	Measured at crossing point V_{OX}	–	–	250	ps
T_{LOCK}	Clock stabilization from power up		–	–	2	ms
BWattn	Closed loop BW attenuation	Measured at 500 KHz relative to corner frequency	–20	–	–	dB
25M Output Characteristics						
F_{CLOCK}	Clock frequency		–	25		MHz
T_{CCJ}	Cycle to Cycle jitter	Peak value	–200	–	200	ps
T_{JLT}	Long Term Jitter (p-p)	Measured at 1.5V with 10 µs delay	–400	–	400	ps
T_{DC}	Duty Cycle	Measured at 1.5V	45	–	55	%
T_R/T_F	Rise and Fall Times	Measured between 20% and 80% of the V_{OD} with 15 pF lumped capacitive load	1	–	3	ns
T_{LOCK}	Clock stabilization from power up		–	–	2	ms
V_{OH}	Voltage High	Math average	2.4	–	–	V
V_{OL}	Voltage Low	Math average	–	–	0.4	V
48M Output Characteristics						
F_{CLOCK}	Clock frequency		–	48		MHz
T_{CCJ}	Cycle to Cycle jitter	Peak value	–200	–	200	ps
T_{JLT}	Long Term Jitter (p-p)	Measured at 1.5V with 10 µs delay	–400	–	400	ps
T_{DC}	Duty Cycle	Measured at 1.5V	45	–	55	%
T_R/T_F	Rise and Fall Times	Measured between 20% and 80% of the V_{OD} with 15 pF lumped capacitive load	0.7	–	2	ns
T_{LOCK}	Clock stabilization from power up		–	–	2	ms
V_{OH}	Voltage High	Math average	2.4	–	–	V
V_{OL}	Voltage Low	Math average	–	–	0.4	V

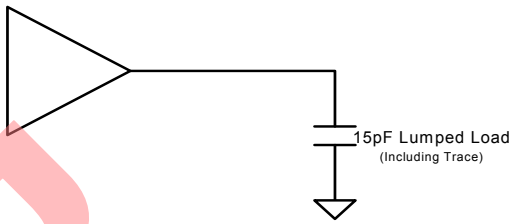
Note
1. Measured at V_{DD} = 3.3V±5%

Test and Measurement Set up

For Single ended Signals

The following diagram shows the test load configurations for the single ended output signals.

Figure 3. Single-ended Load Configuration



For Differential 100 MHz Output Signals

The following diagram shows the test load configuration for the differential CPU and SRC outputs. Trace length is 5 in. Max

Figure 4. 0.7V Single-ended Load Configuration

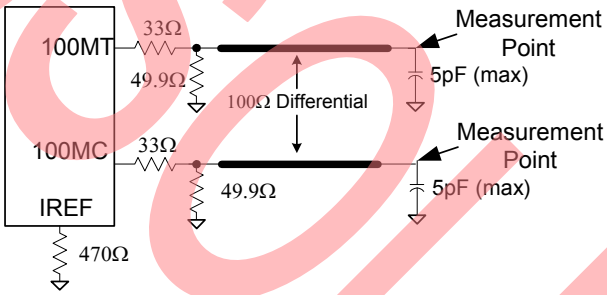


Figure 5. Single-ended Output Signals (for AC Parameters Measurement)

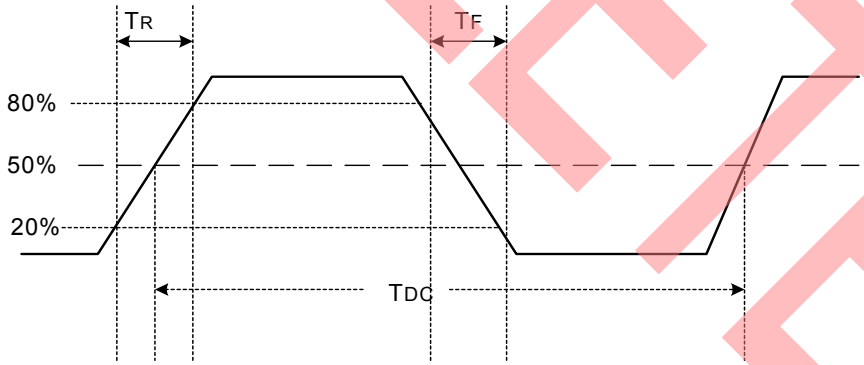
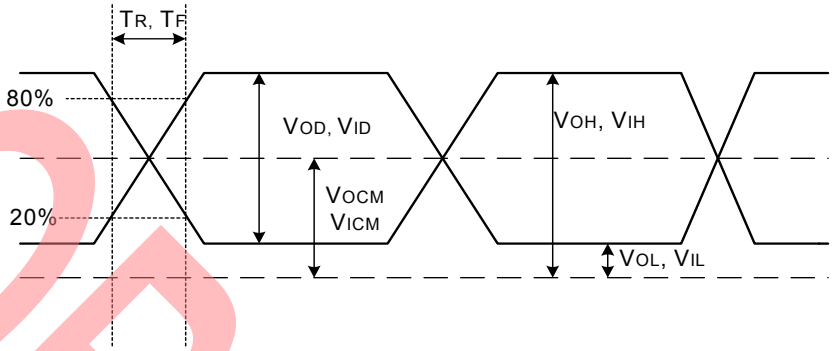


Figure 6. Differential Output Signals (for AC Parameters Measurement)

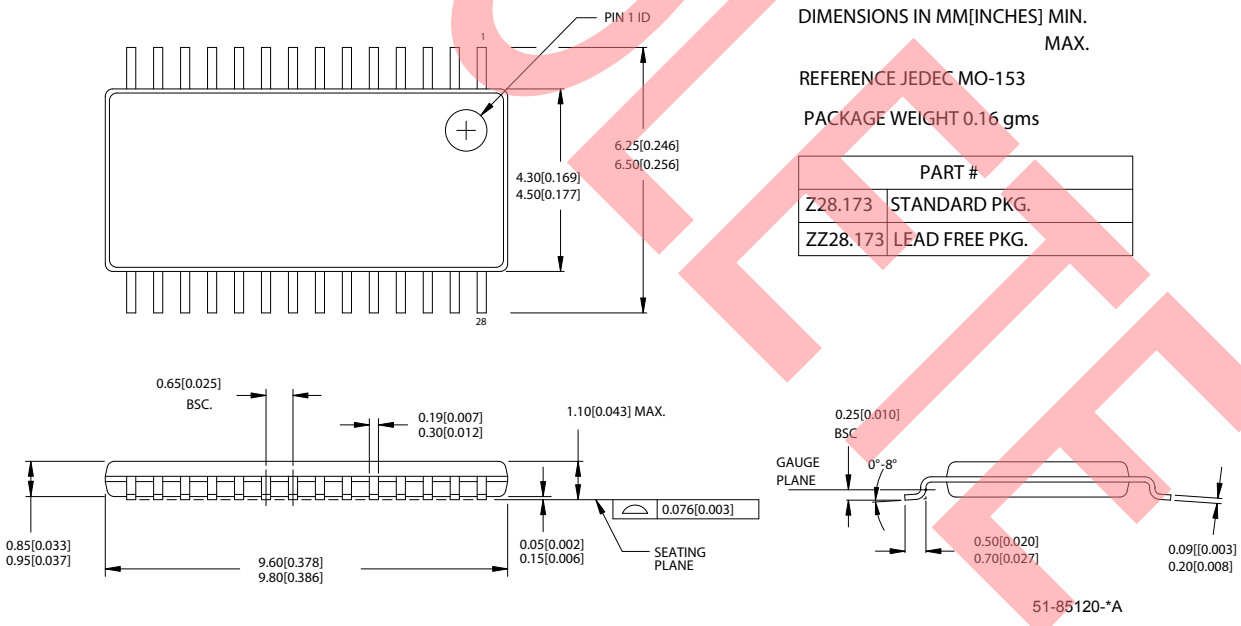


Ordering Information

Part Number	Package Type	Product Flow
Pb free		
CY28517ZXC	28 pin TSSOP	Commercial, 5° to 65°C
CY28517ZXCT	28 pin TSSOP – Tape and Reel	Commercial, 5° to 65°C

Package Drawing and Dimensions

Figure 7. 28-Lead Thin Shrunk Small Outline Package (4.40-mm Body) Z28.173



Document History Page

Document Title: CY28517 PCI Express Clock Generator Document Number: 001-42225				
REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	1664043	See ECN	WWZ/AESA	New Data Sheet
*A	1698623	See ECN	AESA	Updated Copyright
*B	2904608	04/05/2010	CXQ	Inactive part numbers; Obsolete data sheet