

LVPECL Voltage Controlled Crystal Oscillator (VCXO)

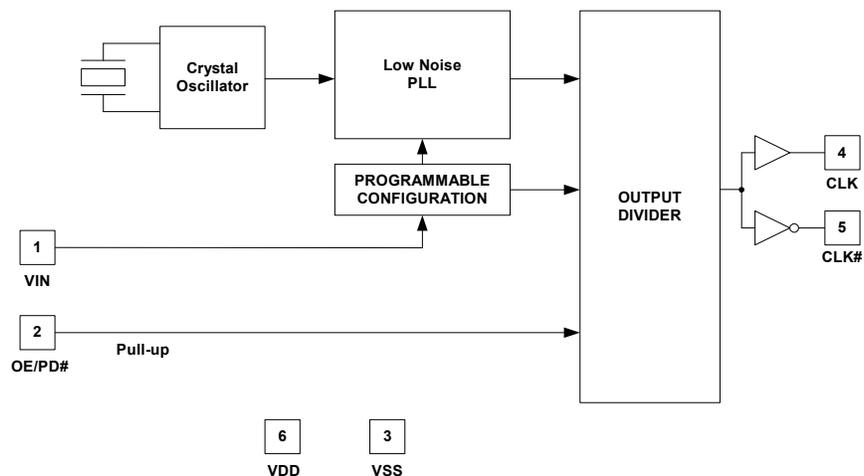
Features

- High-frequency VCXO with LVPECL output
- Any output frequency from 50 MHz to 690 MHz
- Available either factory configured or field programmable
- Integrated phase-locked loop (PLL)
- 1 ps typical RMS Phase Jitter
- Output Enable or Power-down function
- Supply voltage: 3.3 V or 2.5 V
- Pb-free package: 5.0 × 3.2 mm LCC
- Commercial and industrial temperature ranges

Benefits

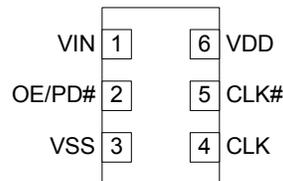
- Eliminates the need for external crystal
- Low-noise internal PLL
- Fast time to market
- Suitable for HDDs, consumer and networking applications
- Small footprint
- Application compatibility in standard and low-power systems
- Field-programmable for reduced inventory

Logic Block Diagram



Pinouts

Figure 1. 6-pin Ceramic LCC pinout



Pin Definitions

| Pin | Name | I/O Type | Description |
|------|-----------------|------------------------------|---|
| 1 | V _{IN} | Analog Input | VCXO control voltage. Positive slope. |
| 2 | OE/PD# | CMOS Input, internal pull-up | Output Enable pin: Active HIGH. If OE = 1, CLK is enabled. Power-down pin: Active LOW. If PD# = 0, Power-down is enabled. The functionality of this pin is programmable. |
| 3 | V _{SS} | Power | Power supply ground |
| 4, 5 | CLK, CLK# | Output | Clock output. LVPECL outputs. CLK# is the complement of CLK. |
| 6 | V _{DD} | Power | Positive power supply: 2.5 V or 3.3 V |

Functional Description

The CY2V014 is a high-performance high-frequency voltage-controlled crystal oscillator (VCXO).

The device uses a Cypress proprietary low-noise PLL to synthesize the frequency from an embedded crystal.

The output frequency is user adjustable by means of an analog control voltage applied to the V_{IN} pin.

VCXO Control Voltage (V_{IN}, pin 1)

V_{IN} is an analog input that is used to adjust the output frequency. The nominal output frequency is defined when V_{IN} = V_{DD}/2. Increasing the voltage on V_{IN} increases the output frequency, while decreasing the voltage on V_{IN} decreases the output frequency. Any voltage between V_{SS} and V_{DD} is allowed on V_{IN}. The voltage/frequency slope is very linear over most of the control voltage range.

Programming Description

Field-Programmable CY2V014

Field-programmable devices are shipped unprogrammed, and must be programmed before use. Customers can use CyberClocks™ Online Software to specify the device configuration and generate a .JED programming file. Programming of samples and prototype quantities is available using the CY3672 programmer. Third-party vendors manufacture programmers for small to large volume applications. Cypress's value-added distribution partners also provide programming services. Field-programmable devices are

designated with an "F" in the part number, and are intended for quick prototyping and inventory reduction.

Factory-Configured CY2V014

For customers wanting ready-to-use devices, the CY2V014 is available factory-configured, with no programming required. All requests must be submitted to the local Cypress Field Application Engineer (FAE) or sales representative. Once the request has been processed, you will receive a new part number, samples, and data sheet with the programmed values. This part number will be used for additional sample requests and production orders.

Programming Variables

Output Frequency

Any frequency between 50 MHz and 690 MHz may be specified.

Absolute Pull Range

The absolute pull range (APR) may be specified.

Pin 2: Output Enable or Power-Down (OE/PD#)

Pin 2 can be programmed as either output enable (OE) or Power-down (PD#). The OE function is used to enable or disable the CLK output very quickly, but it does not reduce core power consumption. The PD# function puts the device into a low-power state, but wake-up takes longer because the PLL must reacquire lock.

Absolute Maximum Conditions

| Parameter | Description | Condition | Min | Max | Unit |
|--------------------|-----------------------------------|-----------------------------|------|-----------------------|------|
| V _{CC} | Supply Voltage | | -0.5 | 4.4 | V |
| V _{IN} | Input Voltage | Relative to V _{SS} | -0.5 | V _{DD} + 0.5 | VDC |
| T _S | Temperature, Storage | Non Functional | -55 | 150 | °C |
| T _J | Temperature, Junction | | -40 | 125 | °C |
| ESD _{HBM} | ESD Protection (Human Body Model) | MIL-STD-883, Method 3015 | 2000 | - | V |
| UL-94 | Flammability Rating | At 1/8 in. | V-0 | | |
| MSL | Moisture Sensitivity Level | | 1 | | |

Note: The voltage on any input or I/O pin cannot exceed the power pin during power-up.

Operating Conditions

| Parameter | Description | Min | Typ | Max | Unit |
|-----------------|---|-------------|------------|-------------|------|
| V _{DD} | Supply Voltage Range | 3.0 2.25 | 3.3 2.5 | 3.6 2.75 | V |
| T _{PU} | Power-up Time for V _{DD} to Reach Minimum Specified Voltage (power ramp must be monotonic) | 0.05 | - | 500 | ms |
| T _A | Ambient Temperature (Commercial) | 0 | - | 70 | °C |
| T _A | Ambient Temperature (Industrial) | -40 | - | 85 | °C |

DC Electrical Characteristics

| Parameter | Description | Condition | Min | Typ | Max | Unit |
|------------------|--|--|------------------------|-----|-------------------------|------|
| V _{OH} | LVPECL High Output Voltage | V _{DD} = 3.3 V or 2.5 V, R _{TERM} = 50 Ω to V _{DD} - 2.0 V | V _{DD} - 1.15 | - | V _{DD} - 0.75 | V |
| V _{OL} | LVPECL Low Output Voltage | V _{DD} = 3.3 V or 2.5 V, R _{TERM} = 50 Ω to V _{DD} - 2.0 V | V _{DD} - 2.0 | - | V _{DD} - 1.625 | V |
| V _{OD1} | LVPECL Output Voltage Swing (V _{OH} - V _{OL}) | V _{DD} = 3.3 V or 2.5 V, R _{TERM} = 50 Ω to V _{DD} - 2.0 V | 600 | - | 1000 | mV |
| V _{OD2} | LVPECL Output Voltage Swing (V _{OH} - V _{OL}) | V _{DD} = 2.5 V, R _{TERM} = 50 Ω to V _{DD} - 1.4 V | 500 | - | 1000 | mV |
| V _{OCM} | LVPECL Output Common Mode Voltage (V _{OH} + V _{OL})/2 | V _{DD} = 2.5 V, R _{TERM} = 50 Ω to V _{DD} - 1.4 V | 1.2 | - | - | V |
| V _{IH} | CMOS Input High Voltage | | 0.7 × V _{DD} | - | - | V |
| V _{IL} | CMOS Input Low Voltage | | - | - | 0.3 × V _{DD} | V |
| R _{UP} | Internal Pull-up Resistor | | - | 100 | - | kΩ |
| I _{IH} | CMOS Input High Current | V _{IN} = V _{DD} | - | - | 10 | μA |
| I _{IL} | CMOS Input Low Current | V _{IN} = V _{SS} | - | - | 120 | μA |
| V _{VIN} | V _{IN} Input Voltage | | 0 | - | V _{DD} | V |
| I _{VIN} | V _{IN} Input Current | V _{SS} ≤ V _{IN} ≤ V _{DD} | - | - | 10 | μA |

DC Electrical Characteristics (continued)

| Parameter | Description | Condition | Min | Typ | Max | Unit |
|-----------|---------------------------------|--|-----|-----|-----|---------|
| L_{IN} | V_{IN} to f_{OUT} Linearity | $0.2 \times V_{DD} \leq V_{IN} \leq 0.8 \times V_{DD}$ | – | 1 | – | % |
| I_{OZ} | Output Leakage Current | Three-state output, PD#/OE = V_{SS} | –35 | – | 35 | μA |
| I_{DD} | Operating Supply Current | $V_{DD} = 3.3 V$ or $2.5 V$, CLK = 150 MHz, $C_{LOAD} = 0$, PD#/OE = V_{DD} | – | – | 100 | mA |
| I_{SB} | Standby Supply Current | PD# = V_{SS} | – | – | 1 | mA |

AC Electrical Characteristics

| Parameter | Description | Condition | Min | Typ | Max | Unit |
|--------------|--|--|-----------------------|--------|--------|------|
| f_{OUT} | Output Frequency | | 50 | – | 690 | MHz |
| FS_{FACT} | Frequency Stability – factory programmed devices | $V_{IN} = V_{DD}/2$ [1] | –60 | – | 60 | ppm |
| FS_{FIELD} | Frequency Stability – field programmable devices | $V_{IN} = V_{DD}/2$ [1] | –100 | – | 100 | ppm |
| APR | Absolute Pull Range | $V_{IN} = V_{DD}$ to V_{SS} , relative to nominal f_{OUT} , across operating temperature and voltage range [2] | ± 100 ± 50 | – – | – – | ppm |
| BW | Modulation Bandwidth (V_{IN}) | –3 dB | 10 | – | – | kHz |
| DC | Output Duty Cycle | Measured at zero crossing | 45 | 50 | 55 | % |
| T_R, T_F | Output Rise and Fall Time | 20% and 80% of full output swing | – | 350 | – | ps |
| T_{OE1} | Output Disable Time | Time from falling edge on OE to stopped outputs (Asynchronous) | – | – | 100 | ns |
| T_{OE2} | Output Enable Time | Time from rising edge on OE to outputs at a valid frequency (Asynchronous) | – | – | 100 | ns |
| T_{LOCK} | Start-up Time | Time for CLK to reach valid frequency measured from the time $V_{DD} = V_{DD}(\text{Min})$ or from PD# rising edge. | – | – | 10 | ms |
| T_{J1} | RMS Phase Jitter | $f_{OUT} = 106.25$ MHz (12 kHz–20 MHz) | – | 1 | – | ps |
| T_{J2} | Peak-to-peak Period Jitter | $f_{OUT} = 106.25$ MHz | – | 30 | – | ps |

Notes

1. Frequency stability is the maximum variation in frequency from F_0 . It includes initial accuracy, plus variation from temperature, supply voltage, shock, vibration and first year aging.
2. APR is the minimum pull range under all conditions over the device lifetime, including aging for 10 years. APR is relative to F_0 .

Switching Waveforms

Figure 2. Duty Cycle Timing ($DC = t_{1A}/t_{1B}$)

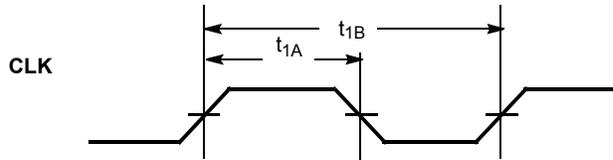


Figure 3. Output Differential Voltage

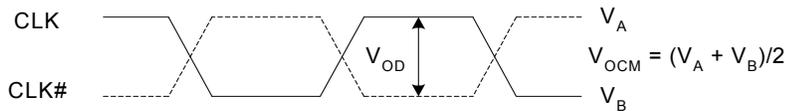
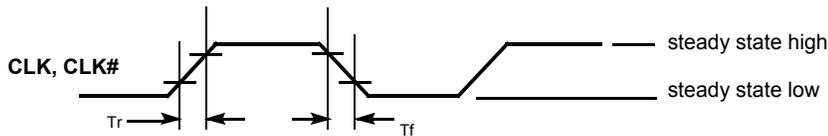
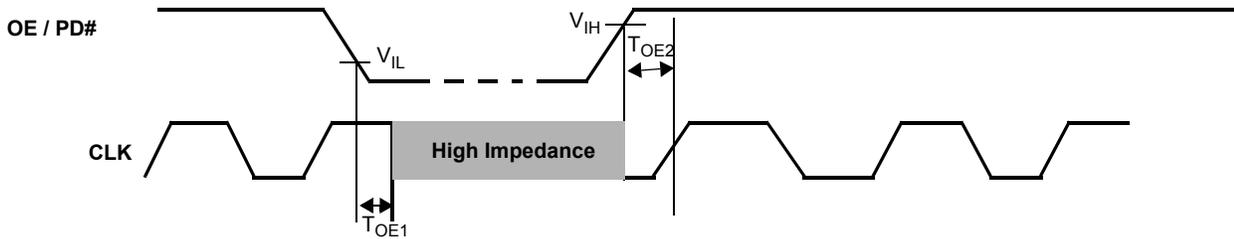


Figure 4. Output Rise/Fall Time



Output Rise time (T_r) = 20 to 80% of full output swing
 Output Fall time (T_f) = 80 to 20% of full output swing

Figure 5. Output Enable/Disable Timing



Termination Circuits

Figure 6. LVPECL Termination



Ordering Information

Table 1 lists the CY2V014 key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at <http://www.cypress.com/products>.

Table 1. Key Features and Ordering Information

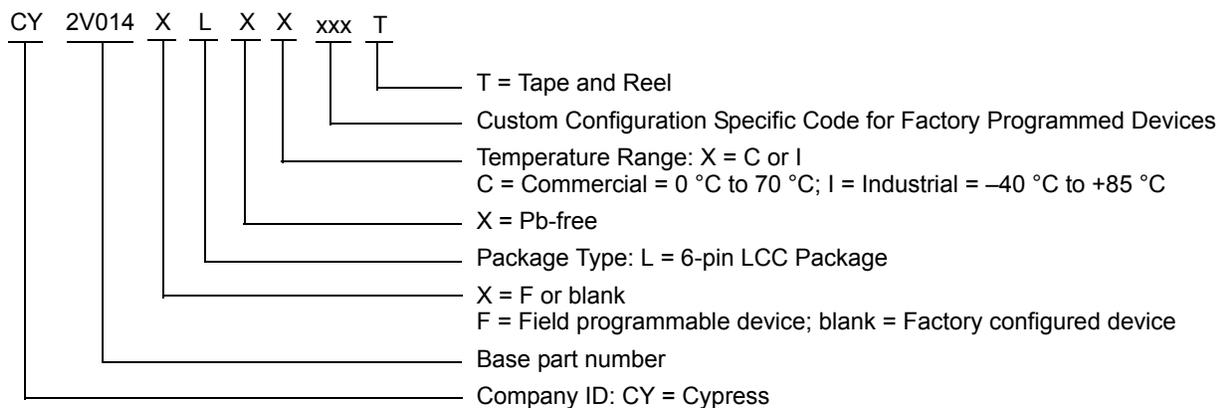
| Part Number | Configuration | Package description | Product Flow |
|----------------|--------------------|---------------------------------------|-----------------------------|
| Pb-free | | | |
| CY2V014FLXCT | Field programmable | 6-pin Ceramic LCC SMD – Tape and Reel | Commercial, 0 °C to 70 °C |
| CY2V014FLXIT | Field programmable | 6-pin Ceramic LCC SMD – Tape and Reel | Industrial, –40 °C to 85 °C |

Possible Configurations

Some product offerings are factory programmed customer specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or Sales Representative for more information.

| Part Number ^[3] | Configuration | Package description | Product Flow |
|----------------------------|--------------------|---------------------------------------|-----------------------------|
| Pb-free | | | |
| CY2V014LXCxxxT | Factory configured | 6-pin Ceramic LCC SMD – Tape and Reel | Commercial, 0 °C to 70 °C |
| CY2V014LXIxxxT | Factory configured | 6-pin Ceramic LCC SMD – Tape and Reel | Industrial, –40 °C to 85 °C |

Ordering Code Definitions

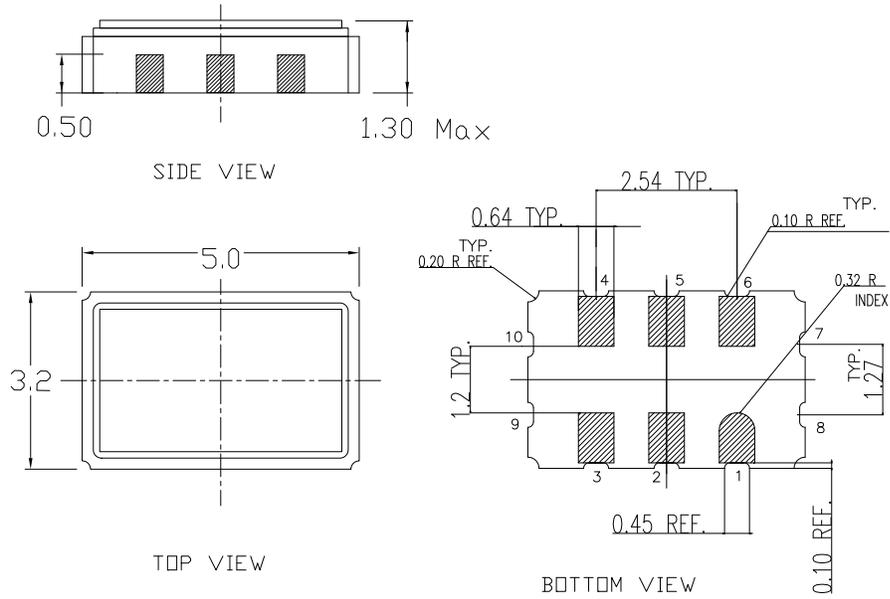


Note

3. "xxx" is a factory assigned code that identifies the programming option.

Package Diagram

Figure 7. 6-pin Ceramic LCC (5.0 × 3.2 × 1.3 mm) LZ06A Package Outline, 001-10044



Dimensions in mm
 Kyocera dwg ref KD-VA6432-A
 Package Weight ~ 0.12 grams

001-10044 *B

Acronyms

Table 2. Acronyms Used in this Document

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| ESD | Electrostatic Discharge |
| FAE | Field Applications Engineer |
| HDD | Hard Disk Drive |
| LCC | Leadless Chip Carrier |
| PLL | Phase-Locked Loop |
| RMS | Root Mean Square |
| SMD | Surface Mount Device |
| VCXO | Voltage-Controlled Crystal Oscillator |

Document Conventions

Units of Measure

Table 3. Units of Measure

| Symbol | Unit of Measure |
|--------|-------------------|
| °C | degree Celsius |
| KHz | kilohertz |
| KΩ | kilohm |
| MHz | megahertz |
| μA | microampere |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| ns | nanosecond |
| Ω | ohm |
| ppm | parts per million |
| % | percent |
| ps | picosecond |
| V | volt |

Document History Page

| Document Title: CY2V014, LVPECL Voltage Controlled Crystal Oscillator (VCXO) Document Number: 001-06458 | | | | |
|--|---------|-----------------|-----------------|---|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 504458 | RGL | See ECN | New data sheet |
| *A | 2899939 | CXQ | 03/26/10 | Updated ordering information table. Updated package diagram. Updated copyright section. |
| *B | 3099970 | CXQ | 12/02/10 | Changed from Preliminary to Final. Changed 700 MHz to 690 MHz in second "Features" bullet. Changed from 700 MHz to 690 MHz in "Programming Variables" section Changed fOUT spec in AC specifications table from 700 max to 690 max. Changed FSfact in AC specifications from +/-60 ppm max to -60ppm min and 60 ppm max. Changed FSfield spec to -100 ppm min and 100 ppm max. Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated template and styles. |
| *C | 4204997 | CINM | 11/28/2013 | Updated Package Diagram : spec 001-10044 – Changed revision from *A to *B. Updated in new template. Completing Sunset Review. |

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