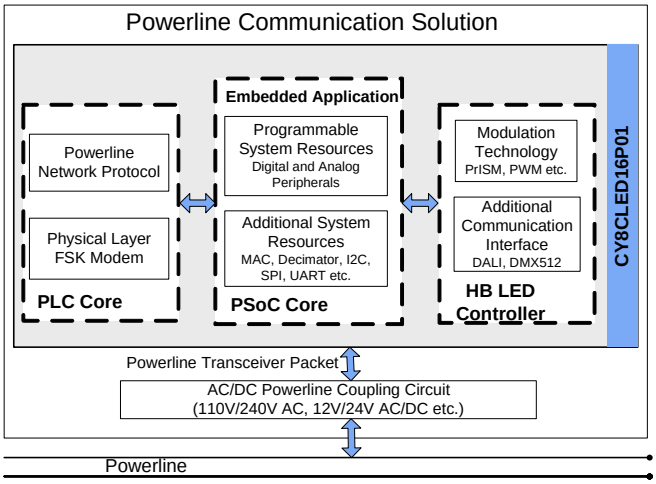
CY8CLED16P01

Powerline Communication Solution

Features

- Powerline Communication Solution
  - Integrated Powerline Modem PHY
  - Frequency Shift Keying Modulation
  - Configurable baud rates up to 2400 bps
  - Powerline Optimized Network Protocol
  - Integrates Data Link, Transport, and Network Layers
  - Supports Bidirectional Half Duplex Communication
  - 8-bit CRC Error Detection to Minimize Data Loss
  - I^2C enabled Powerline Application Layer
  - Supports I^2C Frequencies of 50, 100, and 400 kHz
  - Reference Designs for 110 V/240 V AC and 12 V/24 V AC/DC Powerlines
  - Reference Designs comply with CENELEC EN 50065-1:2001 and FCC Part 15
- HB LED Controller
  - Configurable Dimmers Support up to 16 Independent LED Channels
  - 8 to 32 bits of Resolution per Channel
  - PrISM™ Modulation technology to reduce radiated EMI and Low Frequency Blinking
  - Additional communication interfaces for lighting control such as DALI, DMX512 etc.
- Powerful Harvard Architecture Processor
  - M8C Processor Speeds to 24 MHz
  - Two 8x8 Multiply, 32-bit Accumulate
- Programmable System Resources (PSoC® Blocks)
  - 12 Rail-to-Rail Analog PSoC Blocks provide:
    - Up to 14-bit ADCs
    - Up to 9-bit DACs
    - Programmable Gain Amplifiers
    - Programmable Filters and Comparators
  - 16 Digital PSoC Blocks provide:
    - 8 to 32-bit Timers, Counters, and PWMs
    - CRC and PRS Modules
    - Up to Four Full Duplex UARTs
    - Multiple SPI™ Masters or Slaves
    - Connectable to all GPIO Pins
  - Complex Peripherals by Combining Blocks
- Flexible On-Chip Memory
  - 32 KB Flash Program Storage 50,000 Erase or Write Cycles
  - 2 KB SRAM Data Storage
  - EEPROM Emulation in Flash
- Programmable Pin Configurations
  - 25 mA Sink, 10 mA Source on all GPIOs
  - Pull Up, Pull Down, High Z, Strong, or Open-drain Drive Modes on all GPIOs
  - Up to 12 Analog Inputs on GPIO
  - Configurable Interrupt on all GPIO
- Additional System Resources
  - I^2C Slave, Master, and Multi-Master to 400 kHz
  - Watchdog and Sleep Timers
  - User-Configurable Low Voltage Detection
  - Integrated Supervisory Circuit
  - On-Chip Precision Voltage Reference
- Complete Development Tools
  - Free Development Software (PSoC Designer™)
  - Full Featured In-Circuit Emulator (ICE) and Programmer
  - Full Speed Emulation
  - Complex Breakpoint Structure
  - 128 KB Trace Memory
  - Complex Events
  - C Compilers, Assembler, and Link

Logic Block Diagram



Contents

PLC Functional Overview

The CY8CLED16P01 is an integrated Powerline Communication (PLC) chip with the Powerline Modem PHY and Network Protocol Stack running on the same device. Apart from the PLC core, the CY8CLED16P01 also offers Cypress's revolutionary PSoC technology that enables system designers to integrate multiple functions on the same chip.

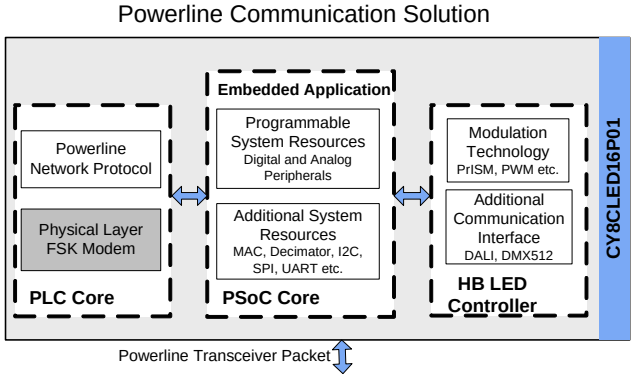
Robust Communication using Cypress's PLC Solution

Powerlines are available everywhere in the world and are a widely available communication medium for PLC technology. The pervasiveness of powerlines also makes it difficult to predict the characteristics and operation of PLC products. Because of the variable quality of powerlines around the world, implementing robust communication has been an engineering challenge for years. The Cypress PLC solution enables secure and reliable communications. Cypress PLC features that enable robust communication over powerlines include:

- Integrated Powerline PHY modem with optimized filters and amplifiers to work with lossy high voltage and low voltage powerlines.
- Powerline optimized network protocol that supports bidirectional communication with acknowledgement-based signaling. In case of data packet loss due to bursty noise on the powerline, the transmitter has the capability to retransmit data.
- The Powerline Network Protocol also supports an 8-bit CRC for error detection and data packet retransmission.
- A Carrier Sense Multiple Access (CSMA) scheme is built into the network protocol that minimizes collisions between packet transmissions on the powerline and supports multiple masters and reliable communication on a bigger network.

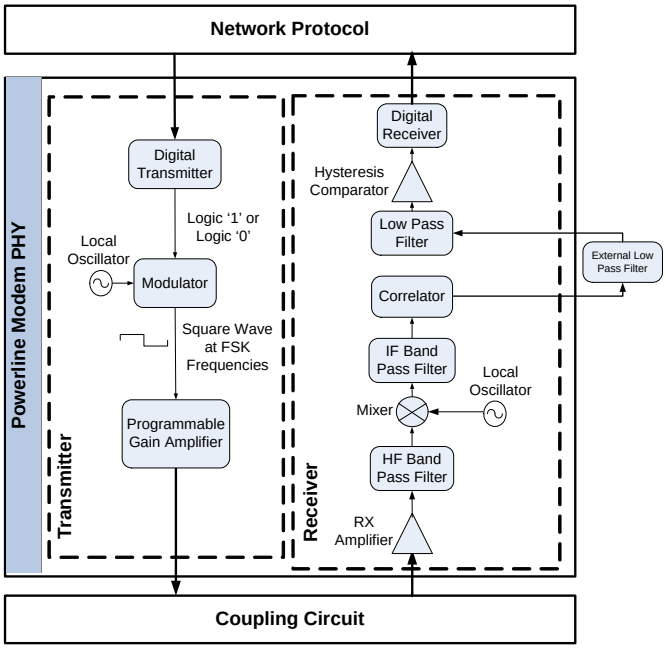
Powerline Modem PHY

Figure 1. Physical Layer FSK Modem



The physical layer of the Cypress PLC solution is implemented using an FSK modem that enables half duplex communication on any high voltage and low voltage powerline. This modem supports raw data rates up to 2400 bps. A block diagram is shown in Figure 2

Figure 2. Physical Layer FSK Modem Block Diagram



Transmitter Section

Digital data from the network layer is serialized by the digital transmitter and fed as input to the modulator. The modulator divides the local oscillator frequency by a definite factor depending on whether the input data is high level logic '1' or low level logic '0'. It then generates a square wave at 133.3 kHz (logic '0') or 131.8 kHz (logic '1'), which is fed to the Programmable Gain Amplifier to generate FSK modulated signals. This enables tunable amplification of the signal depending on the noise in the channel. The logic '1' frequency can also be configured as 130.4 kHz for wider FSK deviation.

Receiver Section

The incoming FSK signal from the powerline is input to a high frequency (HF) band pass filter that filters out-of-band frequency components and outputs a filtered signal within the desired spectrum of 125 kHz to 140 kHz for further demodulation. The mixer block multiplies the filtered FSK signals with a locally generated signal to produce heterodyned frequencies.

The intermediate frequency (IF) band pass filters further remove out-of-band noise as required for further demodulation. This signal is fed to the correlator, which produces a DC component (consisting of logic '1' and '0') and a higher frequency component.

The output of the correlator is fed to a low pass filter (LPF) that outputs only the demodulated digital data at 2400 baud and suppresses all other higher frequency components generated in the correlation process. The output of the LPF is digitized by the hysteresis comparator. This eliminates the effects of correlator delay and false logic triggers due to noise. The digital receiver deserializes this data and outputs to the network layer for interpretation.

Coupling Circuit Reference Design

The coupling circuit couples low voltage signals from the CY8CLED16P01 to the powerline. The topology of this circuit is determined by the voltage on the powerline and design constraints mandated by powerline usage regulations.

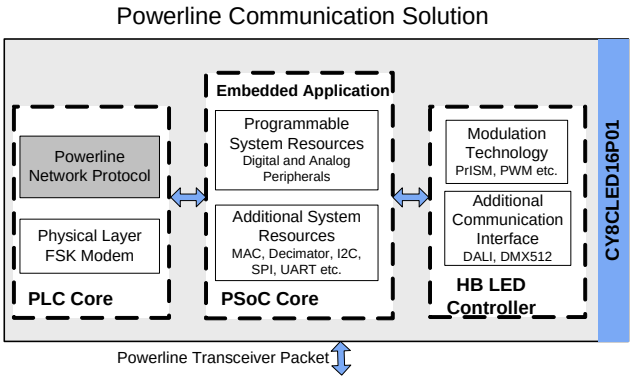
Cypress provides reference designs for a range of powerline voltages including 110 V/240 V AC and 12 V/24 V AC/DC. The CY8CLED16P01 is capable of data communication over other AC/DC Powerlines as well with the appropriate external coupling circuit. The 110 V AC and 240 V AC designs are compliant to the following powerline usage regulations:

- FCC Part 15 for North America
- EN 50065-1:2001 for Europe

Network Protocol

Cypress's powerline optimized network protocol performs the functions of the data link, network, and transport layers in an ISO/OSI-equivalent model.

Figure 3. Powerline Network Protocol



The network protocol implemented on the CY8CLED16P01 supports the following features:

- Bidirectional half duplex communication
- Master-slave or peer-to-peer network topologies
- Multiple masters on powerline network
- 8-bit logical addressing supports up to 256 powerline nodes
- 16-bit extended logical addressing supports up to 65536 powerline nodes
- 64-bit physical addressing supports up to 2^{64} powerline nodes
- Individual, broadcast or group mode addressing
- Carrier Sense Multiple Access (CSMA)
- Full control over transmission parameters
  - Acknowledged
  - Unacknowledged
  - Repeated Transmit

CSMA and Timing Parameters

- CSMA – The protocol provides the random selection of a period between 85 and 115 ms (out of seven possible values in this range). Within this period, the Band-In-Use (BIU) detector must indicate that the line is not in use, before attempting a transmission.
- BIU – A Band-In-Use detector, as defined under CENELEC EN 50065-1, is active whenever a signal that exceeds 86 dBμVrms anywhere in the range 131.5 kHz to 133.5 kHz is present for at least 4 ms. This threshold can be configured for different end-system applications not requiring CENELEC compliance.The modem tries to retransmit after every 85 to 115 ms when the band is in use. The transmitter times out after 1.1 seconds to 3 seconds (depending on the noise on the Powerline) and generates an interrupt to indicate that the transmitter was unable to acquire the powerline.

Powerline Transceiver Packet

The powerline network protocol defines a Powerline Transceiver (PLT) packet structure, which is used for data transfers between nodes across the powerline. Packet formation and data transmission across the powerline network is implemented internally in the CY8CLED16P01.

A PLT packet is divided into a variable length header (minimum 6 bytes to maximum 20 bytes, depending on address type), variable length payload (minimum 0 bytes to maximum 31 bytes), and a packet CRC byte.

This packet (preceded by a one byte preamble "0xAB") is then transmitted by the powerline modem PHY and the external coupling circuit across the powerline.

The format of the PLT packet is shown in the following table.

Table 1. Powerline Transceiver (PLT) Packet Structure

Byte Offset	Bit Offset							
	7	6	5	4	3	2	1	0
0x00	SA Type	DA Type		Service Type	RSVD	RSVD	Response	RSVD
0x01	Destination Address (8-bit Logical, 16-bit Extended Logical or 64-bit Physical)							
0x02	Source Address (8-bit Logical, 16-bit Extended Logical or 64-bit Physical)							
0x03	Command							
0x04	RSVD			Payload Length				
0x05	Seq Num				Powerline Packet Header CRC			
0x06	Payload (0 to 31 Bytes)							
	Powerline Transceiver Packet CRC							

Packet Header

The packet header contains the first 6 bytes of the packet when 1-byte logical addressing is used. When 8-byte physical addressing is used, the source and destination addresses each contain 8 bytes. In this case, the header can consist of a maximum of 20 bytes. Unused fields marked RSVD are for future expansion and are transmitted as bit 0. Table 2 describes the PLT packet header fields in detail.

Table 2. Powerline Transceiver (PLT) Packet Header

Field Name	No. of Bits	Tag	Description
SA Type	1	Source Address Type	0 – Logical Addressing 1 – Physical Addressing
DA Type	2	Destination Address Type	00 – Logical Addressing 01 – Group Addressing 10 – Physical Addressing 11 – Invalid
Service Type	1		0 – Unacknowledged Messaging 1 – Acknowledged Messaging
Response	1	Response	0 – Not an acknowledgement or response packet 1 – Acknowledgement or response packet
Seq Num	4	Sequence Number	4-bit unique identifier for each packet between source and destination.
Header CRC	4		4-bit CRC value. This enables the receiver to suspend receiving the rest of the packet if its header is corrupted

Payload

The packet payload has a length of 0 to 31 bytes. Payload content is user defined and can be read or written through I^2C.

Packet CRC

The last byte of the packet is an 8-bit CRC value used to check packet data integrity. This CRC calculation includes the header and payload portions of the packet and is in addition to the powerline packet header CRC.

Sequence Numbering

The sequence number is increased for every new unique packet transmitted. If in acknowledged mode and an acknowledgment is not received for a given packet, that packet will be re-transmitted (if TX_Retry > 0) with the same sequence number. If in unacknowledged mode, the packet will be transmitted (TX_Retry + 1) times with the same sequence number.

If the receiver receives consecutive packets from the same source address with the same sequence number and packet CRC, it does not notify the host of the reception of the duplicate packet. If in acknowledged mode, it still sends an acknowledgment so that the transmitter knows that the packet was received.

Addressing

The CY8CLED16P01 has three modes of addressing:

- Logical addressing: Every CY8CLED16P01 node can have either a 8-bit logical address or a 16-bit logical address. The logical address of the PLC Node is set by the local application or by a remote node on the Powerline.
- Physical addressing: Every CY8CLED16P01 has a unique 64-bit physical address.
- Group addressing: This is explained in the next section.

Group Membership

Group membership enables the user to multicast messages to select groups. The CY8CLED16P01 supports two types of group addressing:

- Single Group Membership – The network protocol supports up to 256 different groups on the network in this mode. In this mode, each PLC node can only be part of a single group. For example, multiple PLC nodes can be part of Group 131.
- Multiple Group Membership – The network protocol supports eight different groups in this mode and each PLC node can be a part of multiple groups. For example, a single PLC node can be a part of Group 3, Group 4, and Group 7 at the same time.

Both of these membership modes can also be used together for group membership. For example, a single PLC node can be a part of Group 131 and also multiple groups such as Group 3, Group 4, and Group 7.

The group membership ID for broadcasting messages to all nodes in the network is 0x00.

The service type is always set to Unacknowledgment Mode in Group Addressing Mode. This is to avoid acknowledgment flooding on the powerline during multicast.

Remote Commands

In addition to sending normal data over the Powerline, the CY8CPLC10 can also send (and request) control information to (and from) another node on the network. The type of remote command to transmit is set by the TX_CommandID register and when received, is stored in the RX_CommandID register.

When a control command (Command ID = 0x01 - 0x08 and 0x0C - 0x0F) is received, the protocol will automatically process the packet (if Lock_Configuration is ‘0’), respond to the initiator, and notify the host of the successful transmission and reception.

When the send data command (ID 0x09) or request for data command (ID 0x0A) is received, the protocol will reply with an acknowledgment packet (if TX_Service_Type = ‘1’), and notify the host of the new received data. If the initiator doesn't receive the acknowledgment packet within 500ms, it will notify the host of the no acknowledgment received condition.

When a response command (ID 0x0B) is received by the initiator within 1.5s of sending the request for data command, the protocol will notify the host of the successful transmission and reception. If the response command is not received by the initiator within 1.5s, it will notify the host of the no response received condition.

The host is notified by updating the appropriate values in the INT_Status register (including Status_Value_Change).

The command IDs 0x30-0xff can be used for custom commands that would be processed by the external host (e.g. set an LED color, get a temperature/voltage reading). The available remote

commands are described in Table 3 with the respective Command IDs.

Table 3. Remote Commands

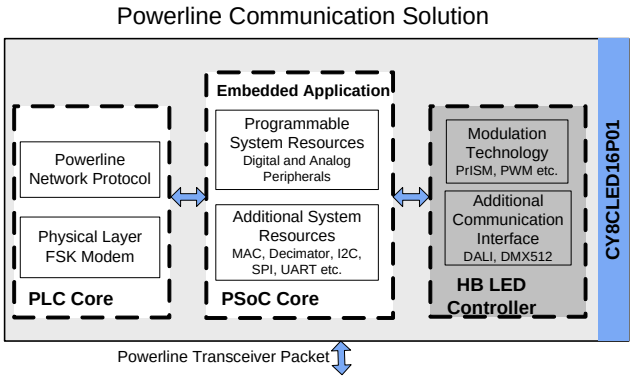
Cmd ID	Command Name	Description	Payload (TX Data)	Response (RX Data)
0x01	SetRemote_TXEnable	Sets the TX Enable bit in the PLC Mode Register. Rest of the PLC Mode register is unaffected	0 – Disable Remote TX 1 – Enable Remote TX	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x03	SetRemote_ExtendedAddr	Set the Addressing to Extended Addressing Mode	0 – Disable Extended Addressing 1 – Enable Extended Addressing	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x04	SetRemote_LogicalAddr	Assigns the specified logical address to the remote PLC Node	If Ext Address = 0, Payload = 8-bit Logical Address If Ext Address = 1, Payload = 16-bit Logical Address	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x05	GetRemote_LogicalAddr	Get the Logical Address of the remote PLC Node	None	If Remote TX Enable = 0, Response = None If Remote TX Enable = 1, {If Ext Address = 0, Response = 8-bit Logical Address If Ext Address = 1, Response = 16-bit Logical Address}
0x06	GetRemote_PhysicalAddr	Get the Physical Address of the remote PLC Node	None	If Remote TX Enable = 0, Response = None If Remote TX Enable = 1, Response = 64-bit Physical Address
0x07	GetRemote_State	Request PLC_Mode Register content from a Remote PLC Node	None	If Remote TX Enable = 0, Response = None If Remote TX Enable = 1, Response = Remote PLC Mode register
0x08	GetRemote_Version	Get the Version Number of the Remote Node	None	If TX Enable = 0, Response = None If TX Enable = 1, Response = Remote Version register
0x09	SendRemote_Data	Transmit data to a Remote Node	Payload = Local TX Data	If Local Service Type = 0, Response = None If Local Service Type = 1, Response = Ack
0x0A	RequestRemote_Data	Request data from a Remote Node	Payload = Local TX Data	If Local Service Type = 1, Response = Ack Then, the remote node host must send a ResponseRemote_Data command. The response must be completely transmitted within 1.5s of receiving the request. Otherwise, the requesting node will time out.
0x0B	ResponseRemote_Data	Transmit response data to a Remote Node.	Payload = Local TX Data	None

Table 3. Remote Commands (continued)

Cmd ID	Command Name	Description	Payload (TX Data)	Response (RX Data)
0x0C	SetRemote_BIU	Enables/Disables BIU functionality at the remote node	0 – Enable Remote BIU 1 – Disable Remote BIU	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x0D	SetRemote_ThresholdValue	Sets the Threshold Value at the Remote node	3-bit Remote Threshold Value	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x0E	SetRemote_GroupMembership	Sets the Group Membership of the Remote node	Byte0 – Remote SIngle Group Membership Address Byte1 – Remote Multiple Group Membership Address	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x0F	GetRemote_GroupMembership	Gets the Group Membership of the Remote node	None	If Remote TX Enable = 0, Response = None If Remote TX Enable = 1, Response = Byte0 - Remote SIngle Group Membership Address Byte1- Remote Multiple Group Membership Address
0x10–0x2F	Reserved			
0x30–0xFF	User Defined Command Set			

High Brightness (HB) LED Controller

Figure 4. CY8CLED16P01: HB LED Controller



The HB LED Controller is based on Cypress's EZ-Color™ technology. EZ-Color offers the ideal control solution for high brightness (HB) LED applications requiring intelligent dimming control. EZ-Color devices combine the power and flexibility of PSoC (Programmable System-on-Chip) with Cypress's PrISM™ (Precise Illumination Signal Modulation) modulation technology providing lighting designers a fully customizable and integrated lighting solution platform.

The CY8CLED16P01 supports up to 16 independent LED channels with up to 32 bits of resolution per channel, giving lighting designers the flexibility to choose the LED array size and color quality. PSoC Designer software, with lighting-specific user modules, significantly cuts development time and simplifies implementation of fixed color points through temperature and LED binning compensation. EZ-Color's virtually limitless analog and digital customization enable simple integration of features in addition to intelligent lighting, such as battery charging, image stabilization, and motor control during the development process. These features, along with Cypress's best-in-class quality and design support, make EZ-Color the ideal choice for intelligent HB LED control applications.

The list of functions that EZ-Color devices implement are:

- LED Dimming Modulation
- Pulse Density Modulation Techniques
  - DMX512
  - DALI
- Digital Communication for Lighting
- LED Temperature Compensation
- 3- and 4-Channel Color Mixing
  - Including LED Binning Compensation
- Optical Feedback Algorithms

LED Dimming Modulation

The LED Dimming modulators are an important part of any HB LED application. All EZ-Color controllers are capable of three primary types of LED dimming modulations. These are:

- Pulse Width Modulation (PWM)
- Precise Illumination Signal Modulation (PrISM)
- Delta Sigma Modulated PWM (DSPWM)

PWM is among the most commonly used and conventional methods of modulation. It is straightforward to use and effective in practice. There are two additional techniques of modulation supported by EZ-Color that are superior to using the PWM alone:

- PrISM is a modulation technique that is developed and patented by Cypress. It results in reduced EMI as compared to the PWM technique while still providing adequate dimming control for LEDs.
- The Delta Sigma Modulated PWM technique provides higher resolution while using the same hardware resources as a conventional PWM.

LED dimming modulators use digital block resources. Digital blocks are configurable 8-bit digital peripherals. There are two types of digital blocks in the CY8CLED16P01: basic and communication. Usually, there are equal numbers of each. Any communication functions must be implemented using communication blocks but basic, noncommunication functions are implemented using either kind of block.

PWM and DSPWM modulators can have a dimming resolution of up to 16 bits. A PrISM modulator can theoretically have a dimming resolution of up to 32 bits, but the maximum recommended resolution for these modulators is 13 bits. This is because the output signal of a PrISM modulator has a frequency output range that increases with the resolution of the modulator. This increase in frequency output range is undesirable as it goes beyond the switching frequency of the current driver. Therefore, a resolution of 13 bits or lower is recommended for a PrISM modulator. Refer to application note AN47372, *PrISM Technology for LED Dimming* on http://www.cypress.com, for details.

To determine the number of digital blocks used by one PWM or PrISM modulator, use Equation 1. Note that a partial digital block cannot be used, so the result must always be rounded up. In Equation 1, n is the dimming resolution of the modulator. The resolution of dimming is determined by the color accuracy needed for the end application.

$$DigBlocks_{PWM,PRISM} = \frac{n}{8} \qquad \text{Equation 1}$$

Equations 2 and 3 are used to determine how many digital blocks are needed by a DSPWM. The total dimming resolution of a DSPWM modulator is the total of the hardware PWM modulation resolution and extra resolution added by Delta Sigma modulation in the software. Equation 3 shows that the number of digital blocks needed is only determined by the hardware resolution.

$$DigBlocks_{DSPWM} = \frac{n_{HW}}{8} \qquad \text{Equation 2}$$

$$n_{Total} = n_{SW} + n_{HW} \qquad \text{Equation 3}$$

These equations show that more dimming resolution is achieved with a DSPWM modulator than with a PWM or PrISM modulator. A DSPWM modulator requires more code space and execution time to use.

Equations 1, 2, and 3 determine the number of digital blocks required by one modulator. The total number of blocks for all modulators is determined by adding up the digital blocks needed by each modulator used in the device.

The CY8CLED16P01 device has a variety of LED dimming configurations. Because it has 16 digital blocks, it can implement eight 16-bit PWM modulators, eight 12-bit PrISM modulators, or sixteen 12-bit DSPWM modulators (assuming the software resolution is 4 bits). As another example, it can implement four 10-bit PrISM modulators and still have 8 digital blocks left over to implement other digital functions.

The CY8CLED16P01 is a one-device solution for powerline communication and HB LED control. For an application that runs powerline communication and HB LED control simultaneously, the CY8CLED16P01 can implement four 16-bit PWM modulators, four 12-bit PrISM modulators, or eight 12-bit DSPWM modulators (assuming the software resolution is 4 bits).

Color Mixing Algorithm

Code algorithms to implement color mixing functionality work well with EZ-Color controllers. Color mixing algorithms convert a set of color coordinates that specify a color into the appropriate 8-bit dimming values for the LED dimming modulators. This enables the EZ-Color controller to be communicated on a higher level and maintain desired color and brightness levels.

The basic 3-channel color mixing firmware performing 8-bit LED dimming requires three 8-bit dimming blocks. The discussion on LED dimming modulation implies that it consumes three digital blocks. The addition of a simple temperature compensation algorithm using a thermistor consumes an additional digital block and analog block (for the ADC).

If the dimming resolution is increased, the number of digital blocks needed should be calculated accordingly.

LED Temperature Compensation

Many HB LED systems need to measure analog signals. One or more thermistors are often present to measure temperatures of the system and the LEDs. The CY8CLED16P01 measures an analog signal with an analog-to-digital converter (ADC). The device can implement a variety of flexible ADC implementations. The ADCs cover a wide range of resolutions and techniques and use varied number of digital and analog block resources. For help in selecting from this multitude of ADCs, refer to application note AN2239, *Analog – ADC Selection* on http://www.cypress.com. When designing with an EZ-Color device, the number of digital and analog blocks used by an ADC must be factored into the total number of digital and analog blocks that are used.

In a typical case, such as the 3-channel color mixing firmware IP developed by Cypress, the simple 8-bit incremental ADC is used. This module occupies one digital and one switched capacitor analog block.

Analog blocks come in two types: continuous time and switched capacitor blocks. The former enables continuous time functions such as comparators and programmable gain amplifiers. The switched capacitor blocks enable functions such as ADCs and filters.

Temperature sensors with an I^2C interface can also be used instead of raw thermistors, thereby eliminating the need for ADCs and complicated processing.

ColorLock Algorithm

ColorLock functionality uses feedback from an optical sensor in the system to adjust the LED dimming modulators correctly to “lock on” to a target color. This is similar to the concept of temperature compensation because it compensates for change in color. Instead of indirectly measuring change in color through temperature, it senses actual change in color and compensates for it.

The ColorLock algorithm implemented by Cypress requires the use of 10 digital blocks. Due to a 9-bit PrISM implementation, 6 digital blocks are used for dimming as in Equation 1. A 16-bit PWM and two 8-bit timers are also used to form the frame generator, pulse counter, and debounce counter.

Digital Communication

Most HB LED-based lighting systems require some form of digital communication to send and receive data to and from the light fixtures to control them. The CY8CLED16P01 is a one-device solution for HB LED lighting control and powerline communication. However, the CY8CLED16P01 supports several other data communication protocols, apart from powerline communication. These are listed in Table 4. Some of the hardware is dedicated for a protocol and does not use any digital blocks. Some protocols use digital blocks to implement the communication.

A DMX512 protocol receiver can be implemented using two digital blocks. This is a standard protocol that is common in stage and concert lighting systems. The receiver has a software programmable address and programmable number of channels that it can control. A typical DMX512 receiver implementation (developed by Cypress) controlling three LED channels consumes five digital blocks (three for the LED modulators).

Table 4. Digital Communication Resource Usage

Data Protocol	Digital Blocks	Communication Digital Blocks
DMX512 (Receiver)	2	1
DALI (Slave)	3	0
I^2C Master or Slave	0	0
Half Duplex UART	1	1
SPI Master or Slave	1	1

DALI is another lighting communication protocol that is common for large commercial buildings. The DALI slave can be implemented in EZ-Color consuming six digital blocks (three for the DALI slave and three to modulate 3 LED channels). The three blocks used to implement DALI need not be communication blocks as the Manchester encoding is performed in the software.

Apart from these specific lighting communication protocols, the industry standard communication protocols such as I^2C, UART, and SPI can be implemented in any of the devices in the family. As examples, SPI can be used to interface to external WUSB devices, while I^2C can be used to interface to external microcontrollers.

Table 4 also shows the number of digital block resources that each type of communication block consumes.

Other Functions

The CY8CLED16P01 is capable of functions other than those previously discussed. Most functions that can be implemented with a standard microcontroller can be also implemented with the CY8CLED16P01.

Similar to regular PSoC devices, the CY8CLED16P01 also has dynamic reconfiguration ability. This is a technique that enables the device’s digital and analog resources to be reused for different functions that may not be available simultaneously. For instance, consider the application to remotely control LED color/intensity (with current feedback) over powerlines using the CY8CLED16P01 for both PLC and LED color control. The PLC functionality and the current feedback do not necessarily need to happen at the same time. Therefore, the digital and analog blocks that implement the PLC functionality can dynamically reconfigure into resources that implement current feedback. By doing this, the CY8CLED16P01 device gets more functionality out of a fixed number of resources than would otherwise be possible. The only constraint on this technique is the amount of Flash and SRAM size required for the code to implement these functions. For more details on dynamic reconfiguration, refer to application note AN2104, *PSoC Dynamic Reconfiguration*.

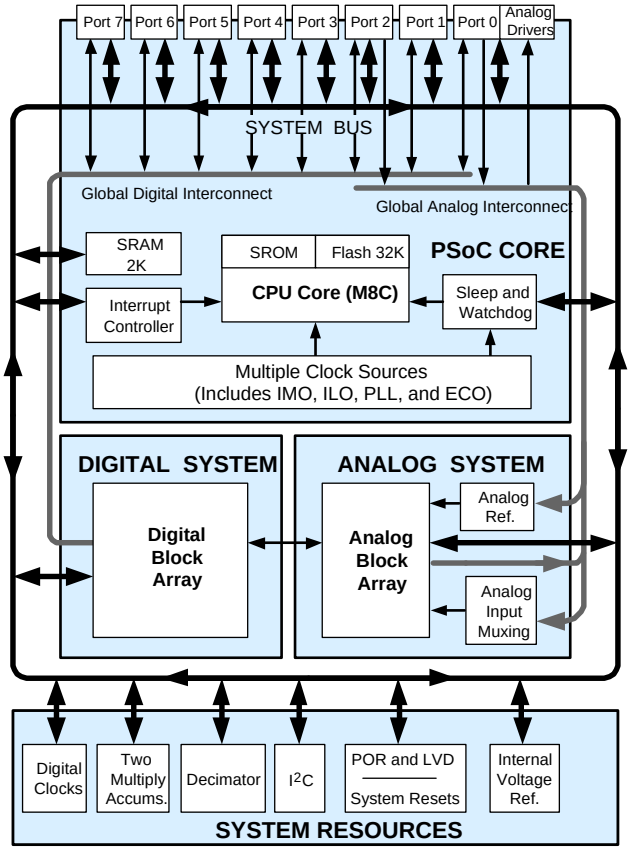
PSoC Core

The CY8CLED16P01 is based on the Cypress PSoC® 1 architecture. The PSoC platform consists of many *Programmable System-on-chip Controller* devices. These devices are designed to replace multiple traditional MCU-based system components with one, low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, and programmable interconnects. This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/Os are included in a range of convenient pinouts and packages.

The PSoC architecture, as shown in Figure 5 on page 10, consists of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global busing enables all the device resources to be combined into a complete custom system. The CY8CLED16P01 family can have up to five I/O ports that connect to the global digital and analog interconnects, providing access to 16 digital blocks and 12 analog blocks.

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose I/O).

Figure 5. PSoC Architecture



The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a 4 MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with 25 vectors, to simplify programming of realtime embedded events. Program execution is timed and protected using the included Sleep and Watchdog timers (WDT).

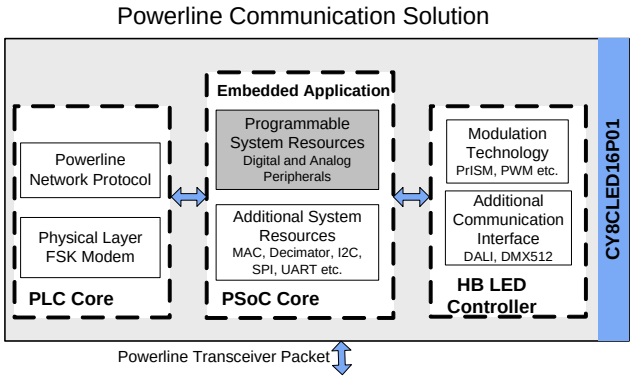
Memory encompasses 32 KB of Flash for program storage, 2 KB of SRAM for data storage, and up to 2 KB of EEPROM emulated using Flash. Program Flash uses four protection levels on blocks of 64 bytes, enabling customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 2.5 percent over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for the digital system use. A low power 32 kHz ILO (internal low speed oscillator) is provided for the sleep timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. When operating the Powerline Transceiver (PLT) user module, the ECO must be selected to ensure accurate protocol timing. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, enabling great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

Programmable System Resources

Figure 6. Programmable System Resources



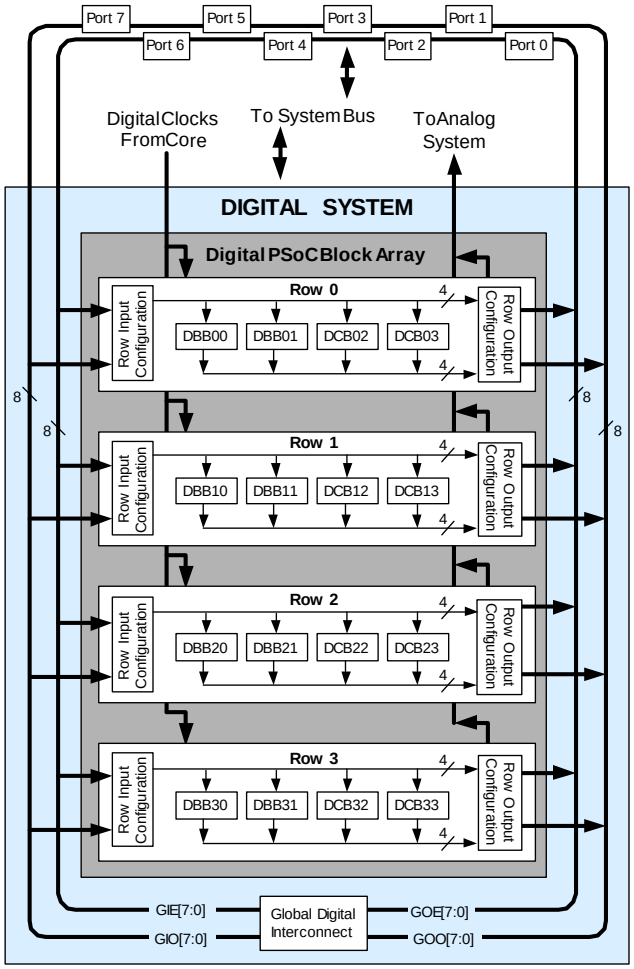
The Digital System

The digital system contains 16 digital PSoC blocks. Each block is an 8-bit resource that can be used alone, or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals called user modules. Digital peripheral configurations include:

- PWMs (8 to 32 bit)
- PWMs with Dead Band (8 to 32 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity (up to four)
- SPI master and slave (up to four each)
- I^2C slave and multi-master (one available as a System Resource)
- Cyclical Redundancy Checker and Generator (8 to 32 bit)
- IrDA (up to 4)
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also enable signal multiplexing and perform logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Figure 7. Digital System Block Diagram



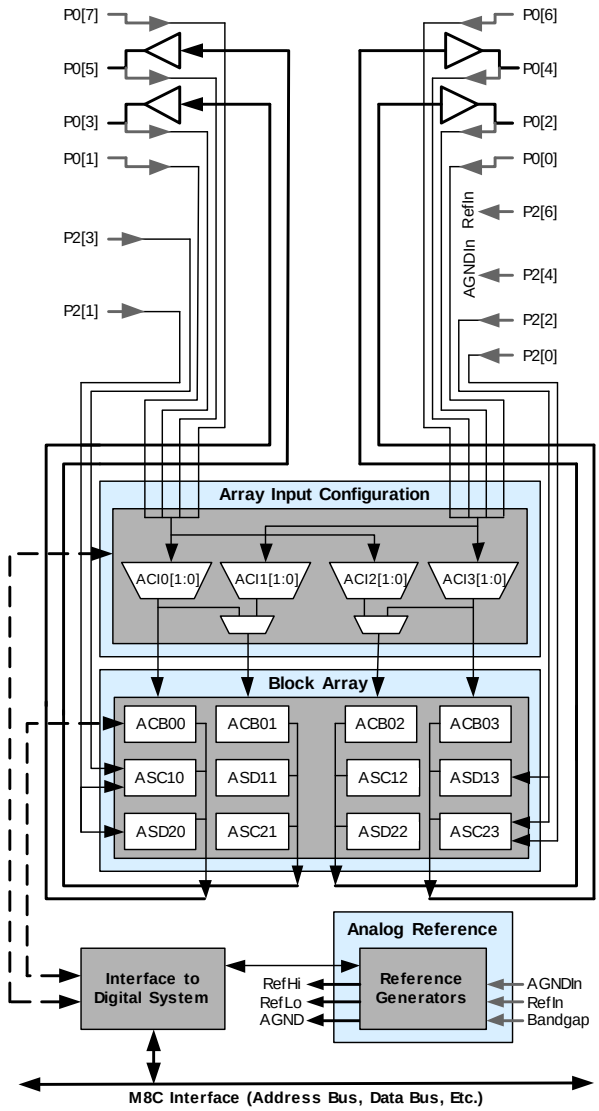
The Analog System

The analog system contains 12 configurable blocks, each containing an opamp circuit, enabling the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (up to 4, with 6- to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (2, 4, 6, or 8 pole band pass, low pass, and notch)
- Amplifiers (up to 4, with selectable gain to 48x)
- Instrumentation amplifiers (up to 2, with selectable gain to 93x)
- Comparators (up to 4, with 16 selectable thresholds)
- DACs (up to 4, with 6- to 9-bit resolution)
- Multiplying DACs (up to 4, with 6- to 9-bit resolution)
- High current output drivers (4 with 40 mA drive as a Core Resource)
- 1.3 V reference (as a System Resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

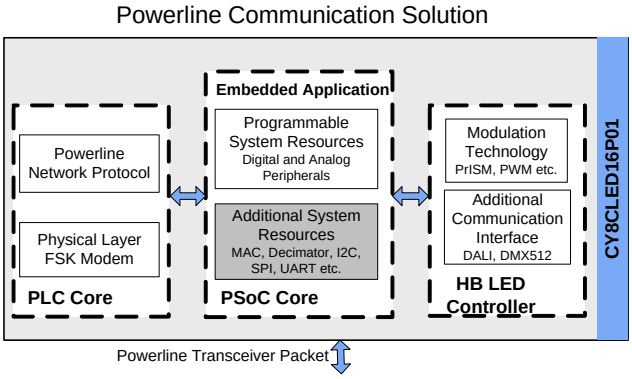
Analog blocks are provided in columns of three, which includes one CT (continuous time) and two SC (switched capacitor) blocks, as shown in the Figure 8.

Figure 8. Analog System Block Diagram



Additional System Resources

Figure 9. Additional System Resources



System Resources, some of which have been previously described, provide additional capability useful to complete systems. Resources include a multiplier, decimator, low voltage detection, and power on reset. The following statements describe the merits of each system resource.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks are generated using digital PSoC blocks as clock dividers.
- Multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in general math and digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- The I^2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are supported.
- Low Voltage Detection (LVD) interrupts signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 V reference provides an absolute reference for the analog system, including ADCs and DACs.

Getting Started

The quickest way to understand Cypress's Powerline Communication offering is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). The latest version of PSoC Designer can be downloaded from http://www.cypress.com. This data sheet is an overview of the CY8CLED16P01 integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the PLC Technical Reference Manual.

For up to date ordering, packaging, and electrical specification information, see the latest PLC device data sheets on the web at http://www.cypress.com.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select user modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called "user modules." User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

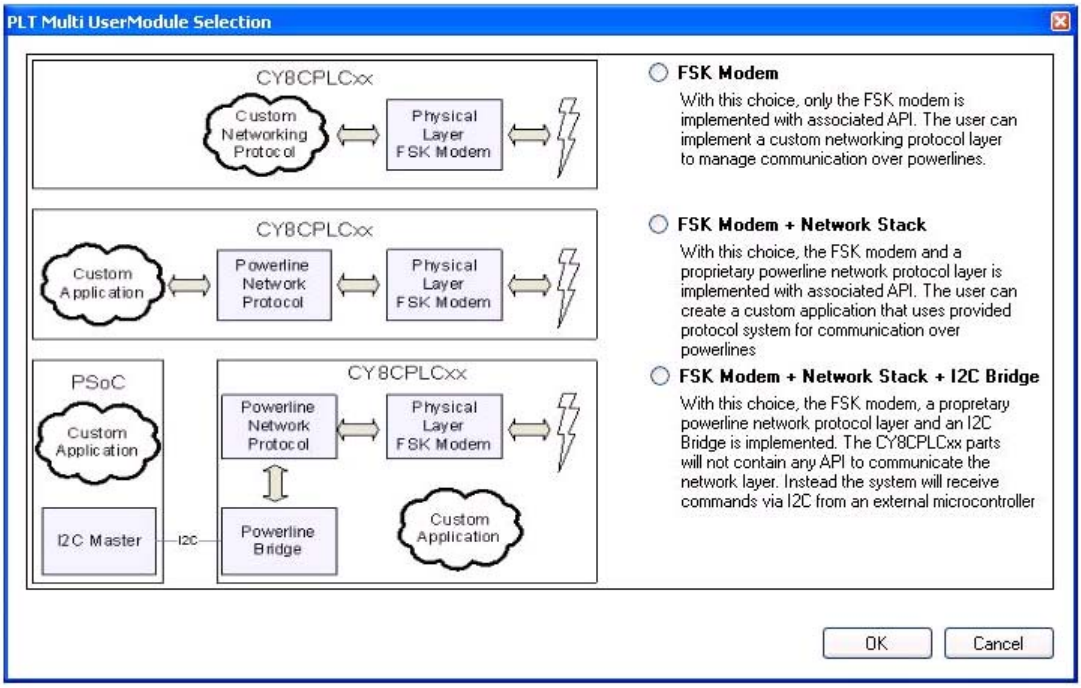
PLC User Modules

Powerline Transceiver (PLT) User Module (UM) enables data communication over powerlines up to baud rates of 2400 bps. This UM also exposes all the APIs from the network protocol for ease of application development. The UM, when instantiated, provides the user with three implementation modes:

- **FSK Modem Only** – This mode enables the user to use the raw FSK modem and build any network protocol or application with the help of the APIs generated by the modem PHY.
- **FSK Modem + Network Stack** – This mode allows the user to use the Cypress network protocol for PLC and build any application with the APIs provided by the network protocol.
- **FSK Modem + Network Stack + I2C** – This mode allows the user to interface the CY8CLEDP01 with any other microcontroller or PSoC device. Users can also split the application between the PLC device and the external microcontroller. If the external microcontroller is a PSoC device, then the I2C UMs can be used to interface it with the PLC device.

Figure 10 on page 15 shows the starting window for the PLT UM with the three implementation modes from which the user can choose.

Figure 10. PLT User Module



Refer to the application note AN55403 - “Estimating CY8CPLC20/CY8CLED16P01 Power Consumption” at http://www.cypress.com to determine the power consumption estimate of the CY8CLED16P01 chip with the PLT User Module, loaded along with the other User Modules.

Intelligent Lighting User Modules

The CY8CLED16P01 has the intelligent lighting control user modules along with the PLC user modules. These user modules enable the user to do the following:

- Control multiple channels, anywhere between 1 and 16.
- Enable temperature compensation and color feedback
- Provide algorithms for high CRI
- Control color with 1931 or 1976 gamuts and through CCT
- Provide additional communication interfaces such as DALI and DMX512

Pin Information

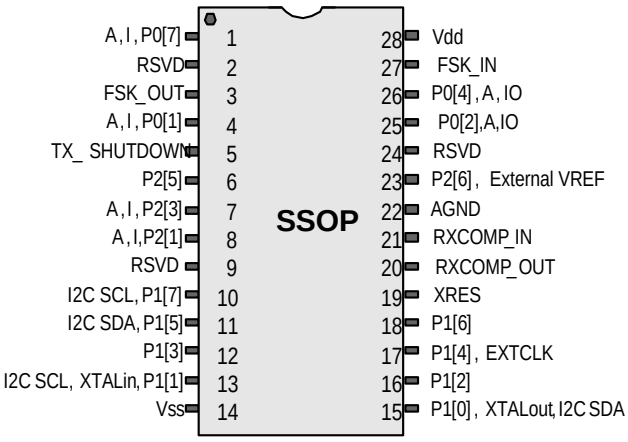
The CY8CLED16P01 PLC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, Vss, Vdd, and XRES are not capable of Digital I/O.

28-pin Part Pinout

Table 5. 28-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog Column Mux Input
2	Reserved		RSVD	Reserved
3		O	FSK_OUT	Analog FSK Output
4	I/O	I	P0[1]	Analog Column Mux Input
5	O		TX_SHUTDOWN	Output to disable PLC transmit circuitry in receive mode Logic ‘0’ - When the Modem is transmitting Logic ‘1’ - When the Modem is not transmitting
6	I/O		P2[5]	
7	I/O	I	P2[3]	Direct switched capacitor block input
8	I/O	I	P2[1]	Direct switched capacitor block input
9	Reserved		RSVD	Reserved
10	I/O		P1[7]	I2C Serial Clock (SCL)
11	I/O		P1[5]	I2C Serial Data (SDA)
12	I/O		P1[3]	XTAL_STABILITY. Connect a 0.1 µF capacitor between the pin and Vss.
13	I/O		P1[1]	Crystal (XTALin)[2], ISSP-SCLK[1], I2C SCL
14	Power		Vss	Ground connection.
15	I/O		P1[0]	Crystal (XTALout)[2], ISSP-SDATA[1], I2C SDA
16	I/O		P1[2]	
17	I/O		P1[4]	Optional External Clock Input (EXTCLK)[2]
18	I/O		P1[6]	
19	Input		XRES	Active high external reset with internal pull down
20		O	RXCOMP_OUT	Analog Output to external Low Pass Filter Circuitry
21		I	RXCOMP_IN	Analog Input from the external Low Pass Filter Circuitry
22	Analog Ground		AGND	Analog Ground. Connect a 1.0 µF capacitor between the pin and Vss.
23	I/O		P2[6]	External Voltage Reference (VREF)
24	Reserved		RSVD	Reserved
25	I/O	I/O	P0[2]	Analog column mux input and column output
26	I/O	I/O	P0[4]	Analog column mux input and column output
27		I	FSK_IN	Analog FSK Input
28	Power		Vdd	Supply Voltage

Figure 11. CY8CLED16P01 28-pin PLC Device



LEGEND: A = Analog, I = Input, O = Output, and RSVD = Reserved (should be left unconnected).

Notes
1. These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Technical Reference Manual* for details.
2. When using the PLT user module, the external crystal is always required for protocol timing. For the FSK modem, either the PLL Mode should be enabled or the external 24 MHz on P1[4] should be selected. The IMO should not be used.

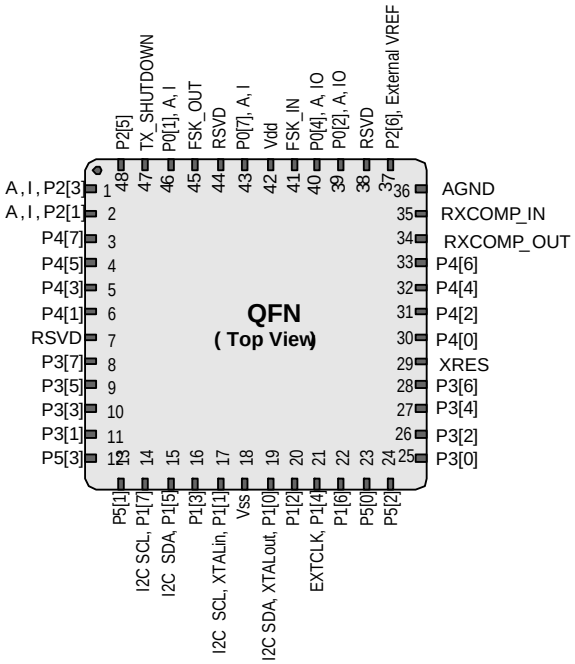
48-pin Part Pinout

Table 6. 48-pin Part Pinout (QFN) [3]

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P2[3]	Direct switched capacitor block input
2	I/O	I	P2[1]	Direct switched capacitor block input
3	I/O		P4[7]	
4	I/O		P4[5]	
5	I/O		P4[3]	
6	I/O		P4[1]	
7	Reserved		RSVD	Reserved
8	I/O		P3[7]	
9	I/O		P3[5]	
10	I/O		P3[3]	
11	I/O		P3[1]	
12	I/O		P5[3]	
13	I/O		P5[1]	
14	I/O		P1[7]	I2C Serial Clock (SCL)
15	I/O		P1[5]	I2C Serial Data (SDA)
16	I/O		P1[3]	XTAL_STABILITY. Connect a 1.0 µF capacitor between the pin and Vss.
17	I/O		P1[1]	Crystal (XTALin)[2], I2C Serial Clock (SCL), ISSP-SCLK[1]
18	Power		Vss	Ground connection.
19	I/O		P1[0]	Crystal (XTALout)[2], I2C Serial Data (SDA), ISSP-SDATA[1]
20	I/O		P1[2]	
21	I/O		P1[4]	Optional External Clock Input (EXTCLK)[2]
22	I/O		P1[6]	
23	I/O		P5[0]	
24	I/O		P5[2]	
25	I/O		P3[0]	
26	I/O		P3[2]	
27	I/O		P3[4]	
28	I/O		P3[6]	
29	Input		XRES	Active high external reset with internal pull down
30	I/O		P4[0]	
31	I/O		P4[2]	
32	I/O		P4[4]	
33	I/O		P4[6]	
34		O	RXCOMP_OUT	Analog Output to external Low Pass Filter Circuitry
35		I	RXCOMP_IN	Analog Input from external Low Pass Filter Circuitry
36	Analog Ground		AGND	Analog Ground. Connect a 1.0 µF capacitor between the pin and Vss.
37	I/O		P2[6]	External Voltage Reference (VREF)
38	Reserved		RSVD	Reserved
39	I/O	I/O	P0[2]	Analog column mux input and column output
40	I/O	I/O	P0[4]	Analog column mux input and column output
41		I	FSK_IN	Analog FSK Input
42	Power		Vdd	Supply Voltage
43	I/O	I	P0[7]	Analog column mux input
44	Reserved		RSVD	Reserved
45		O	FSK_OUT]	Analog FSK Output
46	I/O	I	P0[1]	Analog column mux input
47	O		TX_SHUTDOWN	Output to disable transmit circuitry in receive mode Logic ‘0’ - When the Modem is transmitting Logic ‘1’ - When the Modem is not transmitting
48	I/O		P2[5]	

LEGEND: A = Analog, I = Input, O = Output, and RSVD = Reserved (should be left unconnected).

Figure 12. CY8CLED16P01 48-pin PLC Device



Note
3. The QFN package has a center pad that must be connected to ground (Vss).

100-pin Part Pinout (On-Chip Debug)

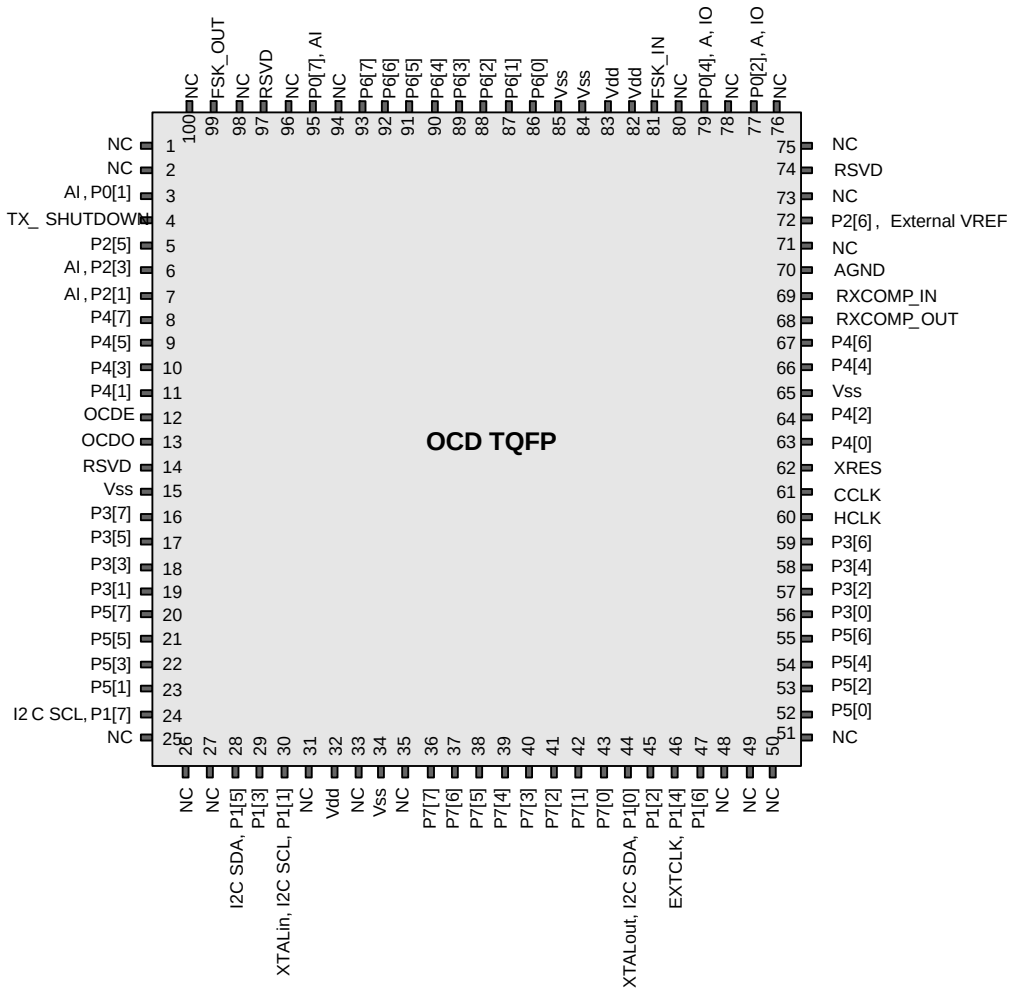
The 100-pin TQFP part is for the CY8CLED16P01-OCD On-Chip Debug PLC device. Note that the OCD parts are only used for in-circuit debugging. OCD parts are not available for production.

Table 7. 100-pin OCD Part Pinout (TQFP)

Pin No.	Digital	Analog	Name	Description	Pin No.	Digital	Analog	Name	Description
1			NC	No Connection	51			NC	No Connection
2			NC	No Connection	52	I/O		P5[0]	
3	I/O	I	P0[1]	Analog Column Mux Input	53	I/O		P5[2]	
4	O		TX_SHUTDOWN	Output to disable transmit circuitry in receive mode Logic '0' - When the Modem is transmitting Logic '1' - When the Modem is not transmitting	54	I/O		P5[4]	
5	I/O		P2[5]		55	I/O		P5[6]	
6	I/O	I	P2[3]	Direct switched capacitor block input	56	I/O		P3[0]	
7	I/O	I	P2[1]	Direct switched capacitor block input	57	I/O		P3[2]	
8	I/O		P4[7]		58	I/O		P3[4]	
9	I/O		P4[5]		59	I/O		P3[6]	
10	I/O		P4[3]		60			HCLK	OCD high speed clock output
11	I/O		P4[1]		61			CCLK	OCD CPU clock output
12			OCDE	OCD even data I/O	62	Input		XRES	Active high pin reset with internal pull down
13			OCDO	OCD odd data output	63	I/O		P4[0]	
14	Reserved		RSVD	Reserved	64	I/O		P4[2]	
15	Power		Vss	Ground Connection	65	Power		Vss	Ground Connection
16	I/O		P3[7]		66	I/O		P4[4]	
17	I/O		P3[5]		67	I/O		P4[6]	
18	I/O		P3[3]		68		O	RXCOMP_OUT	Analog Output to external Low Pass Filter Circuitry
19	I/O		P3[1]		69		I	RXCOMP_IN	Analog Input from external Low Pass Filter Circuitry
20	I/O		P5[7]		70	Ground		AGND	Analog Ground. Connect a 1.0 µF capacitor between the pin and Vss.
21	I/O		P5[5]		71			NC	No Connection
22	I/O		P5[3]		72	I/O		P2[6]	External Voltage Reference (VREF) input
23	I/O		P5[1]		73			NC	No Connection
24	I/O		P1[7]	I2C Serial Clock (SCL)	74	Reserved		RSVD	Reserved
25			NC	No Connection	75			NC	No Connection
26			NC	No Connection	76			NC	No Connection
27			NC	No Connection	77	I/O	I/O	P0[2]	Analog column mux input and column output
28	I/O		P1[5]	I2C Serial Data (SDA)	78			NC	No Connection
29	I/O		P1[3]	XTAL_STABILITY. Connect a 0.1 µF capacitor between the pin and VSS.	79	I/O	I/O	P0[4]	Analog column mux input and column output, VREF
30	I/O		P1[1]	Crystal (XTALin)[2], I2C Serial Clock (SCL), TC SCLK	80			NC	No Connection
31			NC	No Connection	81		I	FSK_IN	Analog FSK Input
32	Power		Vdd	Supply Voltage	82	Power		Vdd	Supply Voltage
33			NC	No Connection	83	Power		Vdd	Supply Voltage
34	Power		Vss	Ground Connection	84	Power		Vss	Ground Connection
35			NC	No Connection	85	Power		Vss	Ground Connection
36	I/O		P7[7]		86	I/O		P6[0]	
37	I/O		P7[6]		87	I/O		P6[1]	
38	I/O		P7[5]		88	I/O		P6[2]	
39	I/O		P7[4]		89	I/O		P6[3]	
40	I/O		P7[3]		90	I/O		P6[4]	
41	I/O		P7[2]		91	I/O		P6[5]	
42	I/O		P7[1]		92	I/O		P6[6]	
43	I/O		P7[0]		93	I/O		P6[7]	
44	I/O		P1[0]	Crystal (XTALout)[2], I2C Serial Data (SDA), TC SDATA	94			NC	No Connection
45	I/O		P1[2]		95	I/O	I	P0[7]	Analog Column Mux Input
46	I/O		P1[4]	Optional External Clock Input (EXTCLK)[2]	96			NC	No Connection
47	I/O		P1[6]		97	Reserved		RSVD	Reserved
48			NC	No Connection	98			NC	No Connection
49			NC	No Connection	99		O	FSK_OUT	Analog FSK Output
50			NC	No Connection	100			NC	No Connection

LEGEND A = Analog, I = Input, O = Output, NC = No Connection, TC/TM: Test, TC/TM: Test, RSVD = Reserved (should be left unconnected).

Figure 13. CY8CLED16P01-OCD



Not for Production

Register Reference

This section lists the registers of the CY8CLED16P01 PLC device. For detailed register information, refer to the *PLC Technical Reference Manual*.

Register Conventions

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The CY8CLEDP01 device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are reserved and should not be accessed.

Table 8. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBB20DR0	40	#	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0IE	01	RW	DBB20DR1	41	W	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0GS	02	RW	DBB20DR2	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0DM2	03	RW	DBB20CR0	43	#	ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DR	04	RW	DBB21DR0	44	#	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1IE	05	RW	DBB21DR1	45	W	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1GS	06	RW	DBB21DR2	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1DM2	07	RW	DBB21CR0	47	#	ASD11CR3	87	RW		C7	
PRT2DR	08	RW	DCB22DR0	48	#	ASC12CR0	88	RW	RDI3RI	C8	RW
PRT2IE	09	RW	DCB22DR1	49	W	ASC12CR1	89	RW	RDI3SYN	C9	RW
PRT2GS	0A	RW	DCB22DR2	4A	RW	ASC12CR2	8A	RW	RDI3IS	CA	RW
PRT2DM2	0B	RW	DCB22CR0	4B	#	ASC12CR3	8B	RW	RDI3LT0	CB	RW
PRT3DR	0C	RW	DCB23DR0	4C	#	ASD13CR0	8C	RW	RDI3LT1	CC	RW
PRT3IE	0D	RW	DCB23DR1	4D	W	ASD13CR1	8D	RW	RDI3RO0	CD	RW
PRT3GS	0E	RW	DCB23DR2	4E	RW	ASD13CR2	8E	RW	RDI3RO1	CE	RW
PRT3DM2	0F	RW	DCB23CR0	4F	#	ASD13CR3	8F	RW		CF	
PRT4DR	10	RW	DBB30DR0	50	#	ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW	DBB30DR1	51	W	ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW	DBB30DR2	52	RW	ASD20CR2	92	RW		D2	
PRT4DM2	13	RW	DBB30CR0	53	#	ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW	DBB31DR0	54	#	ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW	DBB31DR1	55	W	ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW	DBB31DR2	56	RW	ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW	DBB31CR0	57	#	ASC21CR3	97	RW	I2C_SCR	D7	#
PRT6DR	18	RW	DCB32DR0	58	#	ASD22CR0	98	RW	I2C_DR	D8	RW
PRT6IE	19	RW	DCB32DR1	59	W	ASD22CR1	99	RW	I2C_MSCR	D9	#
PRT6GS	1A	RW	DCB32DR2	5A	RW	ASD22CR2	9A	RW	INT_CLR0	DA	RW
PRT6DM2	1B	RW	DCB32CR0	5B	#	ASD22CR3	9B	RW	INT_CLR1	DB	RW
PRT7DR	1C	RW	DCB33DR0	5C	#	ASC23CR0	9C	RW	INT_CLR2	DC	RW
PRT7IE	1D	RW	DCB33DR1	5D	W	ASC23CR1	9D	RW	INT_CLR3	DD	RW
PRT7GS	1E	RW	DCB33DR2	5E	RW	ASC23CR2	9E	RW	INT_MSK3	DE	RW
PRT7DM2	1F	RW	DCB33CR0	5F	#	ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCB02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCB02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBB10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBB10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBB11CR0	37	#	ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCB12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCB13CR0	3F	#	ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Table 0-1. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBB20FN	40	RW	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0DM1	01	RW	DBB20IN	41	RW	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBB20OU	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW		43		ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBB21FN	44	RW	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1DM1	05	RW	DBB21IN	45	RW	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBB21OU	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW	DCB22FN	48	RW	ASC12CR0	88	RW	RDI3RI	C8	RW
PRT2DM1	09	RW	DCB22IN	49	RW	ASC12CR1	89	RW	RDI3SYN	C9	RW
PRT2IC0	0A	RW	DCB22OU	4A	RW	ASC12CR2	8A	RW	RDI3IS	CA	RW
PRT2IC1	0B	RW		4B		ASC12CR3	8B	RW	RDI3LT0	CB	RW
PRT3DM0	0C	RW	DCB23FN	4C	RW	ASD13CR0	8C	RW	RDI3LT1	CC	RW
PRT3DM1	0D	RW	DCB23IN	4D	RW	ASD13CR1	8D	RW	RDI3RO0	CD	RW
PRT3IC0	0E	RW	DCB23OU	4E	RW	ASD13CR2	8E	RW	RDI3RO1	CE	RW
PRT3IC1	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DM0	10	RW	DBB30FN	50	RW	ASD20CR0	90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW	DBB30IN	51	RW	ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW	DBB30OU	52	RW	ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW	DBB31FN	54	RW	ASC21CR0	94	RW		D4	
PRT5DM1	15	RW	DBB31IN	55	RW	ASC21CR1	95	RW		D5	
PRT5IC0	16	RW	DBB31OU	56	RW	ASC21CR2	96	RW		D6	
PRT5IC1	17	RW		57		ASC21CR3	97	RW		D7	
PRT6DM0	18	RW	DCB32FN	58	RW	ASD22CR0	98	RW		D8	
PRT6DM1	19	RW	DCB32IN	59	RW	ASD22CR1	99	RW		D9	
PRT6IC0	1A	RW	DCB32OU	5A	RW	ASD22CR2	9A	RW		DA	
PRT6IC1	1B	RW		5B		ASD22CR3	9B	RW		DB	
PRT7DM0	1C	RW	DCB33FN	5C	RW	ASC23CR0	9C	RW		DC	
PRT7DM1	1D	RW	DCB33IN	5D	RW	ASC23CR1	9D	RW	OSC_GO_EN	DD	RW
PRT7IC0	1E	RW	DCB33OU	5E	RW	ASC23CR2	9E	RW	OSC_CR4	DE	RW
PRT7IC1	1F	RW		5F		ASC23CR3	9F	RW	OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7		DEC_CR2	E7	RW
DCB02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	W
DCB02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
DBB10FN	30	RW	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10IN	31	RW	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10OU	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11FN	34	RW	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11IN	35	RW	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11OU	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12FN	38	RW	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12IN	39	RW	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12OU	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
	3B		ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13FN	3C	RW	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13IN	3D	RW	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13OU	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
	3F		ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLED16P01 device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 9. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 65 °C degrade reliability.
$T_{BAKETEMP}$	Bake Temperature	–	125	See package label	°C	
$T_{BAKETIME}$	Bake Time	See package label	–	72	Hours	
T_A	Ambient Temperature with Power Applied	–40	–	+85	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	–0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss – 0.5	–	Vdd + 0.5	V	
V_{IOZ}	DC Voltage Applied to Tristate	Vss – 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	–25	–	+50	mA	
I_{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	-50	–	+50	mA	
ESD	Electrostatic Discharge Voltage	2000	–	–	V	Human Body Model ESD
LU	Latch-up Current	–	–	200	mA	

Operating Temperature

Table 10. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	°C	
T_J	Junction Temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 43.The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 11. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	4.75	–	5.25	V	
I_{DD}	Supply Current	–	8	14	mA	Conditions are 5.0 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz.
V_{REF}	Reference Voltage (Bandgap)	1.28	1.3	1.32	V	Trimmed for appropriate Vdd.

DC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature range: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 12. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull Up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull Down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd – 1.0	–	–	V	I_{OH} = 10 mA, (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I_{OH} budget.
V_{OL}	Low Output Level	–	–	0.75	V	I_{OL} = 25 mA, (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I_{OL} budget.
I_{OH}	High Level Source Current	10	–	–	mA	V_{OH} = Vdd – 1.0 V. See the limitations of the total current in the Note for V_{OH}.
I_{OL}	Low Level Sink Current	25	–	–	mA	V_{OL} = 0.75 V. See the limitations of the total current in the Note for V_{OL}.
V_{IL}	Input Low Level	–	–	0.8	V	
V_{IH}	Input High Level	2.1	–		V	
V_H	Input Hysteresis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.

DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 13. 5-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = Low, Opamp bias = Low Power = Low, Opamp bias = High Power = Medium, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = Low Power = High, Opamp bias = High	 – – – – – –	 1.6 1.6 1.6 1.6 1.6 1.6	 10 10 10 10 10 10	 mV mV mV mV mV mV	
TCV_{OSOA}	Average input offset voltage drift	–	4	23	µV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	200	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range (All cases, except Power = High, Opamp bias = High) Common mode voltage range (Power = High, Opamp bias = High)	0 0.5	– –	V_{DD} V_{DD} – 0.5	V V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
CMRROA	Common mode rejection ratio	60	–	–	dB	
GOLOA	Open loop gain	80	–	–	dB	
$V_{OHIGHOA}$	High output voltage swing (internal signals)	V_{DD} – 0.01	–	–	V	
V_{OLOWOA}	Low output voltage swing (internal signals)	–	–	0.1	V	
I_{SOA}	Supply current (including associated AGND buffer) Power = Low, Opamp bias = Low Power = Low, Opamp bias = High Power = Medium, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = Low Power = High, Opamp bias = High	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply voltage rejection ratio	67	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$.

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 14. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low Power Comparator (LPC) Reference Voltage Range	0.2	–	Vdd – 1	V	
I_{SLPC}	LPC Supply Current	–	10	40	µA	
V_{OSLPC}	LPC Voltage Offset	–	2.5	30	mV	

DC Analog Output Buffer Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 15. DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit driven by the analog output buffer.
V_{OSOB}	Input Offset Voltage (Absolute Value) Power = Low, Opamp bias = Low Power = Low, Opamp bias = High Power = High, Opamp bias = Low Power = High, Opamp bias = High	 – – – –	 3.2 3.2 3.2 3.2	 18 18 18 18	 mV mV mV mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	5.5	26	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	Vdd – 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 – –	 1 1	 W W	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 0.5 × Vdd + 1.3 0.5 × Vdd + 1.3	 – –	 – –	 V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 × Vdd – 1.3 0.5 × Vdd – 1.3	 V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 2 5	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	40	64	–	dB	

DC Analog Reference Specifications

Table 16 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Table 16. 5-V DC Analog Reference Specifications

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b000	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.228	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.352	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.078	$V_{DD}/2$ – 0.007	$V_{DD}/2$ + 0.063	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.336	$V_{DD}/2$ – 1.295	$V_{DD}/2$ – 1.250	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.224	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.356	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.056	$V_{DD}/2$ – 0.005	$V_{DD}/2$ + 0.043	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.338	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.255	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.356	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.057	$V_{DD}/2$ – 0.006	$V_{DD}/2$ + 0.044	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.337	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.256	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.294	$V_{DD}/2$ + 1.359	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.047	$V_{DD}/2$ – 0.004	$V_{DD}/2$ + 0.035	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.338	$V_{DD}/2$ – 1.299	$V_{DD}/2$ – 1.258	V

Table 16. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b001	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	P2[4] + P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.085	P2[4] + P2[6] – 0.016	P2[4] + P2[6] + 0.044	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.022	P2[4] – P2[6] + 0.010	P2[4] – P2[6] + 0.055	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.077	P2[4] + P2[6] – 0.010	P2[4] + P2[6] + 0.051	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.022	P2[4] – P2[6] + 0.005	P2[4] – P2[6] + 0.039	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	P2[4] + P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.070	P2[4] + P2[6] – 0.010	P2[4] + P2[6] + 0.050	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.022	P2[4] – P2[6] + 0.005	P2[4] – P2[6] + 0.039	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.070	P2[4] + P2[6] – 0.007	P2[4] + P2[6] + 0.054	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.022	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.032	V
0b010	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.037	V_{DD} – 0.009	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.061	$V_{DD}/2$ – 0.006	$V_{DD}/2$ + 0.047	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.007	V_{SS} + 0.028	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.039	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.049	$V_{DD}/2$ – 0.005	$V_{DD}/2$ + 0.036	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.019	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.037	V_{DD} – 0.007	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.054	$V_{DD}/2$ – 0.005	$V_{DD}/2$ + 0.041	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.024	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.042	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.046	$V_{DD}/2$ – 0.004	$V_{DD}/2$ + 0.034	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.017	V

Table 16. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b011	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	3 × Bandgap	3.788	3.891	3.986	V
		V_{AGND}	AGND	2 × Bandgap	2.500	2.604	3.699	V
		V_{REFLO}	Ref Low	Bandgap	1.257	1.306	1.359	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	3 × Bandgap	3.792	3.893	3.982	V
		V_{AGND}	AGND	2 × Bandgap	2.518	2.602	2.692	V
		V_{REFLO}	Ref Low	Bandgap	1.256	1.302	1.354	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	3 × Bandgap	3.795	3.894	3.993	V
		V_{AGND}	AGND	2 × Bandgap	2.516	2.603	2.698	V
		V_{REFLO}	Ref Low	Bandgap	1.256	1.303	1.353	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	3 × Bandgap	3.792	3.895	3.986	V
		V_{AGND}	AGND	2 × Bandgap	2.522	2.602	2.685	V
		V_{REFLO}	Ref Low	Bandgap	1.255	1.301	1.350	V
0b100	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.495 – P2[6]	2.586 – P2[6]	2.657 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.502	2.604	2.719	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.531 – P2[6]	2.611 – P2[6]	2.681 – P2[6]	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.500 – P2[6]	2.591 – P2[6]	2.662 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.519	2.602	2.693	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.530 – P2[6]	2.605 – P2[6]	2.666 – P2[6]	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.503 – P2[6]	2.592 – P2[6]	2.662 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.517	2.603	2.698	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.529 – P2[6]	2.606 – P2[6]	2.665 – P2[6]	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.505 – P2[6]	2.594 – P2[6]	2.665 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.525	2.602	2.685	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.528 – P2[6]	2.603 – P2[6]	2.661 – P2[6]	V

Table 16. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b101	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.222	P2[4] + 1.290	P2[4] + 1.343	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.331	P2[4] – 1.295	P2[4] – 1.254	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.226	P2[4] + 1.293	P2[4] + 1.347	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.331	P2[4] – 1.298	P2[4] – 1.259	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.227	P2[4] + 1.294	P2[4] + 1.347	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.331	P2[4] – 1.298	P2[4] – 1.259	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.228	P2[4] + 1.295	P2[4] + 1.349	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.332	P2[4] – 1.299	P2[4] – 1.260	V
0b110	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	2 × Bandgap	2.535	2.598	2.644	V
		V_{AGND}	AGND	Bandgap	1.227	1.305	1.398	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.009	V_{SS} + 0.038	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	2 × Bandgap	2.530	2.598	2.643	V
		V_{AGND}	AGND	Bandgap	1.244	1.303	1.370	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.024	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	2 × Bandgap	2.532	2.598	2.644	V
		V_{AGND}	AGND	Bandgap	1.239	1.304	1.380	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.026	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	2 × Bandgap	2.528	2.598	2.645	V
		V_{AGND}	AGND	Bandgap	1.249	1.302	1.362	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.018	V
0b111	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	3.2 × Bandgap	4.041	4.155	4.234	V
		V_{AGND}	AGND	1.6 × Bandgap	1.998	2.083	2.183	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.010	V_{SS} + 0.038	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	3.2 × Bandgap	4.047	4.153	4.236	V
		V_{AGND}	AGND	1.6 × Bandgap	2.012	2.082	2.157	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.024	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	3.2 × Bandgap	4.049	4.154	4.238	V
		V_{AGND}	AGND	1.6 × Bandgap	2.008	2.083	2.165	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.026	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	3.2 × Bandgap	4.047	4.154	4.238	V
		V_{AGND}	AGND	1.6 × Bandgap	2.016	2.081	2.150	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.018	V

DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 17. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ	
C_{SC}	Capacitor Unit Value (Switch Cap)	–	80	–	fF	

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C = TA = 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 18. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
VPPOR2R	Vdd Value for PPOR Trip (positive ramp) PORLEV[1:0] = 10b	–	4.55	–	V	
VPPOR2	Vdd Value for PPOR Trip (negative ramp) PORLEV[1:0] = 10b	–	4.55	–	V	
VPH2	PPOR Hysteresis PORLEV[1:0] = 10b	–	0	–	mV	
VLVD6 VLVD7	Vdd Value for LVD Trip VM[2:0] = 110b VM[2:0] = 111b	4.63 4.72	4.73 4.81	4.82 4.91	V V	

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 19. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools.
V_{DDLV}	Low V_{DD} for verify	4.7	4.8	4.9	V	This specification applies to the functional requirements of external programmer tools.
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools.
$V_{DDIWRITE}$	Supply voltage for flash write operation	4.75	5,0	5.25	V	This specification applies to this device when it is executing internal flash writes.
I_{DDP}	Supply Current During Programming or Verify	–	10	30	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying V_{ILP} to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor
I_{IHP}	Input Current when Applying V_{IHP} to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block
$Flash_{ENT}$	Flash Endurance (total)[5]	1,800,000	–	–	–	Erase/write cycles
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

DC I^2C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 20. DC I^2C Specifications

Parameter	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}[4]	Input low level	–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}[4]	Input high level	0.7 × V_{DD}	–	–	V	4.75 V ≤ V_{DD} ≤ 5.25 V

Note
4. All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO specifications sections.The I^2C GPIO pins also meet the mentioned specs.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Note See the individual user module data sheets for information on maximum frequencies for user modules.

Table 21. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	Internal Main Oscillator Frequency for 24 MHz	23.4	24	24.6	MHz	Trimmed for 5 V operation using factory trim values. SLIMO Mode = 0.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.5	6	6.5[6]	MHz	Trimmed for 5 V operation using factory trim values. SLIMO Mode = 1.
F_{CPU1}	CPU Frequency (5V Nominal)	0.0914	24	24.6[6]	MHz	SLIMO Mode = 0.
F_{48M}	Digital PSoC Block Frequency	0	48	49.2[6, 7]	MHz	Refer to the AC Digital Block Specifications below.
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{32K_U}	Internal Low Speed Oscillator (ILO) Untrimmed Frequency	5	–	100	kHz	After a reset and before the m8c starts to run, the ILO is not trimmed. See the System Resets section of the *PSoC Technical Reference Manual* for details on timing this.
F_{PLL}	PLL Frequency	–	23.986	–	MHz	A multiple (x732) of crystal frequency.
$T_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	
$T_{PLLSLEWLOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T_{OS}	External Crystal Oscillator Startup to 1%	–	250	500	ms	
T_{OSACC}	External Crystal Oscillator Startup to 100 ppm	–	300	600	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{OSACC} period. Correct operation assumes a properly loaded 1 µW maximum drive level 32.768 kHz crystal. –40 °C ≤ T_A ≤ 85 °C.
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
SR_{POWER_UP}	Power Supply Slew Rate	–	–	250	V/ms	Vdd slew rate during power up.
$T_{POWERUP}$	Time from End of POR to CPU Executing Code	–	16	100	ms	Power up from 0 V. See the System Resets section of the *PSoC Technical Reference Manual*.
DC24M	24 MHz Duty Cycle	40	50	60	%	

Notes

5. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles). For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.
6. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
7. See the individual user module data sheets for information on maximum frequencies for user modules.
8. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

Table 21. AC Chip-Level Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
DC_{ILO}	Internal Low Speed Oscillator Duty Cycle	20	50	80	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2	MHz	Trimmed using factory trim values.
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
t_{jit_IMO} [8]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	700	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	900	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	100	400	ps	
t_{jit_PLL} [8]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	800	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	1200	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	100	700	ps	

Figure 14. PLL Lock Timing Diagram

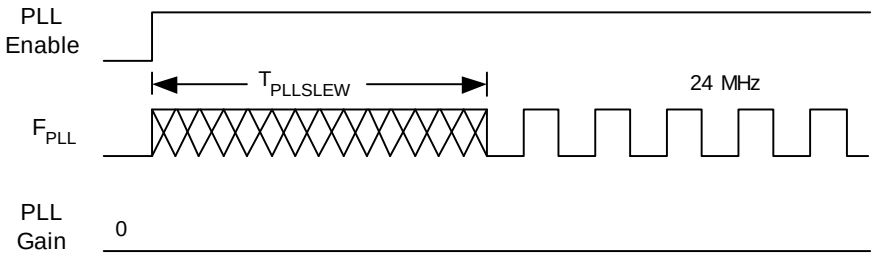


Figure 15. PLL Lock for Low Gain Setting Timing Diagram

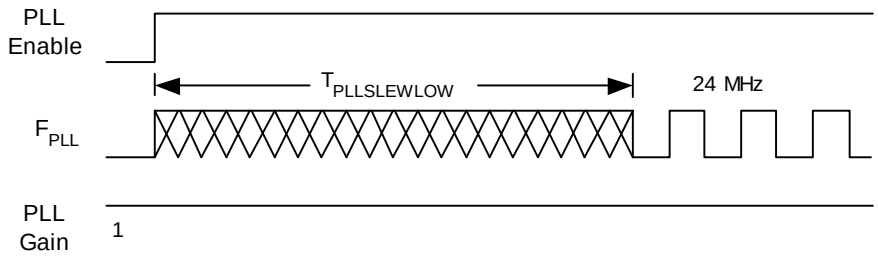
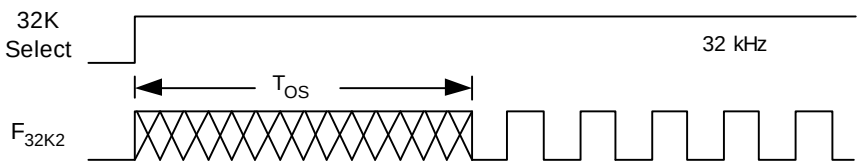


Figure 16. External Crystal Oscillator Startup Timing Diagram



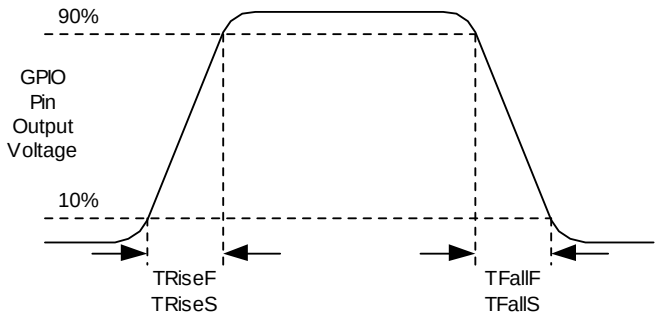
AC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 22. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12.3	MHz	Normal Strong Mode
T_{RiseF}	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	10% – 90%
T_{FallF}	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	10% – 90%
T_{RiseS}	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	10% – 90%
T_{FallS}	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	10% – 90%

Figure 17. GPIO Timing Diagram



AC Operational Amplifier Specifications

Table 23 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Table 23. 5V AC Operational Amplifier Specifications

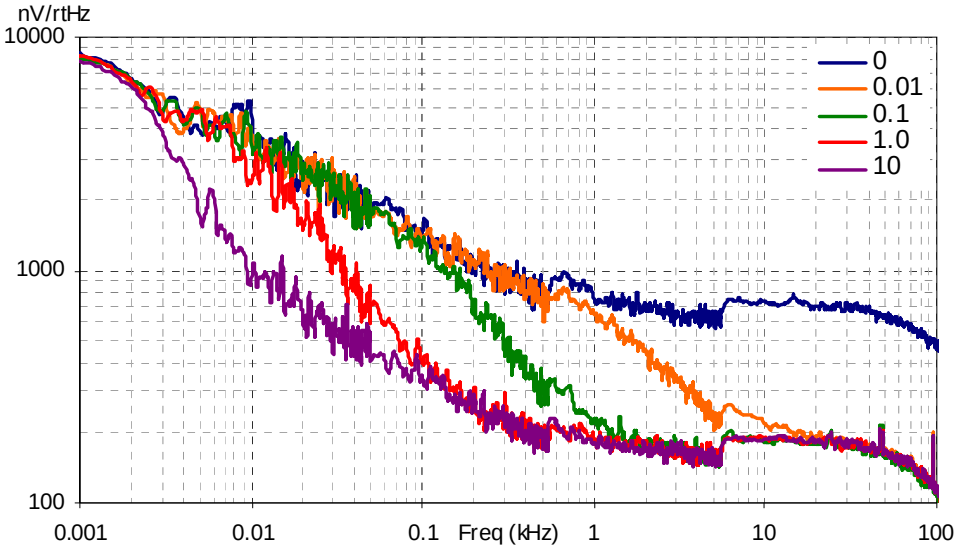
Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time to 0.1% for a 1 V Step (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	–	–	3.9	µs	
	Power = Medium, Opamp Bias = High	–	–	0.72	µs	
	Power = High, Opamp Bias = High	–	–	0.62	µs	
T_{SOA}	Falling Settling Time to 0.1% for a 1 V Step (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	–	–	5.9	µs	
	Power = Medium, Opamp Bias = High	–	–	0.92	µs	
	Power = High, Opamp Bias = High	–	–	0.72	µs	
SR_{ROA}	Rising Slew Rate (20% to 80%) of a 1 V Step (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.15	–	–	V/µs	
	Power = Medium, Opamp Bias = High	1.7	–	–	V/µs	
	Power = High, Opamp Bias = High	6.5	–	–	V/µs	
SR_{FOA}	Falling Slew Rate (20% to 80%) of a 1 V Step (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.01	–	–	V/µs	
	Power = Medium, Opamp Bias = High	0.5	–	–	V/µs	
	Power = High, Opamp Bias = High	4.0	–	–	V/µs	

Table 23. 5V AC Operational Amplifier Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz	
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz	

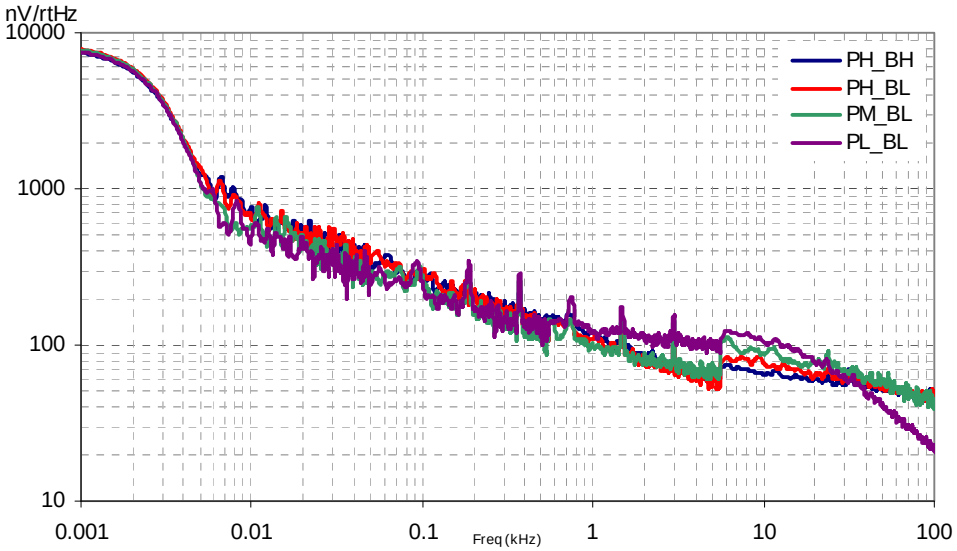
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 18. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 19. Typical Opamp Noise



AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 24. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 25. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All functions	Block input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
Timer	Input clock frequency					
	No capture, V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	With capture	–	–	24.6	MHz	
	Capture pulse width	50[9]	–	–	ns	
Counter	Input clock frequency					
	No enable input, V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	With enable input	–	–	24.6	MHz	
	Enable input pulse width	50[9]	–	–	ns	
Dead Band	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50[9]	–	–	ns	
	Disable mode	50[9]	–	–	ns	
	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
CRCPRS (PRS Mode)	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	24.6	MHz	
SPIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode
	Width of SS_negated between transmissions	50[9]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	49.2	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	24.6	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	49.2	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	24.6	MHz	

Note
9. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

AC Analog Output Buffer Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 26. 5V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1 V Step, 100 pF Load Power = Low Power = High	 – –	 – –	 4 4	 µs µs	
T_{SOB}	Falling Settling Time to 0.1%, 1 V Step, 100 pF Load Power = Low Power = High	 – –	 – –	 3.4 3.4	 µs µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1 V Step, 100 pF Load Power = Low Power = High	 0.5 0.5	 – –	 – –	 V/µs V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1 V Step, 100 pF Load Power = Low Power = High	 0.55 0.55	 – –	 – –	 V/µs V/µs	
BW_{OB}	Small Signal Bandwidth, 20mV_{pp}, 3 dB BW, 100 pF Load Power = Low Power = High	 0.8 0.8	 – –	 – –	 MHz MHz	
BW_{OB}	Large Signal Bandwidth, 1V_{pp}, 3 dB BW, 100 pF Load Power = Low Power = High	 300 300	 – –	 – –	 kHz kHz	

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 27. 5V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High Period	20.6	–	5300	ns	
–	Low Period	20.6	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 28. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Setup Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
T_{WRITE}	Flash Block Write Time	–	40	–	ms	

Table 28. AC Programming Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	
$T_{ERASEALL}$	Flash Erase Time (Bulk)	–	80	–	ms	Erase all Blocks and protection fields at once
$T_{PROGRAM\_HOT}$	Flash Block Erase + Flash Block Write Time	–	–	100[10]	ms	0 °C ≤ Tj ≤ 100 °C
$T_{PROGRAM\_COLD}$	Flash Block Erase + Flash Block Write Time	–	–	200[10]	ms	–40 °C ≤ Tj ≤ 0 °C

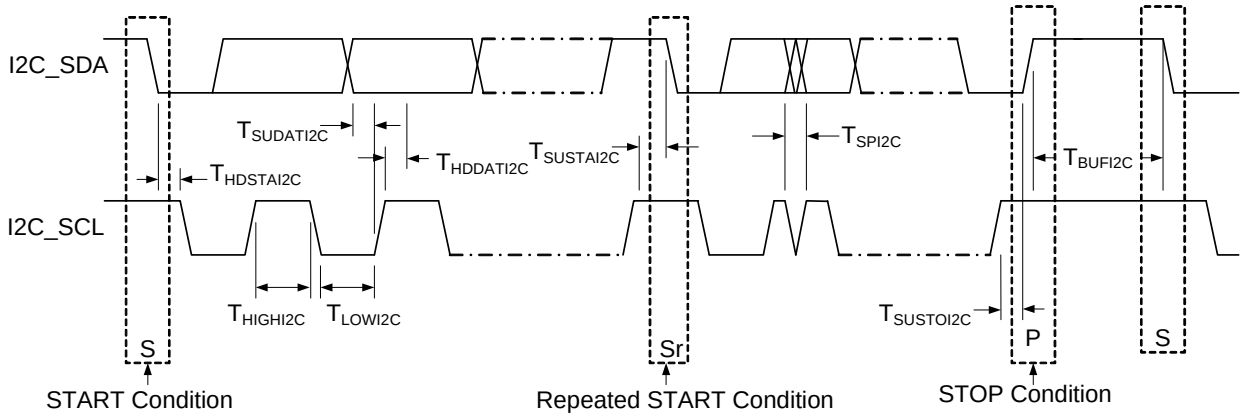
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 29. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard-Mode		Fast-Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz	
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs	
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs	
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	µs	
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs	
$T_{SUDATI2C}$	Data Setup Time	250	–	100[11]	–	ns	
$T_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	0.6	–	µs	
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs	
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter	–	–	0	50	ns	

Figure 20. Definition for Timing for Fast-/Standard-Mode on the I²C Bus Packaging Dimensions



Notes

10. For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com for more information.
11. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If this device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

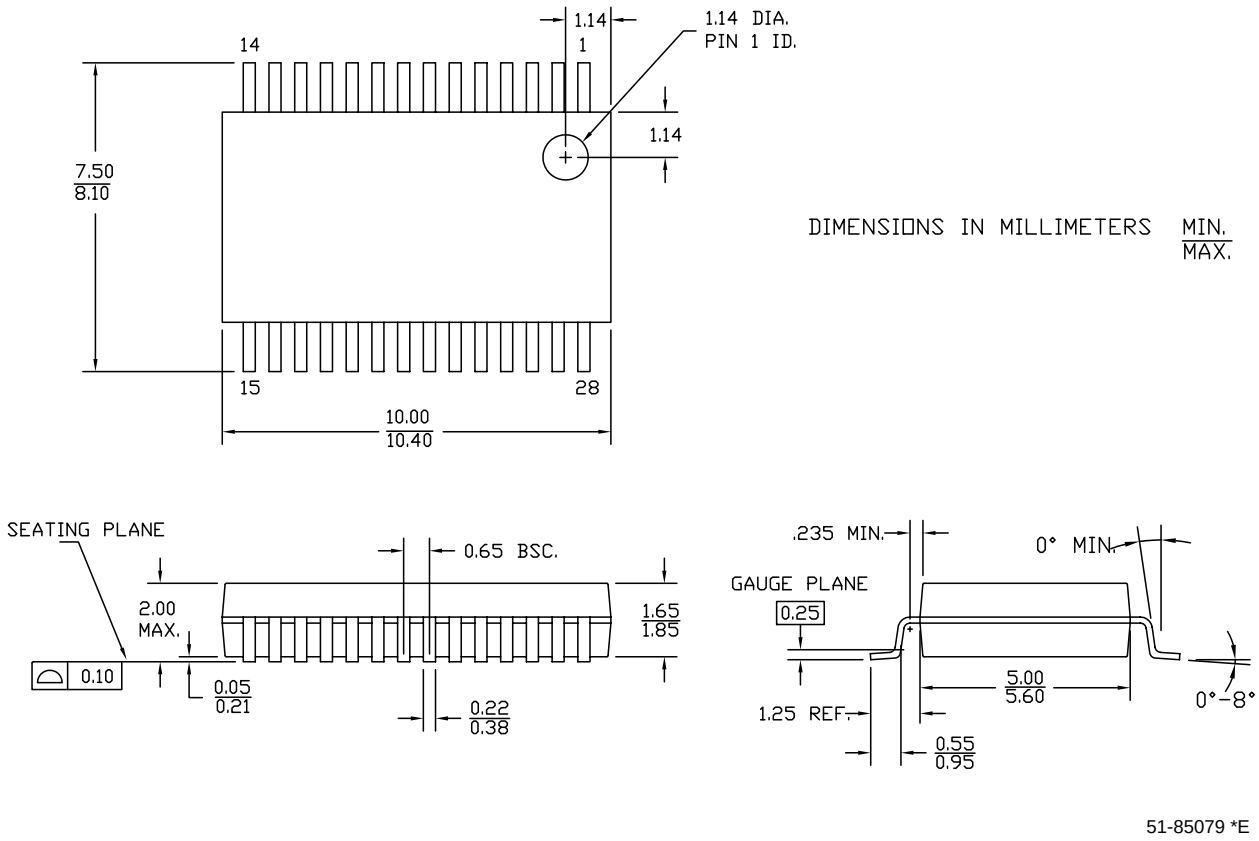
Packaging Information

This section illustrates the packaging specifications for the CY8CLED16P01 PLC device, along with the thermal impedances for each package, and the typical package capacitance on crystal pins.

Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the Emulator Pod Dimension drawings at http://www.cypress.com.

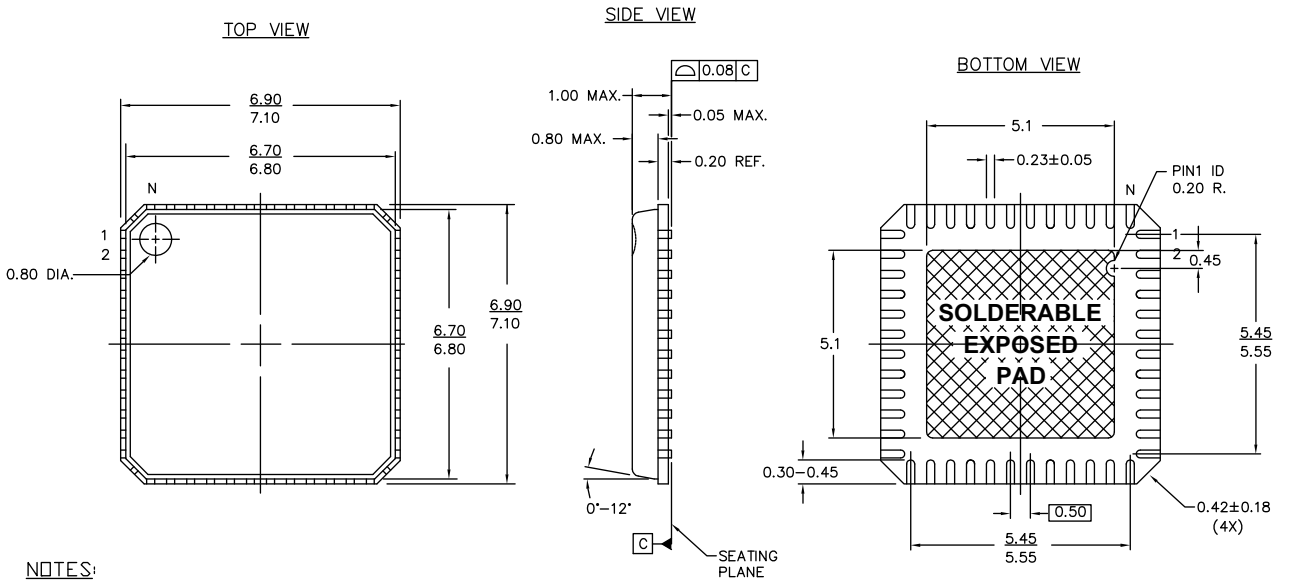
Packaging Dimensions

Figure 21. 28-pin SSOP (210 Mils) O28.21 Package Outline



51-85079 *E

Figure 22. 48-pin QFN (7 × 7 × 1.0 mm) LF48A/LY48A 5.1 × 5.1 E-Pad (Subcon Punch Type Package) Package Outline



NOTES:

1. ▨ HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF48A	STANDARD
LY48A	LEAD FREE

001-12919 *C

Important Note

For information on the preferred dimensions for mounting QFN packages, refer to Application Note, “Application Notes for Surface Mount Assembly of Amkor’s MicroLeadFrame (MLF) Packages” available at http://www.amkor.com.

Pinned vias for thermal conduction are not required for the low power PSoC devices.

Figure 23. 48-pin QFN (7 × 7 × 1.0 mm) LT48A 5.1 × 5.1 E-Pad (Sawn) Package Outline

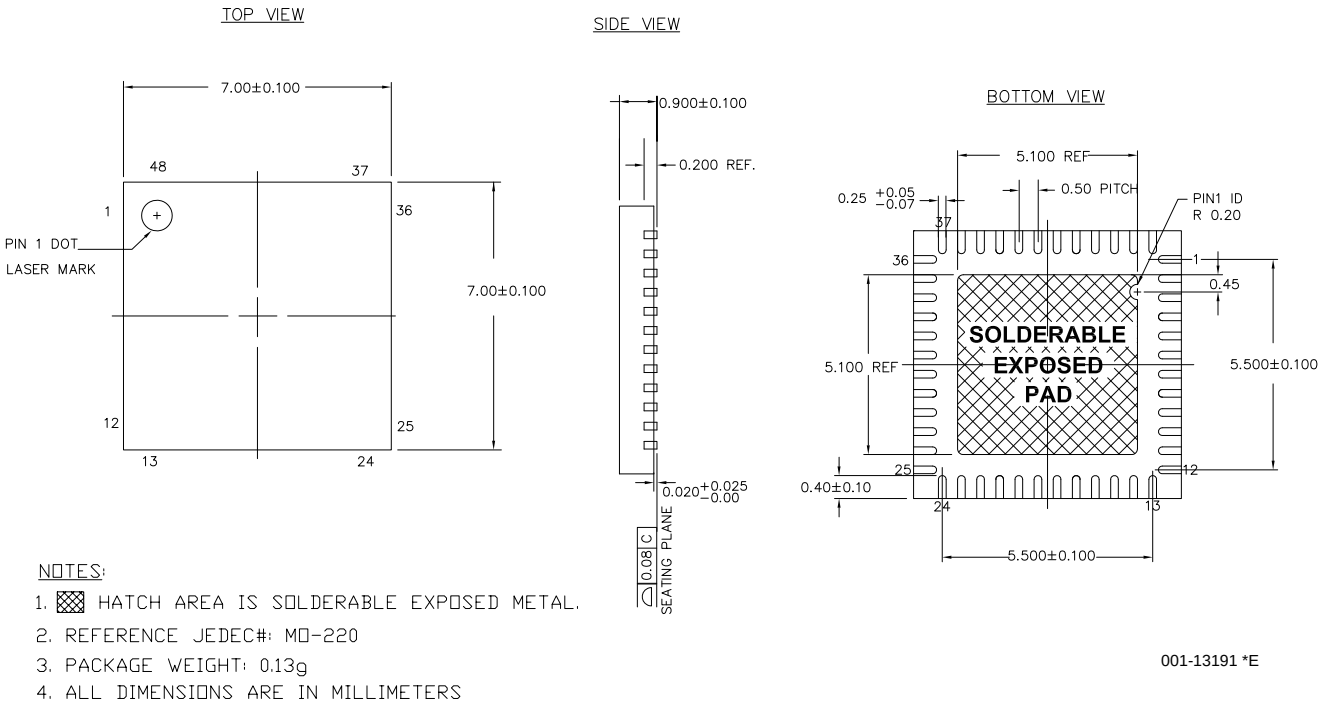
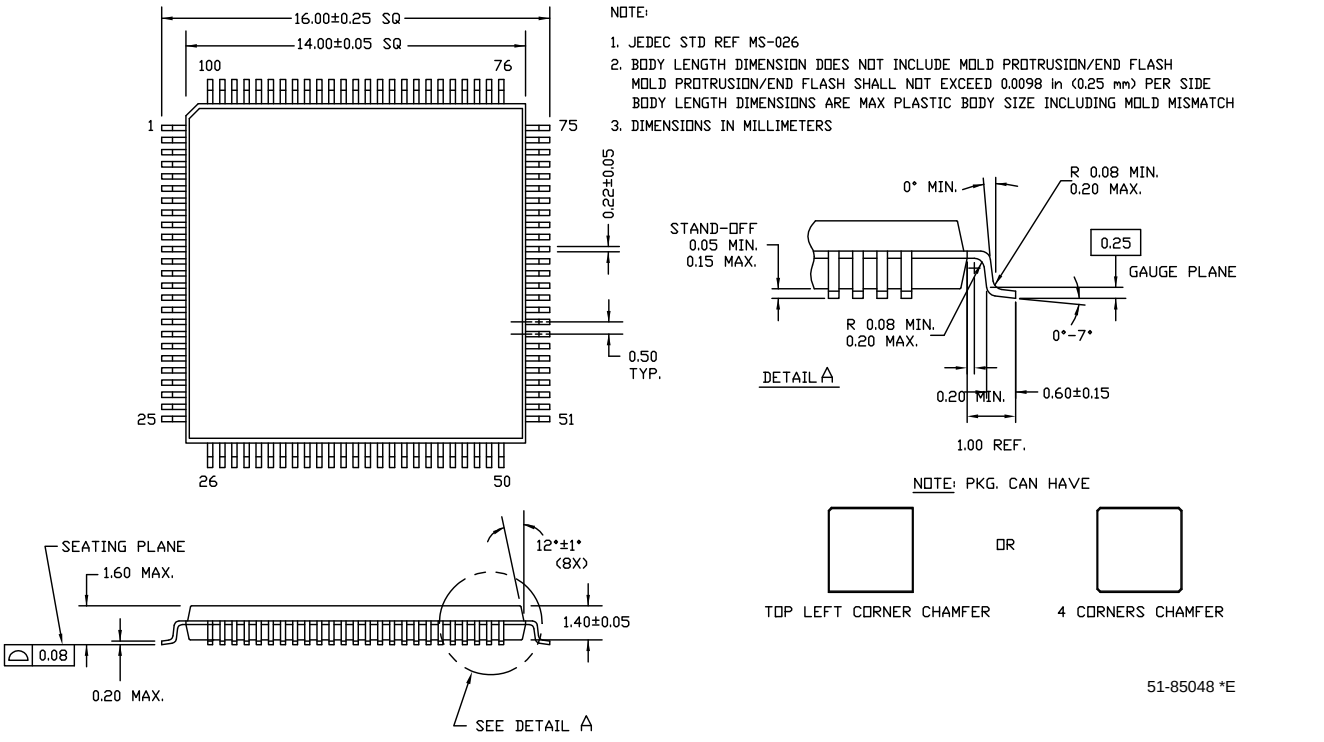


Figure 24. 100-pin TQFP (14 × 14 × 1.4 mm) A100SA Package Outline



Thermal Impedances

Table 30. Thermal Impedances per Package

Package	Typical θ_{JA}[12]	Typical θ_{JC}
28-pin SSOP	59 °C/W	23 °C/W
48-pin QFN[13]	15 °C/W	18 °C/W
100-pin TQFP	42 °C/W	15 °C/W

Capacitance on Crystal Pins

Table 31. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
28-pin SSOP	2.8 pF
48-pin QFN	1.8 pF
100-pin TQFP	3.1 pF

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 32. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Time at Maximum Peak Temperature
28-pin SSOP	260 °C	20 s
48-pin QFN	260 °C	20 s
100-pin TQFP	260 °C	20 s

Notes
12. $T_J = T_A + POWER \times \theta_{JA}$
13. To achieve the thermal impedance specified for the QFN package, refer to “Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages” available at http://www.amkor.com.

Development Tool Selection

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate firmware applications. PSoC Designer is available free of charge at http://www.cypress.com. PSoC Designer comes with a free C compiler.

PSoC Programmer

PSoC Programmer is a very flexible programming application. It is used on the bench in development and is also suitable for factory programming. PSoC Programmer works either in a standalone configuration or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

Device Programmers

All device programmers are sold at the Cypress.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- Three Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207 ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment.

Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

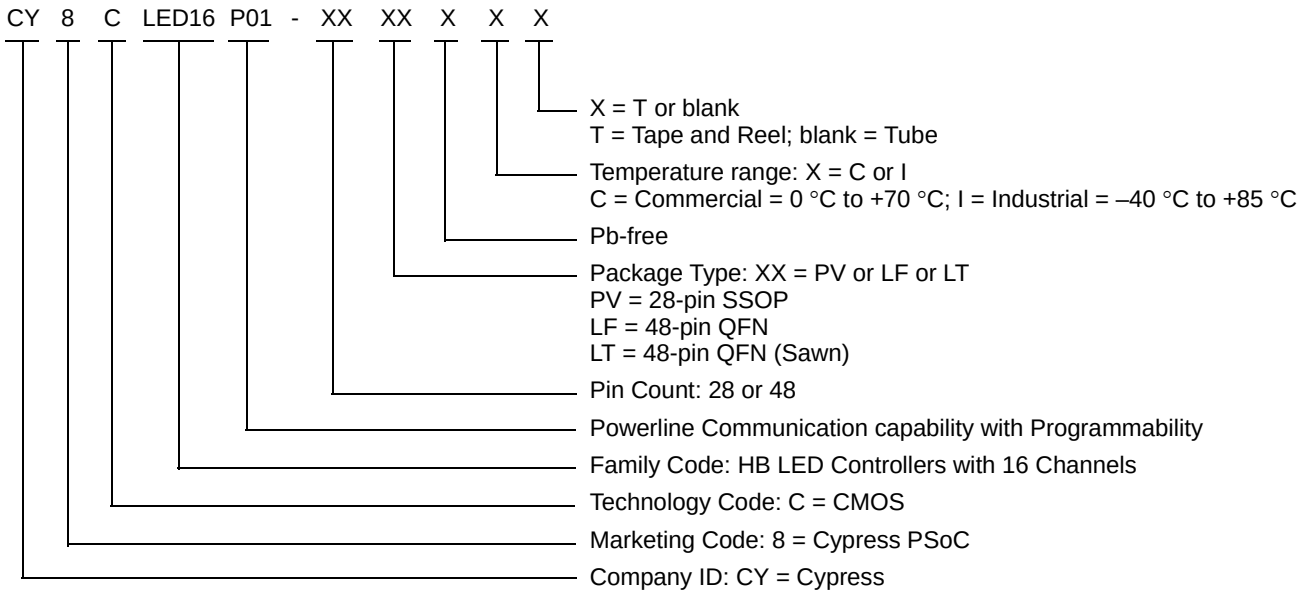
Ordering Information

The following table lists the CY8CLED16P01 PLC device family key package features and ordering codes. The CY8CLED16P01 devices are not recommended for new designs. Instead, the CY8CPLC20 device should be used for new designs.

Table 33. CY8CLED16P01 PLC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	RAM (Bytes)	Temperature Range	Digital PSoC Blocks	Analog PSoC Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
28-pin (210-Mil) SSOP [14]	CY8CLED16P01-28PVXI	32 K	2 K	–40 °C to +85 °C	16	12	24	12	4	Yes
28-pin (210-Mil) SSOP (Tape and Reel) [14]	CY8CLED16P01-28PVXIT	32 K	2 K	–40 °C to +85 °C	16	12	24	12	4	Yes
48-pin QFN [14]	CY8CLED16P01-48LFXI	32 K	2 K	–40 °C to +85 °C	16	12	44	12	4	Yes
48-pin QFN (Sawn) [14]	CY8CLED16P01-48LTXI	32 K	2 K	–40 °C to +85 °C	16	12	44	12	4	Yes
48-pin QFN (Sawn) (Tape and Reel) [14]	CY8CLED16P01-48LTXIT	32 K	2 K	–40 °C to +85 °C	16	12	44	12	4	Yes

Ordering Code Definitions



Note
14. Not recommended for new designs. Instead, the CY8CPLC20 device should be used for new designs.

Acronyms

Acronyms Used

Table 34 lists the acronyms that are used in this document.

Table 34. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MCU	microcontroller unit
ADC	analog-to-digital converter	MIPS	million instructions per second
API	application programming interface	OCD	on-chip debug
BIU	band-in-use	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PDIP	plastic dual-in-line package
CPU	central processing unit	PGA	programmable gain amplifier
CRC	cyclic redundancy check	PLC	powerline communication
CSMA	carrier sense multiple access	PLL	phase-locked loop
CT	continuous time	PLT	powerline transceiver
DAC	digital-to-analog converter	POR	power on reset
DC	direct current	PPOR	precision power on reset
DTMF	dual-tone multi-frequency	PRS	pseudo-random sequence
ECO	external crystal oscillator	PSoC®	Programmable System-on-Chip
EEPROM	electrically erasable programmable read-only memory	PWM	pulse width modulator
FSK	frequency-shift keying	QFN	quad flat no leads
GPIO	general-purpose I/O	RTC	real time clock
I/O	input/output	SAR	successive approximation
ICE	in-circuit emulator	SC	switched capacitor
IDE	integrated development environment	SLIMO	slow IMO
ILO	internal low speed oscillator	SPITM	serial peripheral interface
IMO	internal main oscillator	SRAM	static random access memory
IrDA	infrared data association	SROM	supervisory read only memory
ISSP	in-system serial programming	SSOP	shrink small-outline package
LCD	liquid crystal display	TQFP	thin quad flat pack
LED	light-emitting diode	UART	universal asynchronous receiver / transmitter
LPC	low power comparator	USB	universal serial bus
LPF	low pass filter	WDT	watchdog timer
LVD	low voltage detect	XRES	external reset
MAC	multiply-accumulate		

Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 (001-14503)

Estimating CY8CPLC20/CY8CLED16P01 Power Consumption – AN55403 (001-55403)

PSoC Dynamic Reconfiguration – AN2104 (001-36000)

Analog – ADC Selection – AN2239 (001-33719)

PrISM™ Technology for LED Dimming – AN47372 (001-47372)

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages – available at http://www.amkor.com.

Document Conventions

Units of Measure

Table 35 lists the units of measures.

Table 35. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
kB	1024 bytes	ms	millisecond
dB	decibels	mV	millivolts
°C	degree Celsius	nA	nanoampere
fF	femtofarad	ns	nanosecond
kHz	kilohertz	nV	nanovolt
kΩ	kilohm	ppm	parts per million
MHz	megahertz	%	percent
µA	microampere	pF	picofarad
µF	microfarad	ps	picosecond
µs	microsecond	pA	picoampere
µV	microvolts	rt-Hz	root hertz
µW	microwatts	V	volt
mA	milliampere	W	watt
mm	millimeter		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or 0x are decimals.

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
Application programming interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.

asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.
bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.

dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.
duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
External Reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
Flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.

master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device*.**
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
Phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
Power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is a type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.

settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning “voltage drain.” The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning “voltage source.” The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Document History Page

Document Title: CY8CLED16P01, Powerline Communication Solution Document Number: 001-49263				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	2575716	10/01/08	GHH / PYRS	New Datasheet
*A	2731927	07/06/09	GHH / HMT / DSG	Added - Configurable baud rates and FSK Frequencies - PLC Pod Kits for development purposes Modified - Pin Information for all packages
*B	2748537	See ECN	GHH	Added Sections on Getting Started and Document Conventions Modified the following Electrical Parameters AC Chip-Level Specifications - F_{IMO6} Min: Changed from 5.75 MHz to 5.5 MHz - F_{IMO6} Max: Changed from 6.35 MHz to 6.5 MHz AC Digital Block Specifications - SPIS (Maximum input clock frequency): Changed from 4.1 ns to 4.1 MHz AC Programming Specifications - T_{WRITE} (Flash Block Write Time): Changed from 40 ms to 10 ms
*C	2752799	08/17/09	GHH	Posting to external web.
*D	2759000	09/02/2009	GHH	Fixed typos in the data sheet. Updated Figure 2 on page 3 and Figure 5 on page 10.
*E	2778970	10/05/2009	FRE	Added a table for DC POR and LVD Specifications Updated DC GPIO Specifications, AC Chip-Level Specifications, and AC Programming Specifications as follows: AC Chip-Level Specifications - Modified F_{IMO6} AC Programming Specifications - Modified T_{WRITE} AC External Clock Specifications - Modified Power Up IMO to Switch DC GPIO Specifications - Added I_{OH}, I_{OL} AC Chip-Level Specifications - Added DC_{ILO}, F_{32K_U}, $T_{POWERUP}$, and SR_{POWER_UP} specifications AC Programming Specifications - Added $T_{ERASEALL}$ Added 48-Pin QFN (Sawn) package in Packaging Information and CY8CLED16P01-48LTXI and CY8CLED16P01-48LTXIT part details in the Ordering Information table Updated Development Tools and Table 5, Table 6, and Table 7 to state the requirement to use the external crystal for PLC protocol timing Table 5 and Figure 11: Changed pins 9 and 25 from NC to RSVD Table 6 and Figure 12: Changed pins 7 and 39 from NC to RSVD Table 7 and Figure 13: Changed pins 14 and 77 from NC to RSVD Table 5, Table 6, Table 7: Added explanation to Connect a 0.1 µF capacitor between XTAL_Stability and VSS. Fixed minor typos
*F	2846686	01/12/2010	FRE	Added Contents. Updated copyright and Sales URLs. Updated Packaging Information (28-pin SSOP, 48-pin QFN, 48-pin QFN (Sawn Type) package diagrams). Add footnote in Ordering Information table of CY8CPLC20-48LFXI stating, “Not recommended for new designs.” Updated Table 5, Table 6, Table 7 (Added capacitor description to AGND pin.)

Document History Page (continued)

Document Title: CY8CLED16P01, Powerline Communication Solution Document Number: 001-49263				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
*G	2903114	04/01/2010	NJF	Updated Cypress website links Updated Absolute Maximum Ratings (Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters). Updated Packaging Information.
*H	2938300	05/27/10	CGX	Minor ECN to post to external website
*I	3114960	12/19/10	NJF	Added DC I2C Specifications table. Updated Table 21 (Added F_{32K_U} max limit). Updated Table 21 (Added T_{jit_IMO} specification, removed existing jitter specifications). Updated Table 13, Table 15 and Table 16. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated Solder Reflow Peak Temperature. No specific changes were made to Table 25 and I^2C Timing Diagram. They were updated for clearer understanding. Updated Figure 18 since the labelling for y-axis was incorrect. Removed footnote reference for Table 32. Added the typical θ_{JC} parameter to the Table 30. Table 5 and Figure 11: Changed pin 25 from RSVD to P0[2]. Table 6 and Figure 12: Changed pin 39 from RSVD to P0[2]. Table 7 and Figure 13: Changed pin 77 from RSVD to P0[2].
*J	3284094	06/17/11	FRE	Updated Getting Started, Development Tools, and Designing with PSoC Designer
*K	3380327	09/22/2011	FRE	Removed the sections “Development Kits” and “Evaluation Kits” under the main section Development Tool Selection. Updated Ordering Information (Changed the status of all devices to “Not Recommended for New Designs” and removed the CY8CLED16P01-OCD device).

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 5