CY23FP12-002

200-MHz Field Programmable Zero Delay Buffer

Features

- Pre-programmed configuration
- Fully field-programmable
  - Input and output dividers
  - Inverting/non inverting outputs
  - Phase-locked loop (PLL) or fanout buffer configuration
- 10 MHz to 200 MHz operating range
- Split 2.5-V or 3.3-V outputs
- Two low-voltage complementary metal oxide semiconductor (LVCMOS) reference inputs
- Twelve low-skew outputs
  - Output-output skew < 200 ps
  - Device-device skew < 500 ps
- Input-output skew < 250 ps
- Cycle-cycle jitter < 100 ps (typical)
- Three-stateable outputs
- Less than 50 µA shutdown current
- Spread Aware™
- 28-pin shrunk small outline package (SSOP)
- 3.3-V operation

Functional Description

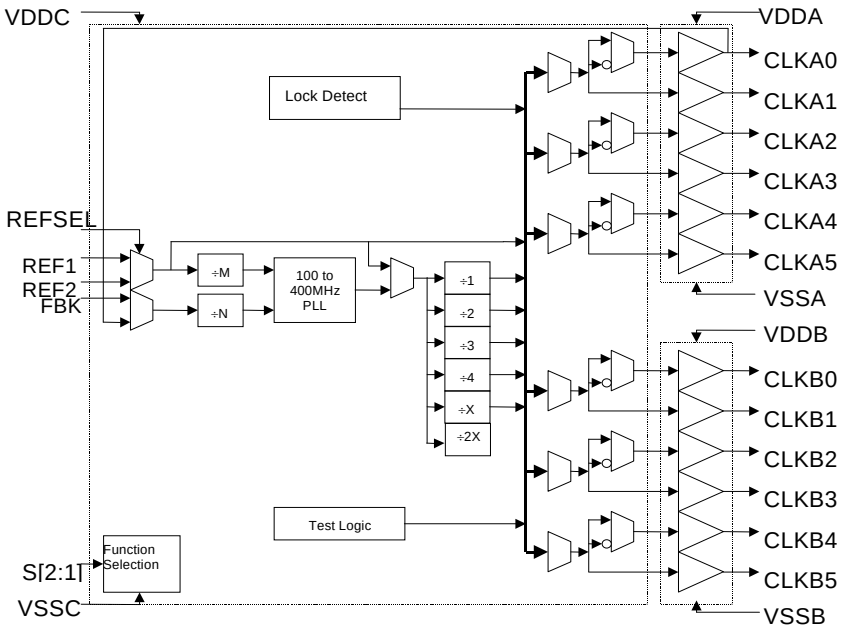
The CY23FP12-002 is a pre-programmed version of the CY23FP12. It features a high-performance fully field-programmable 200-MHz zero delay buffer designed for high-speed clock distribution. The integrated PLL is designed for low jitter and optimized for noise rejection. These parameters are critical for reference clock distribution in systems using high-performance ASICs and microprocessors.

The CY23FP12-002 is fully programmable through volume or prototype programmers, enabling the user to define an application-specific zero delay buffer with customized input and output dividers, feedback topology (internal/external), output inversions, and output drive strengths. For additional flexibility, the user can mix and match multiple functions, listed in Table 2 on page 5, and assign a particular function set to any one of the four possible S1-S2 control bit combinations. This feature enables the implementation of four distinct personalities, selectable with S1-S2 bits, on a single programmed silicon. The CY23FP12-002 also features a proprietary auto power down circuit that shuts down the device in case of a REF failure, resulting in less than 50 µA of current draw.

The CY23FP12-002 provides 12 outputs grouped in two banks with separate power supply pins which can be connected independently to either a 2.5 V or a 3.3 V rail.

Selectable reference input is a fault tolerance feature which allows for glitch-free switch over to secondary clock source when REFSEL is asserted/deasserted.

Logic Block Diagram



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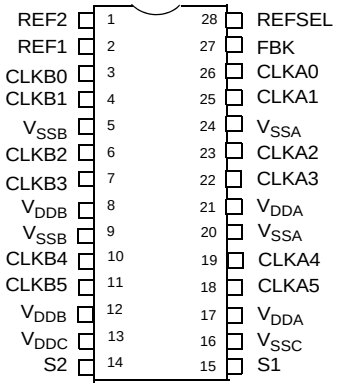
Pin Configuration

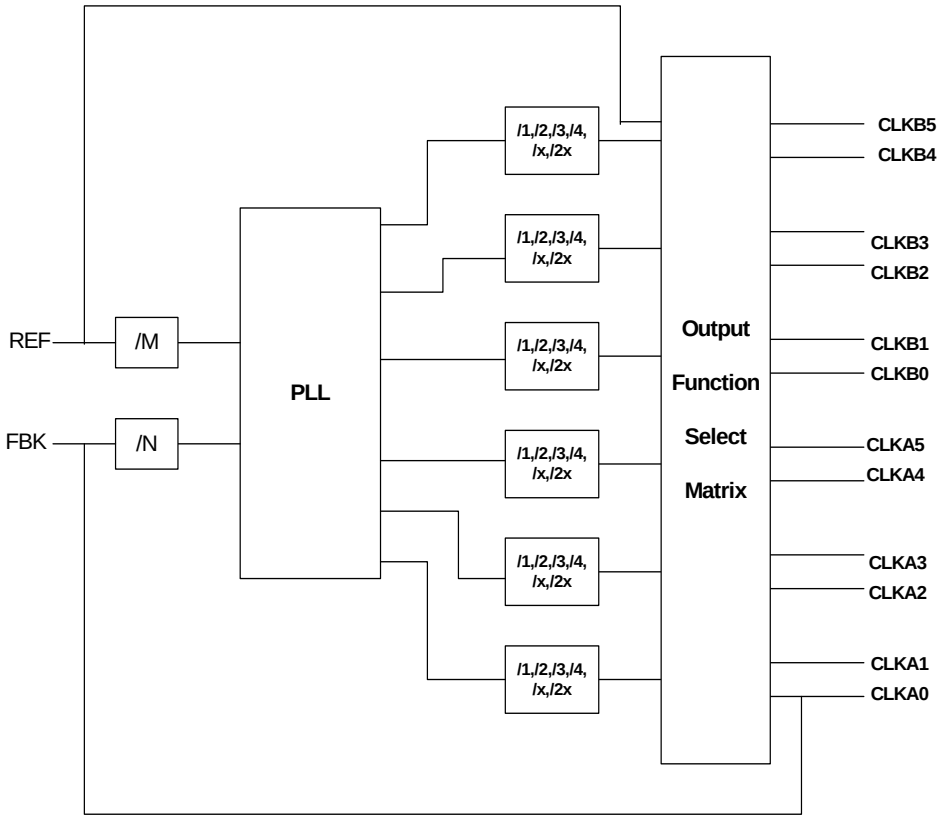
Figure 1. 28-Pin SSOP



Pin Description

Pin	Name	I/O	Type	Description
1	REF2	I	LVTTL/LVCMOS	Input reference frequency, 5 V-tolerant input.
2	REF1	I	LVTTL/LVCMOS	Input reference frequency, 5 V-tolerant input.
3	CLKB0	O	LVTTL	Clock output, Bank B.
4	CLKB1	O	LVTTL	Clock output, Bank B.
5	V_{SSB}	PWR	POWER	Ground for Bank B.
6	CLKB2	O	LVTTL	Clock output, Bank B.
7	CLKB3	O	LVTTL	Clock output, Bank B.
8	V_{DDB}	PWR	POWER	2.5-V or 3.3-V supply, Bank B.
9	V_{SSB}	PWR	POWER	Ground for Bank B.
10	CLKB4	O	LVTTL	Clock output, Bank B.
11	CLKB5	O	LVTTL	Clock output, Bank B.
12	V_{DDB}	PWR	POWER	2.5-V or 3.3-V supply, Bank B.
13	V_{DDC}	PWR	POWER	3.3 V core supply.
14	S2	I	LVTTL	Select input.
15	S1	I	LVTTL	Select input.
16	V_{SSC}	PWR	POWER	Ground for core.
17	V_{DDA}	PWR	POWER	2.5-V or 3.3-V supply, Bank A.
18	CLKA5	O	LVTTL	Clock output, Bank A.
19	CLKA4	O	LVTTL	Clock output, Bank A.
20	V_{SSA}	PWR	POWER	Ground for Bank A.
21	V_{DDA}	PWR	POWER	2.5-V or 3.3-V supply Bank A.
22	CLKA3	O	LVTTL	Clock output, Bank A.
23	CLKA2	O	LVTTL	Clock output, Bank A.
24	V_{SSA}	PWR	POWER	Ground for Bank A.
25	CLKA1	O	LVTTL	Clock output, Bank A.
26	CLKA0	O	LVTTL	CLock output, Bank A.
27	FBK	I	LVTTL	PLL feedback input.
28	REFSEL	I	LVTTL	Reference select input. When REFSEL = 0, REF1 is selected. When REFSEL = 1, REF2 is selected.

Figure 2. Basic PLL Block Diagram



Following is a list of independent functions that can be programmed with a volume or prototype programmer on the “pre-programmed” silicon.

Table 1. Programmable Functions

Configuration	Description	Default
DC Drive Bank A	Programs the drive strength of Bank A outputs. The user can select one out of two possible drive strength settings that produce output DC currents in the range of ±16 mA to ±20 mA.	±20 mA
DC Drive Bank B	Programs the drive strength of Bank B outputs. The user can select one out of two possible drive strength settings that produce output DC currents in the range of ±16 mA to ±20 mA.	±20 mA
Output Enable for Bank B clocks	Enables/disables CLKB[5:0] outputs. Each of the six outputs can be disabled *individually* if not used, to minimize electromagnetic interference (EMI) and switching noise.	Enable
Output Enable for Bank A clocks	Enables/disables CLKA[5:0] outputs. Each of the six outputs can be disabled *individually* if not used, to minimize EMI and switching noise.	Enable
Inv CLKA0	Generates an inverted clock on the CLKA0 output. When this option is programmed, CLKA0 and CLKA1 will become complimentary pairs.	Non invert
Inv CLKA2	Generates an inverted clock on the CLKA2 output. When this option is programmed, CLKA2 and CLKA3 will become complimentary pairs.	Non invert
Inv CLKA4	Generates an inverted clock on the CLKA4 output. When this option is programmed, CLKA4 and CLKA5 will become complimentary pairs.	Non invert
Inv CLKB0	Generates an inverted clock on the CLKB0 output. When this option is programmed, CLKB0 and CLKB1 will become complimentary pairs.	Non invert

Table 1. Programmable Functions (continued)

Configuration	Description	Default
Inv CLKB2	Generates an inverted clock on the CLKB2 output. When this option is programmed, CLKB2 and CLKB3 will become complimentary pairs.	Non-invert
Inv CLKB4	Generates an inverted clock on the CLKB4 output. When this option is programmed, CLKB4 and CLKB5 will become complimentary pairs.	Non-invert
Pull down Enable	Enables/disables internal pulldowns on all outputs	Enable
Fbk Pull down Enable	Enables/disables internal pulldowns on the feedback path (applicable to both internal and external feedback topologies)	Enable
Fbk Sel	Selects between the internal and the external feedback topologies	Internal

The following table lists independent functions, which can be assigned to each of the four S1 and S2 combinations. When a particular S1 and S2 combination is selected, the device assumes the configuration (which is essentially a set of functions given in Table 2) that has been preassigned to that particular combination.

Table 2. Programmable Functions for S1/S2 Combinations

Function	Description	Default
Output Enable CLKB[5:4]	Enables/disables CLKB[5:4] output pair	Enable
Output Enable CLKB[3:2]	Enables/disables CLKB[3:2] output pair	Enable
Output Enable CLKB[1:0]	Enables/disables CLKB[1:0] output pair	Enable
Output Enable CLKA[5:4]	Enables/disables CLKA[5:4] output pair	Enable
Output Enable CLKA[3:2]	Enables/disables CLKA[3:2] output pair	Enable
Output Enable CLKA[1:0]	Enables/disables CLKA[1:0] output pair	Enable
Auto Power down Enable	Enables/disables the auto power down circuit, which monitors the reference clock rising edges and shuts down the device in case of a reference 'failure.' This failure is triggered by a drift in reference frequency below a set limit. This auto power down circuit is disabled internally when one or more of the outputs are configured to be driven directly from the reference clock.	Enable
PLL Power down	Shuts down the PLL when the device is configured as a non-PLL fanout buffer.	See Table 4 on page 6
M[7:0]	Assigns an eight-bit value to reference divider –M. The divider can be any integer value from 1 to 256; however, the PLL input frequency cannot be lower than 10 MHz.	See Table 4 on page 6
N[7:0]	Assigns an eight-bit value to feedback divider –N. The divider can be any integer value from 1 to 256; however, the PLL input frequency cannot be lower than 10 MHz.	See Table 4 on page 6
X[6:0]	Assigns a seven-bit value to output divider –X. The divider can be any integer value from 5 to 130. Divide by 1,2,3, and 4 are preprogrammed on the device and can be activated by the appropriate output mux setting.	See Table 4 on page 6
Divider Source	Selects between the PLL output and the reference clock as the source clock for the output dividers.	See Table 4 on page 6
CLKA54 Source	Independently selects one out of the eight possible output dividers that will connect to the CLKA5 and CLKA4 pair. Please refer to Table 3 on page 6 for a list of divider values.	See Table 4 on page 6
CLKA32 Source	Independently selects one out of the eight possible output dividers that will connect to the CLKA3 and CLKA2 pair. Please refer to Table 3 on page 6 for a list of divider values.	See Table 4 on page 6
CLKA10 Source	Independently selects one out of the eight possible output dividers that will connect to the CLKA1 and CLKA0 pair. Please refer to Table 3 on page 6 for a list of divider values.	See Table 4 on page 6
CLKB54 Source	Independently selects one out of the eight possible output dividers that will connect to the CLKB5 and CLKB4 pair. Please refer to Table 3 on page 6 for a list of divider values.	See Table 4 on page 6
CLKB32 Source	Independently selects one out of the eight possible output dividers that will connect to the CLKB3 and CLKB2 pair. Please refer to Table 3 on page 6 for a list of divider values.	See Table 4 on page 6
CLKB10 Source	Independently selects one out of the eight possible output dividers that will connect to the CLKB1 and CLKB0 pair. Please refer to Table 3 on page 6 for a list of divider values.	See Table 4 on page 6

Table 3 is a list of output dividers that are independently selected to connect to each output pair.

In the default (pre-programmed) state of the device, S1 and S2 pins will function as indicated in Table 4. The CY23FP12-002 can be programmed to other configurations.

Table 3. Output Dividers

CLKA/B Source	Output Connects To
0 [000]	REF
1 [001]	Divide by 1
2 [010]	Divide by 2
3 [011]	Divide by 3
4 [100]	Divide by 4
5 [101]	Divide by X
6 [110]	Divide by 2X[1]
7 [111]	TEST mode [LOCK signal][2]

Table 4. Pre-Programmed Configuration

Outputs	S2, S1	DivSrc	Example Output		
			REF Input (MHz)	VCO (MHz)	Output (MHz)
ClkA0, A1	00	1	25	200	200
ClkA2, A3	00	3	25	200	66.7
ClkA4, A5	00	X=6	25	200	33.3
ClkB0, B1	00	X=6	25	200	33.3
ClkB2, B3	00	4	25	200	50
ClkB4, B5	00	Ref	25	200	25
ClkA0, A1	01	4	100	200	50
ClkA2, A3	01	4	100	200	50
ClkA4, A5	01	4	100	200	50
ClkB0, B1	01	4	100	200	50
ClkB2, B3	01	X=8	100	200	25
ClkB4, B5	01	X=8	100	200	25
ClkA0, A1	10	X=8	33.3	266.6	33.3
ClkA2, A3	10	X=8	33.3	266.6	33.3
ClkA4, A5	10	X=8	33.3	266.6	33.3
ClkB0, B1	10	4	33.3	266.6	66.6
ClkB2, B3	10	4	33.3	266.6	66.6
ClkB4, B5	10	4	33.3	266.6	66.6
ClkA0, A1	11	Ref	100	powerdown	100
ClkA2, A3	11	Ref	100	powerdown	100
ClkA4, A5	11	Ref	100	powerdown	100
ClkB0, B1	11	2	100	powerdown	50
ClkB2, B3	11	2	100	powerdown	50
ClkB4, B5	11	2	100	powerdown	50

Notes

1. Outputs will be rising edge aligned only to those outputs using this same device setting.
2. When the source of an output pair is set to [111], the output pair becomes lock indicator signal. For example, if the source of an output pair (CLKA0, CLKA1) is set to [111], the CLKA0 and CLKA1, becomes lock indicator signals. In non-invert mode, CLKA0 and CLKA1 signals will be high when the PLL is in lock mode. If CLKA0 is in an invert mode, the CLKA0 will be low and the CLKA1 will be high when the PLL is in lock mode.

Field Programming the CY23FP12-002

The CY23FP12-002 comes pre-programmed and ready for use, but it can also be reprogrammed to any other valid configuration. When programming, it must be programmed in a device programmer prior to being installed in a circuit. The CY23FP12-002 is based on flash technology, so it can be reprogrammed up to 100 times. This enables fast and easy design changes and product updates, and eliminates any issues with old and out-of-date inventory.

Samples and small prototype quantities can be programmed on the CY3672-USB programmer. Cypress's value-added distribution partners and third-party programming systems from BP Microsystems, HiLo Systems, and others are available for large production quantities.

CyberClocks™ Software

CyberClocks is an easy-to-use software application that allows the user to custom-configure the CY23FP12-002. Users can specify the REF, PLL frequency, output frequencies and/or post-dividers, and different functional options. CyberClocks outputs an industry standard JEDEC file used for programming the CY23FP12-002.

CyberClocks can be downloaded free of charge from the Cypress website at www.cypress.com.

CY3672-USB Development Kit

The Cypress CY3672-USB Developer Kit, in combination with the CY3692 Socket Adapter, is used to program samples and small prototype quantities of the CY23FP12-002. This portable programmer connects to a PC through a USB interface.

The JEDEC file output of CyberClocks can be downloaded to the portable programmer for small-volume programming, or for use with a production programming system for larger volumes.

CY23FP12-002 Frequency Calculation

The CY23FP12-002 is an extremely flexible clock buffer with up to 12 individual outputs, generated from an integrated PLL. Four variables are used to determine the final output frequency. These are the input reference frequency, the M and N dividers, and the post divider.

The basic PLL block diagram is shown in Figure 2 on page 4. Each of the six clock output pairs has many post divider options available to it. X is a programmable value between 5 and 130, and 2X is twice that value. There are six post divider options: /1, /2, /3, /4, /X, and /2X. The post divider options can be applied to the calculated PLL frequency or to the REF directly. The feedback is connected either internally to CLKA0 or externally to any output.

A programmable divider, M, is inserted between the reference input, REF, and the phase detector. The divider M can be any integer 1 to 256. The PLL input frequency cannot be lower than 10 MHz or higher than 200 MHz. A programmable divider, N, is inserted between the feedback input, FBK, and the phase detector. The divider N can be any integer 1 to 256. The PLL input frequency cannot be lower than 10 MHz or higher than 200 MHz.

The output can be calculated as follows:
$F_{REF} / M = F_{FBK} / N$.
$F_{PLL} = (F_{REF} * N * \text{post divider}) / M$.
$F_{OUT} = F_{PLL} / \text{post divider}$.

In addition to above divider options, another option bypasses the PLL and passes the REF directly to the output.

$F_{OUT} = F_{REF}$.

Absolute Maximum Conditions

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	Supply voltage	Nonfunctional	–0.5	7	VDC
V_{IN}	Input voltage REF	Relative to V_{CC}	–0.5	V_{DD} + 0.5	VDC
V_{IN}	Input voltage Except REF	Relative to V_{CC}	–0.5	V_{DD} + 0.5	VDC
LU_I	Latch up immunity	Functional	300		mA
T_S	Temperature, storage	Nonfunctional	–65	125	°C
T_J	Junction temperature	–	–	125	°C
$Ø_{Jc}$	Dissipation, junction to case	Functional	30		°C/W
$Ø_{Ja}$	Dissipation, junction to ambient	Functional	67		°C/W
ESD_h	ESD protection (human body model)	–	2000		V
M_{SL}	Moisture sensitivity level	–	MSL – 1		class
G_{ATES}	Total functional gate count	Assembled die	21375		each
UL–94	Flammability rating	At 1/8 in.	V–0		class
FIT	Failure in time	Manufacturing test	10		ppm

Operating Conditions

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{DDC}	Core supply voltage	–	3.135	3.465	V
V_{DDA}, V_{DDB}	Bank A, bank B supply voltage	–	3.135	3.465	V
		–	2.375	2.625	V
T_A	Temperature, operating ambient	Commercial temperature	0	70	°C
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	–	0.05	500	ms

DC Electrical Specifications

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input LOW voltage[3]	–	–	–	0.3 × V_{DD}	V
V_{IH}	Input HIGH voltage[3]	–	0.7 × V_{DD}	–	–	V
I_{IL}	Input LOW current[3]	V_{IN} = 0 V	–	–	50	µA
I_{IH}	Input HIGH current[3]	V_{IN} = V_{DD}	–	–	50	µA
V_{OL}	Output LOW voltage[4]	V_{DDA}/V_{DDB} = 3.3 V, I_{OL} = 16 mA (standard drive) V_{DDA}/V_{DDB} = 3.3 V, I_{OL} = 20 mA (high drive) V_{DDA}/V_{DDB} = 2.5 V, I_{OL} = 16 mA (high drive)	–	–	0.5	V
V_{OH}	Output HIGH voltage[4]	V_{DDA}/V_{DDB} = 3.3 V, I_{OH} = –16 mA (standard drive) V_{DDA}/V_{DDB} = 3.3 V, I_{OH} = –20 mA (high drive) V_{DDA}/V_{DDB} = 2.5 V, I_{OH} = –16 mA (high drive)	V_{DD} – 0.5	–	–	V
I_{DDS}	Power-down supply current	REF = 0 MHz	–	12	50	µA
I_{DD}	Supply current	V_{DDA} = V_{DDB} = 2.5 V, Unloaded outputs at 166 MHz	–	40	65	mA
		V_{DDA} = V_{DDB} = 2.5 V, Loaded outputs at166 MHz, C_L = 15 pF	–	65	100	
		V_{DDA} = V_{DDB} = 3.3 V, Unloaded outputs at 166 MHz	–	50	80	
		V_{DDA} = V_{DDB} = 3.3 V, Loaded outputs at 166 MHz, C_L = 15 pF	–	100	120	

Notes
3. Applies to both REF Clock and FBK.
4. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics [5]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
f_{REF}	Reference frequency[6]		10	–	200	MHz
ER_{REF}	Reference edge rate		1	–	–	V/ns
DC_{REF}	Reference duty cycle		25	–	75	%
f_{OUT}	Output frequency[7]	C_L = 15 pF	10	–	200	MHz
		C_L = 30 pF	10	–	100	
DC_{OUT}	Output duty cycle[5]	$V_{DDA/B}$ = 3.3 V, measured at $V_{DD}/2$	45	50	55	%
		$V_{DDA/B}$ = 2.5 V, measured at $V_{DD}/2$	40	50	60	
t_3	Rise time[5]	$V_{DDA/B}$ = 3.3 V, 0.8 V to 2.0 V, C_L = 30 pF (standard drive and high drive)	–	–	1.6	ns
		$V_{DDA/B}$ = 3.3 V, 0.8 V to 2.0 V, C_L = 15 pF (standard drive and high drive)	–	–	0.8	
		$V_{DDA/B}$ = 2.5 V, 0.6 V to 1.8 V, C_L = 30 pF (high drive only)	–	–	2.0	
		$V_{DDA/B}$ = 2.5 V, 0.6 V to 1.8 V, C_L = 15 pF (high drive only)	–	–	1.0	
t_4	Fall time[5]	$V_{DDA/B}$ = 3.3 V, 0.8 V to 2.0 V, C_L = 30 pF (standard drive and high drive)	–	–	1.6	ns
		$V_{DDA/B}$ = 3.3 V, 0.8 V to 2.0 V, C_L = 15 pF (standard drive and high drive)	–	–	0.8	
		$V_{DDA/B}$ = 2.5 V, 0.6 V to 1.8 V, C_L = 30 pF (high drive only)	–	–	1.6	
		$V_{DDA/B}$ = 2.5 V, 0.6 V to 1.8 V, C_L = 15 pF (high drive only)	–	–	0.8	
TTB	Total timing budget,[8,9] Bank A and B same frequency	Outputs at 200 MHz, tracking skew not included	–	–	650	ps
	Total timing budget, bank A and B different frequency		–	–	850	
t_5	Output-to-output skew[5]	All outputs equally loaded	–	–	200	ps
	Bank-to-bank skew	Same frequency	–	–	200	
	Bank-to-bank skew	Different frequency	–	–	400	
	Bank-to-bank skew	Different voltage, same frequency	–	–	400	
t_6	Input-to-output skew (static phase offset)[5]	Measured at $V_{DD}/2$, REF to FBK	–	0	250	ps
t_7	Device-to-device skew[5]	Measured at $V_{DD}/2$	–	0	500	ps
t_J	Cycle-to-cycle jitter[5] (Peak-to-peak)	Bank A and B same frequency	–	–	200	ps
	Cycle-to-cycle jitter[[5] (Peak-to-peak)	Bank A and B different frequency	–	–	400	

Notes

5. All parameters are specified with loaded outputs.
6. When the device is configured as a non-PLL fanout buffer (PLL Power down enabled), the reference frequency can be lower than 10MHz. With auto power down disabled and PLL power down enabled, the reference frequency can be as low as DC level.
7. When the device is configured as a non-PLL fanout buffer (PLL Power down enabled), the output frequency can be lower than 10MHz. With auto power down disabled and PLL power down enabled, the output frequency can be as low as DC level.
8. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.
9. TTB is the window between the earliest and the latest output clocks with respect to the input reference clock across variations in output frequency, supply voltage, operating temperature, input clock edge rate, and process. The measurements are taken with the AC test load specified and include output-output skew, cycle-cycle jitter, and dynamic phase error.TTB will be equal to or smaller than the maximum specified value at a given frequency.

Switching Characteristics (continued)[5]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
t_{TSK}	Tracking skew	Input reference clock at < 50-KHz modulation with ±3.75% spread	–	–	200	ps
t_{LOCK}	PLL lock time[5]	Stable power supply, valid clock at REF	–	–	1.0	ms
t_{LD}	Inserted loop delay	Max loop delay for PLL Lock (stable frequency)	–	–	7	ns
		Max loop delay to meet Tracking Skew Spec	–	–	4	ns

Switching Waveforms

Figure 3. Duty Cycle Timing

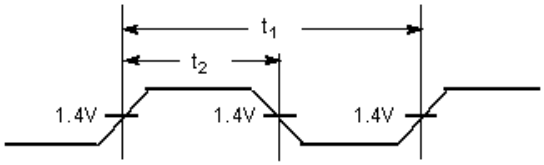


Figure 4. All Outputs Rise/Fall Time

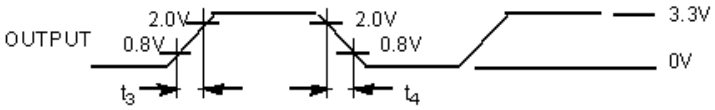


Figure 5. Output-Output Skew

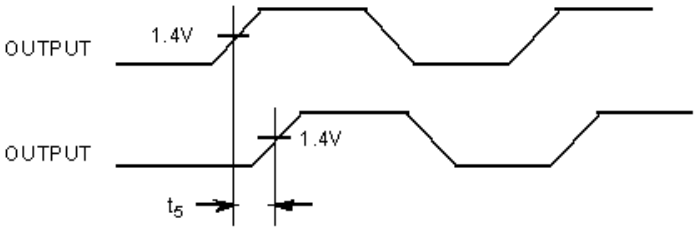


Figure 6. Input-Output Propagation Delay

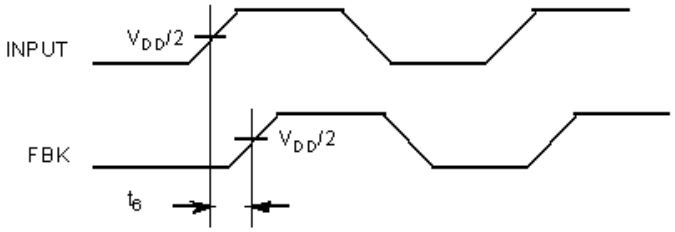
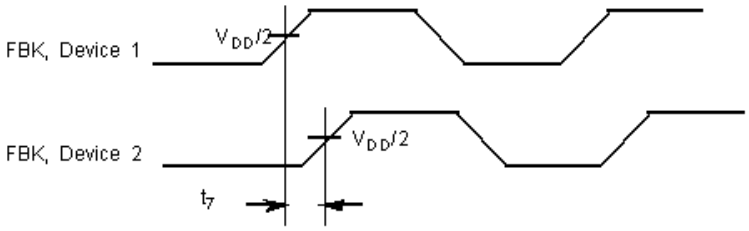
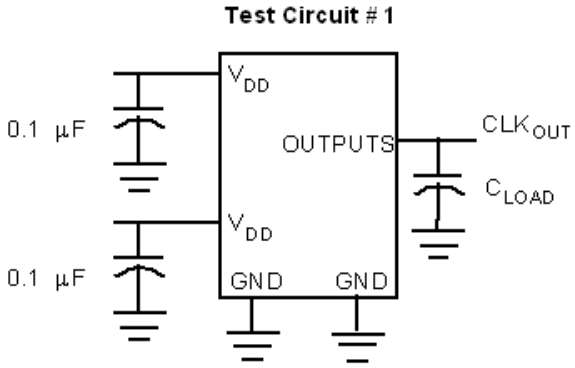


Figure 7. Device-Device Skew



Test Circuits

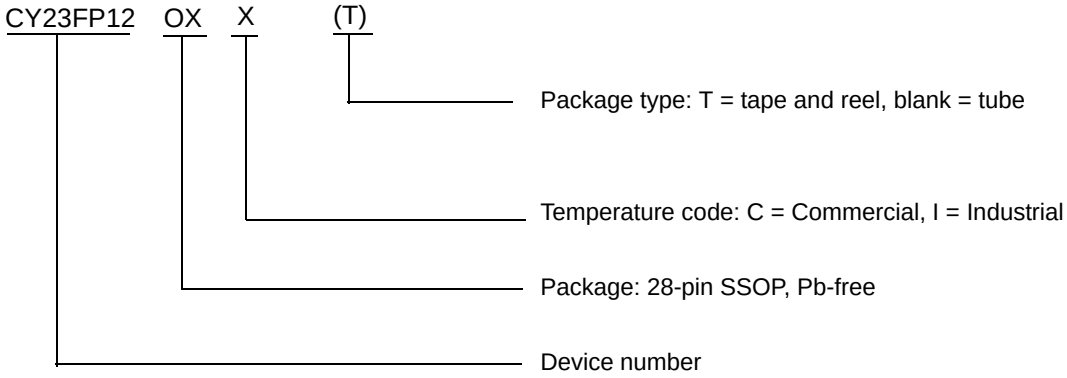


Test Circuit for all parameters

Ordering Information

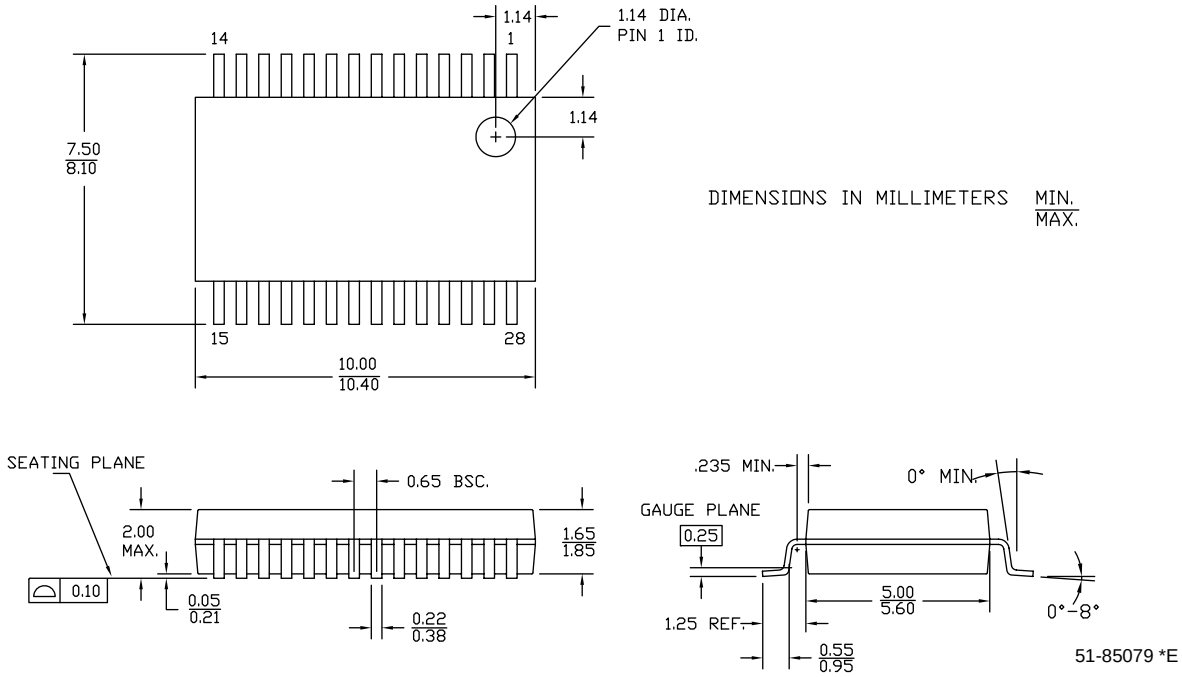
Ordering Code	Package Type	Operating Range
Pb-free		
CY23FP12OXC-002	28-pin SSOP	Commercial, 0 °C to 70 °C
CY23FP12OXC-002T	28-pin SSOP – Tape and Reel	Commercial,0 °C to 70 °C
Programmer		
CY3672-USB	Programmer with USB Interface	
CY3692	CY23FP12 Socket Adapter for CY3672-USB Programmer (Label CY3672 ADP006)	

Ordering Code Definition



Package Drawing and Dimension

Figure 8. 28-Pin (5.3 mm) Shrunk Small Outline Package



Acronyms

Acronym	Description
DCXO	digitally controlled crystal oscillator
ESD	electrostatic discharge
PLL	phase-locked loop
RMS	root mean square
SSOP	shrunk small outline package
XTAL	crystal

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	micro amperes
mA	milli amperes
ms	milli seconds
MHz	Mega Hertz
ns	nano seconds
pF	pico Farad
ps	pico seconds
V	Volts

Document History Page

Document Title: CY23FP12-002 200-MHz Field Programmable Zero Delay Buffer Document Number: 38-07644				
REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	206761	See ECN	RGL	New Data Sheet
*A	2865396	01/25/2010	KVM	Updated template. Removed references to industrial temperature range Added captions to tables 1-4. Added Operating Conditions table. Various edits to text. Removed “FTG” from text about the CY3672 programmer. Added part numbers CY23FP12OXC-002, CY23FP12OXC-002T Removed part numbers CY23FP12OC-002, CY23FP12OC-002T, CY23FP12OI-002 and CY23FP12OI-002T Changed part number CY3672 to CY3672-USB. Updated package drawing.
*B	3146346	01/18/2011	BASH	Modified VIN max value from 7 to V_{DD} + 0.5 in Absolute Maximum Conditions. Added Acronyms, Document Conventions, and Ordering Code Definition
*C	3373869	09/20/2011	PURU	Added hyper link in page 7 Updated Package Drawing and Dimension. Updated Absolute Maximum Conditions Table.

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