Low Skew Clock Buffer

Features

- All outputs skew < 100 ps typical (250 max)
- 15 to 80 MHz output operation
- Zero input to output delay
- 50% duty cycle outputs
- Outputs drive 50 Ω terminated lines
- Low operating current
- 24-pin small-outline integrated circuit (SOIC) package
- Jitter: < 200 ps peak-to-peak, < 25 ps RMS

Functional Description

The CY7B9910 and CY7B9920 low skew clock buffers offer low skew system clock distribution. These multiple output clock drivers optimize the timing of high performance computer systems. Each of the eight individual drivers can drive terminated transmission lines with impedances as low as 50 Ω. They deliver minimal and specified output skews and full swing logic levels (CY7B9910 TTL or CY7B9920 CMOS).

The completely integrated PLL enables ‘zero delay’ capability. External divide capability, combined with the internal PLL, allows distribution of a low frequency clock that is multiplied by virtually any factor at the clock destination. This facility minimizes clock distribution difficulty while allowing maximum system clock speed and flexibility.

Block Diagram Description

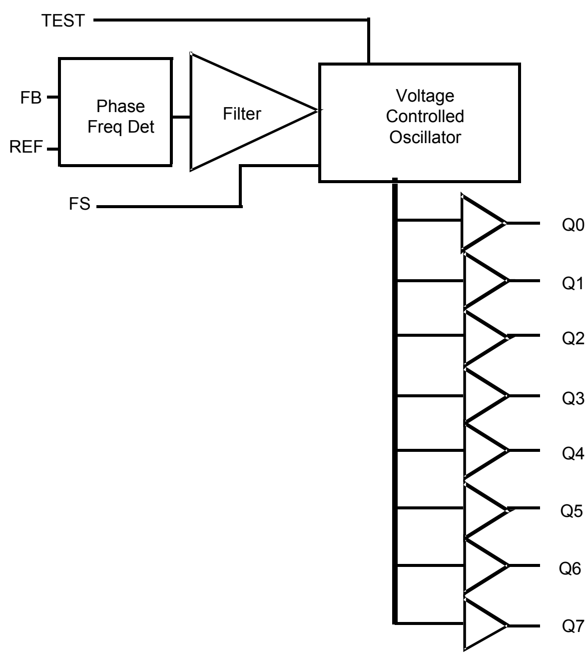
Phase Frequency Detector and Filter

The phase frequency detector and Filter blocks accept inputs from the reference frequency (REF) input and the feedback (FB) input and generate correction information to control the frequency of the voltage controlled oscillator (VCO). These blocks, along with the VCO, form a phase-locked loop (PLL) that tracks the incoming REF signal.

VCO

The VCO accepts analog control inputs from the PLL filter block and generates a frequency. The operational range of the VCO is determined by the FS control pin.

Logic Block Diagram



Contents

Pinouts

Figure 1. Pin Configuration – 24-pin (300-Mil) Molded SOIC

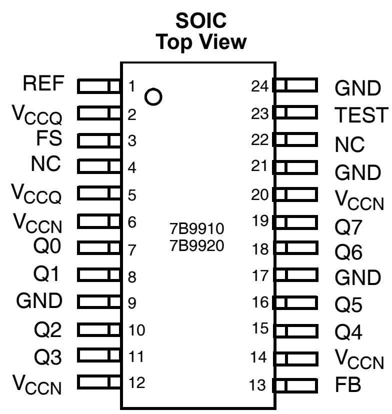


Table 1. Pin Definition

Signal Name	IO	Description
REF[1]	I	Reference frequency input. This input supplies the frequency and timing against which all functional variations are measured.
FB	I	PLL feedback input (typically connected to one of the eight outputs).
FS[1, 2, 3]	I	Three level frequency range select. The ranges are described in the switching characteristics tables.
TEST	I	Three level select. See TEST MODE.
Q[0..7]	O	Clock outputs.
NC	NC	No connect.
V_{CCN}	PWR	Power supply for output drivers.
V_{CCQ}	PWR	Power supply for internal circuitry.
GND	PWR	Ground.

Test Mode

The TEST input is a three level input. In normal system operation, this pin is connected to ground, allowing the CY7B9910 and CY7B9920 to operate as described in Block Diagram Description on page 1. For testing purposes, any of the three level inputs can have a removable jumper to ground or be tied LOW through a 100 Ω resistor. This enables an external tester to change the state of these pins.

If the TEST input is forced to its MID or HIGH state, the device operates with its internal phase locked loop disconnected and input levels supplied to REF directly control all outputs. Relative output-to-output functions are the same as in normal mode.

Notes

1. When the FS pin is selected HIGH, the REF input must not transition upon power up until V_{CC} reached 4.3 V.
2. The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) of the VCO (see Logic Block Diagram). The frequency appearing at the REF and FB inputs are f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs are f_{NOM} / X when the device is configured for a frequency multiplication by using external division in the feedback path of value X.
3. For all three state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to V_{CC} / 2.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ....–65 °C to +150 °C

Ambient temperature with power applied ....–55 °C to +125 °C

Supply voltage to ground potential ....–0.5 V to +7.0 V

DC input voltage ....–0.5 V to +7.0 V

Output current into outputs (LOW) .... 64 mA

Static discharge voltage... > 2001 V (MIL-STD-883, method 3015)

Latch-up current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial	–40 °C to +85 °C	5 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	CY7B9910		CY7B9920		Unit
			Min	Max	Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –16 mA	2.4	–	–	–	V
		V_{CC} = Min, I_{OH} = –40 mA	–	–	V_{CC} – 0.75	–	
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 46 mA	–	0.45	–	–	V
		V_{CC} = Min, I_{OL} = 46 mA	–	–	–	0.45	
V_{IH}	Input HIGH voltage (REF and FB inputs only)		2.0	V_{CC}	V_{CC} – 1.35	V_{CC}	V
V_{IL}	Input LOW voltage (REF and FB inputs only)		–0.5	0.8	–0.5	1.35	V
V_{IHH}	Three level input HIGH voltage (Test, FS)[4]	Min ≤ V_{CC} ≤ Max	V_{CC} – 1 V	V_{CC}	V_{CC} – 1 V	V_{CC}	V
V_{IMM}	Three level input MID voltage (Test, FS)[4]	Min ≤ V_{CC} ≤ Max	V_{CC} / 2 – 500 mV	V_{CC} / 2 + 500 mV	V_{CC} / 2 – 500 mV	V_{CC} / 2 + 500 mV	V
V_{ILL}	Three level input LOW voltage (Test, FS)[4]	Min ≤ V_{CC} ≤ Max	0.0	1.0	0.0	1.0	V
I_{IH}	Input HIGH leakage current (REF and FB inputs only)	V_{CC} = Max, V_{IN} = Max	–	10	–	10	μA
I_{IL}	Input LOW leakage current (REF and FB inputs only)	V_{CC} = Max, V_{IN} = 0.4 V	–500	–	–500	–	μA
I_{IHH}	Input HIGH current (Test, FS)	V_{IN} = V_{CC}	–	200	–	200	μA
I_{IMM}	Input MID current (Test, FS)	V_{IN} = V_{CC} / 2	–50	50	–50	50	μA
I_{ILL}	Input LOW current (Test, FS)	V_{IN} = GND	–	–200	–	–200	μA
I_{OS}	Output short circuit current[5]	V_{CC} = Max, V_{OUT} = GND (25 °C only)	–	–250	–	N/A	mA

Notes

4. These inputs are normally wired to V_{CC}, GND, or left unconnected (actual threshold voltages vary as a percentage of V_{CC}). Internal termination resistors hold unconnected inputs at V_{CC} / 2. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.
5. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle. Room temperature only. CY7B9920 outputs are not short circuit protected.

Electrical Characteristics

Over the Operating Range *(continued)*

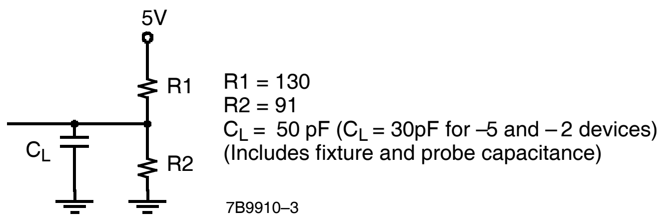
Parameter	Description	Test Conditions		CY7B9910		CY7B9920		Unit
				Min	Max	Min	Max	
I_{CCQ}	Operating current used by internal circuitry	$V_{CCN} = V_{CCQ}$ = Max All input selects open	Commercial	–	85	–	85	mA
			Industrial	–	90	–	90	
I_{CCN}	Output buffer current per output pair[6]	$V_{CCN} = V_{CCQ}$ = Max I_{OUT} = 0 mA Input selects open, f_{MAX}		–	14	–	19	mA
PD	Power dissipation per output pair[7]	$V_{CCN} = V_{CCQ}$ = Max I_{OUT} = 0 mA Input selects open, f_{MAX}		–	78	–	104[8]	mW

Capacitance[9]

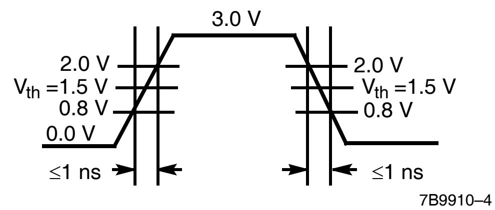
Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	10	pF

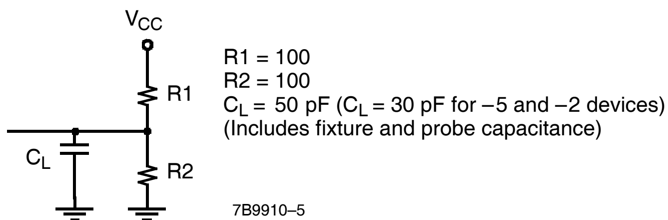
Figure 2. AC Test Loads and Waveforms



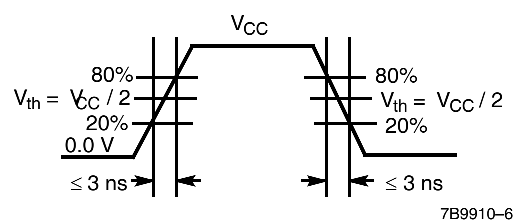
TTL AC Test Load (CY7B9910)



TTL Input Test Waveform (CY7B9910)



CMOS AC Test Load (CY7B9920)



CMOS Input Test Waveform (CY7B9920)

Notes

6. Total output current per output pair is approximated by the following expression that includes device current plus load current:
CY7B9910:
ICCN = [(4 + 0.11 F) + [((835 – 3 F) / Z) + (.0022 FC)] N] x 1.1
CY7B9920:
ICCN = [(3.5 +.17 F) + [((1160 – 2.8 F) / Z) + (.0025 FC)] N] x 1.1
Where
F = frequency in MHz
C = capacitive load in pF
Z = line impedance in ohms
N = number of loaded outputs; 0, 1, or 2
FC = F < C.
7. Total power dissipation per output pair is approximated by the following expression that includes device power dissipation plus power dissipation due to the load circuit:
CY7B9910:
PD = [(22 + 0.61 F) + [((1550 – 2.7 F) / Z) + (.0125 FC)] N] x 1.1
CY7B9920:
PD = [(19.25+ 0.94 F) + [((700 + 6 F) / Z) + (.017 FC)] N] x 1.1.See note 3 for variable definition.
8. CMOS output buffer current and power dissipation specified at 50 MHz reference frequency.
9. Applies to REF and FB inputs only.

Switching Characteristics

Over the Operating Range [10]

Parameter	Description		CY7B9910–2[11]			CY7B9920–2[11]			Unit
			Min	Typ	Max	Min	Typ	Max	
f_{NOM}	Operating clock frequency in MHz	FS = LOW[12, 13]	15	–	30	15	–	30	MHz
		FS = MID[12, 13]	25	–	50	25	–	50	
		FS = HIGH[12, 13, 14]	40	–	80	40	–	80[15]	
t_{RPWH}	REF pulse width HIGH		5.0	–	–	5.0	–	–	ns
t_{RPWL}	REF pulse width LOW		5.0	–	–	5.0	–	–	ns
t_{SKEW}	Zero output skew (all outputs)[16, 17]		–	0.1	0.25	–	0.1	0.25	ns
t_{DEV}	Device-to-device skew[17, 18]		–	–	0.75	–	–	0.75	ns
t_{PD}	Propagation delay, REF rise to FB rise		–0.25	0.0	+0.25	–0.25	0.0	+0.25	ns
t_{ODCV}	Output duty cycle variation[19]		–0.65	0.0	+0.65	–0.65	0.0	+0.65	ns
t_{ORISE}	Output rise time[20, 21]		0.15	1.0	1.2	0.5	2.0	2.5	ns
t_{OFALL}	Output fall time[20, 21]		0.15	1.0	1.2	0.5	2.0	2.5	ns
t_{LOCK}	PLL lock time[22]		–	–	0.5	–	–	0.5	ms
t_{JR}	Cycle-to-cycle output jitter	Peak-to-peak	–	–	200	–	–	200	ps
		RMS	–	–	25	–	–	25	ps

Notes

10. Test measurement levels for the CY7B9910 are TTL levels (1.5 V to 1.5 V). Test measurement levels for the CY7B9920 are CMOS levels (V_{CC} / 2 to V_{CC} / 2). Test conditions assume signal transition times of 2 ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
11. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.
12. For all three state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to V_{CC} / 2.
13. The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) of the VCO (see Logic Block Diagram). The frequency appearing at the REF and FB inputs are f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs are f_{NOM} / X when the device is configured for a frequency multiplication by using external division in the feedback path of value X.
14. When the FS pin is selected HIGH, the REF input must not transition upon power-up until V_{CC} reached 4.3 V.
15. Except as noted, all CY7B9920–2 and –5 timing parameters are specified to 80 MHz with a 30 pF load.
16. t_{SKEW} is defined as the time between the earliest and the latest output transition among all outputs when all are loaded with 50 pF and terminated with 50 Ω to 2.06 V (CY7B9910) or V_{CC} / 2 (CY7B9920).
17. t_{SKEW} is defined as the skew between outputs.
18. t_{DEV} is the output-to-output skew between any two outputs on separate devices operating under the same conditions (V_{CC}, ambient temperature, air flow, and so on).
19. t_{ODCV} is the deviation of the output from a 50% duty cycle.
20. Specified with outputs loaded with 30 pF for the CY7B99X0–2 and –5 devices and 50 pF for the CY7B99X0–7 devices. Devices are terminated through 50 Ω to 2.06 V (CY7B9910) or V_{CC} / 2 (CY7B9920).
21. t_{ORISE} and t_{OFALL} measured between 0.8 V and 2.0 V for the CY7B9910 or 0.8 V_{CC} and 0.2 V_{CC} for the CY7B9920.
22. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

Switching Characteristics

Over the Operating Range [23]

Parameter	Description		CY7B9910–5			CY7B9920–5			Unit
			Min	Typ	Max	Min	Typ	Max	
f_{NOM}	Operating clock frequency in MHz	FS = LOW[24, 25]	15	–	30	15	–	30	MHz
		FS = MID[24, 25]	25	–	50	25	–	50	
		FS = HIGH[24, 25, 26]	40	–	80	40	–	80[27]	
t_{RPWH}	REF pulse width HIGH		5.0	–	–	5.0	–	–	ns
t_{RPWL}	REF pulse width LOW		5.0	–	–	5.0	–	–	ns
t_{SKEW}	Zero output skew (All outputs)[28, 29]		–	0.25	0.5	–	0.25	0.5	ns
t_{DEV}	Device-to-device skew[30, 31]		–	–	1.0	–	–	1.0	ns
t_{PD}	Propagation delay, REF rise to FB rise		–0.5	0.0	+0.5	–0.5	0.0	+0.5	ns
t_{ODCV}	Output duty cycle variation[32]		–1.0	0.0	+1.0	–1.0	0.0	+1.0	ns
t_{ORISE}	Output rise time[33, 34]		0.15	1.0	1.5	0.5	2.0	3.0	ns
t_{OFALL}	Output fall time[33, 34]		0.15	1.0	1.5	0.5	2.0	3.0	ns
t_{LOCK}	PLL lock time[35]		–	–	0.5	–	–	0.5	ms
t_{JR}	Cycle-to-cycle output jitter	Peak-to-peak[30]	–	–	200	–	–	200	ps
		RMS[30]	–	–	25	–	–	25	ps

Notes

23. Test measurement levels for the CY7B9910 are TTL levels (1.5 V to 1.5 V). Test measurement levels for the CY7B9920 are CMOS levels (V_{CC} / 2 to V_{CC} / 2). Test conditions assume signal transition times of 2 ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
24. For all three state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to V_{CC} / 2.
25. The level to be set on FS is determined by the “normal” operating frequency (f_{NOM}) of the VCO (see Logic Block Diagram). The frequency appearing at the REF and FB inputs are f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs are f_{NOM} / X when the device is configured for a frequency multiplication by using external division in the feedback path of value X.
26. When the FS pin is selected HIGH, the REF input must not transition upon power up until V_{CC} reached 4.3 V.
27. Except as noted, all CY7B9920–2 and –5 timing parameters are specified to 80 MHz with a 30 pF load.
28. t_{SKEW} is defined as the time between the earliest and the latest output transition among all outputs when all are loaded with 50 pF and terminated with 50 Ω to 2.06 V (CY7B9910) or V_{CC} / 2 (CY7B9920).
29. t_{SKEW} is defined as the skew between outputs.
30. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.
31. t_{DEV} is the output-to-output skew between any two outputs on separate devices operating under the same conditions (V_{CC}, ambient temperature, air flow, and so on).
32. t_{ODCV} is the deviation of the output from a 50% duty cycle.
33. Specified with outputs loaded with 30 pF for the CY7B99X0–2 and –5 devices and 50 pF for the CY7B99X0–7 devices. Devices are terminated through 50 Ω to 2.06 V (CY7B9910) or V_{CC} / 2 (CY7B9920).
34. t_{ORISE} and t_{OFALL} measured between 0.8 V and 2.0 V for the CY7B9910 or 0.8 V_{CC} and 0.2 V_{CC} for the CY7B9920.
35. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

Switching Characteristics

Over the Operating Range [36]

Parameter	Description		CY7B9910–7			CY7B9920–7			Unit
			Min	Typ	Max	Min	Typ	Max	
f_{NOM}	Operating clock frequency in MHz	FS = LOW[37, 38]	15	–	30	15	–	30	MHz
		FS = MID[37, 38]	25	–	50	25	–	50	
		FS = HIGH[37, 38, 39]	40	–	80	40	–	80[40]	
t_{RPWH}	REF pulse width HIGH		5.0	–	–	5.0	–	–	ns
t_{RPWL}	REF pulse width LOW		5.0	–	–	5.0	–	–	ns
t_{SKEW}	Zero output skew (All outputs)[41, 42]		–	0.3	0.75	–	0.3	0.75	ns
t_{DEV}	Device-to-device skew[43, 44]		–	–	1.5	–	–	1.5	ns
t_{PD}	Propagation delay, REF Rise to FB Rise		–0.7	0.0	+0.7	–0.7	0.0	+0.7	ns
t_{ODCV}	Output duty cycle variation[45]		–1.2	0.0	+1.2	–1.2	0.0	+1.2	ns
t_{ORISE}	Output rise time[46, 47]		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{OFALL}	Output fall time[46, 47]		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{LOCK}	PLL lock time[48]		–	–	0.5	–	–	0.5	ms
t_{JR}	Cycle-to-cycle output jitter	Peak-to-peak[43]	–	–	200	–	–	200	ps
t_{JR}		RMS[43]	–	–	25	–	–	25	ps

Notes

36. Test measurement levels for the CY7B9910 are TTL levels (1.5 V to 1.5 V). Test measurement levels for the CY7B9920 are CMOS levels (V_{CC} / 2 to V_{CC} / 2). Test conditions assume signal transition times of 2 ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
37. For all three state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to V_{CC} / 2.
38. The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) of the VCO (see Logic Block Diagram). The frequency appearing at the REF and FB inputs are f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs are f_{NOM} / X when the device is configured for a frequency multiplication by using external division in the feedback path of value X.
39. When the FS pin is selected HIGH, the REF input must not transition upon power up until V_{CC} reached 4.3 V.
40. Except as noted, all CY7B9920–2 and –5 timing parameters are specified to 80 MHz with a 30 pF load.
41. t_{SKEW} is defined as the time between the earliest and the latest output transition among all outputs when all are loaded with 50 pF and terminated with 50 Ω to 2.06 V (CY7B9910) or V_{CC} / 2 (CY7B9920).
42. t_{SKEW} is defined as the skew between outputs.
43. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.
44. t_{DEV} is the output-to-output skew between any two outputs on separate devices operating under the same conditions (V_{CC}, ambient temperature, air flow, and so on).
45. t_{ODCV} is the deviation of the output from a 50% duty cycle.
46. Specified with outputs loaded with 30 pF for the CY7B99X0–2 and –5 devices and 50 pF for the CY7B99X0–7 devices. Devices are terminated through 50 Ω to 2.06 V (CY7B9910) or V_{CC} / 2 (CY7B9920).
47. t_{ORISE} and t_{OFALL} measured between 0.8 V and 2.0 V for the CY7B9910 or 0.8 V_{CC} and 0.2 V_{CC} for the CY7B9920.
48. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

AC Timing Diagrams

Figure 3. AC Timing Diagrams

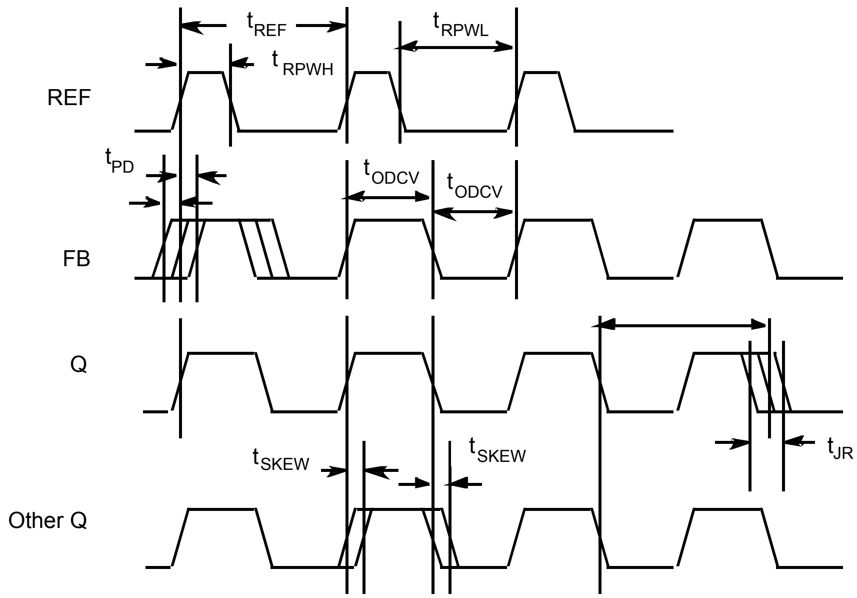
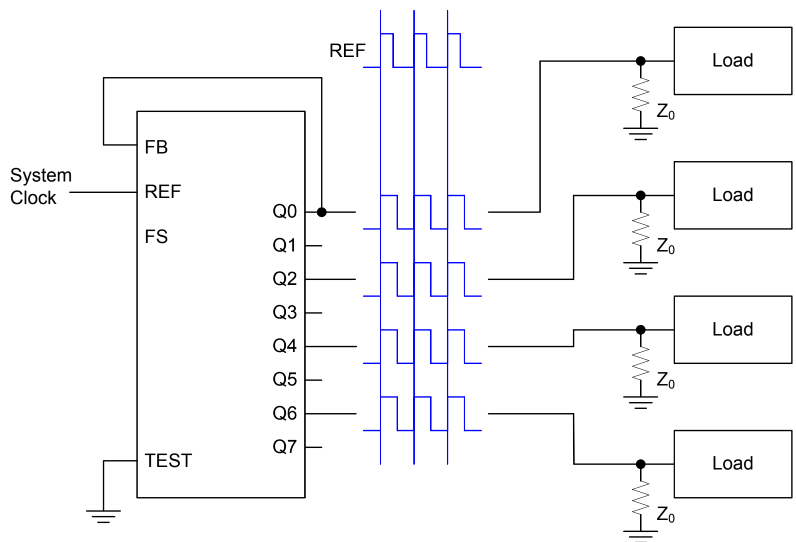


Figure 4. Zero Skew and Zero Delay Clock Driver

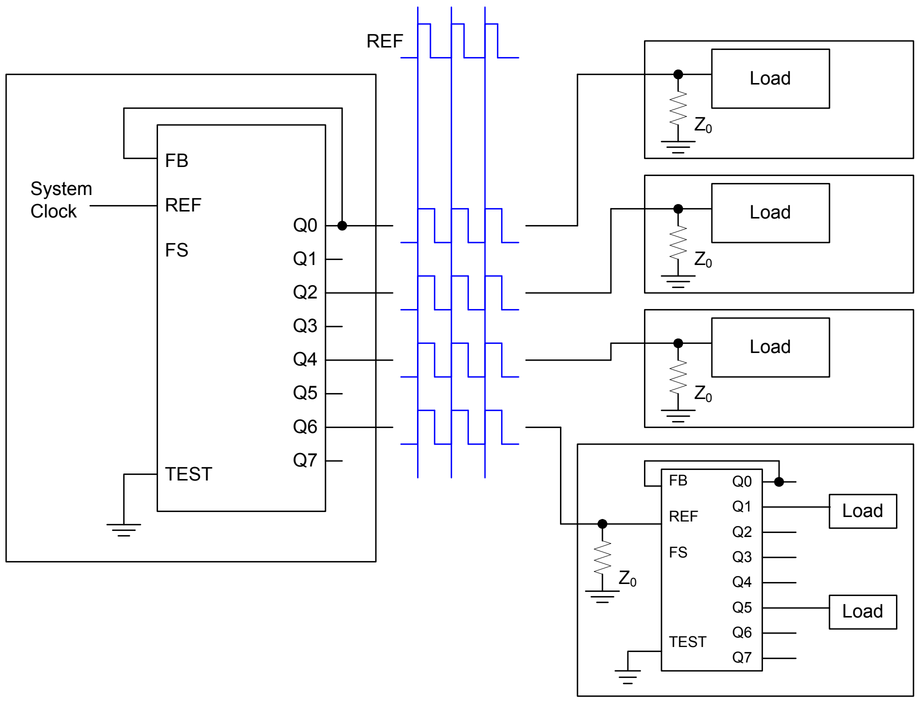


Operational Mode Descriptions

Figure 4 on page 9 shows the device configured as a zero skew clock buffer. In this mode the CY7B9910/CY7B9920 is used as the basis for a low skew clock distribution tree. The outputs are aligned and may each drive a terminated transmission line to an independent load. The FB input is tied to any output and the operating frequency range is selected with the FS pin. The low skew specification, coupled with the ability to drive terminated transmission lines (with impedances as low as 50 ohms), enables efficient printed circuit board design.

Figure 3 on page 9 shows the CY7B9910/CY7B9920 connected in series to construct a zero skew clock distribution tree between boards. Cascaded clock buffers accumulates low frequency jitter because of the non-ideal filtering characteristics of the PLL filter. Do not connect more than two clock buffers in series.

Figure 5. Board-to-Board Clock Distribution



Ordering Information

Accuracy (ps)	Ordering Code	Package Type	Operating Range
500	CY7B9920–5SC[49]	24-Pin Small Outline IC	Commercial, 0 °C to +70 °C
	CY7B9920–5SCT[49]	24-Pin Small Outline IC - Tape and Reel	Commercial, 0 °C to +70 °C
	CY7B9920–5SI[49]	24-Pin Small Outline IC	Industrial, –40 °C to +85 °C
Pb-free			
250	CY7B9910–2SXC	24-Pin Small Outline IC	Commercial, 0 °C to +70 °C
	CY7B9910–2SXCT	24-Pin Small Outline IC - Tape and Reel	Commercial, 0 °C to +70 °C
500	CY7B9910–5SXC	24-Pin Small Outline IC	Commercial, 0 °C to +70 °C
	CY7B9910–5SXCT	24-Pin Small Outline IC - Tape and Reel	Commercial, 0 °C to +70 °C
	CY7B9910–5SXI	24-Pin Small Outline IC	Industrial, –40 °C to +85 °C
	CY7B9910–5SXIT	24-Pin Small Outline IC - Tape and Reel	Industrial, –40 °C to +85 °C
750	CY7B9910–7SXC	24-Pin Small Outline IC	Commercial, 0 °C to +70 °C
	CY7B9910–7SXCT	24-Pin Small Outline IC - Tape and Reel	Commercial, 0 °C to +70 °C

Ordering Code Definition

CY 7B99X0 – X S (X) C (T)

T = Tape and Reel, blank = Tube

Temperature: C = Commercial; I = Industrial

X = Pb-free, blank = not Pb-free

S = SOIC package

Speed grade: 2 / 5 / 7, based on propagation delay

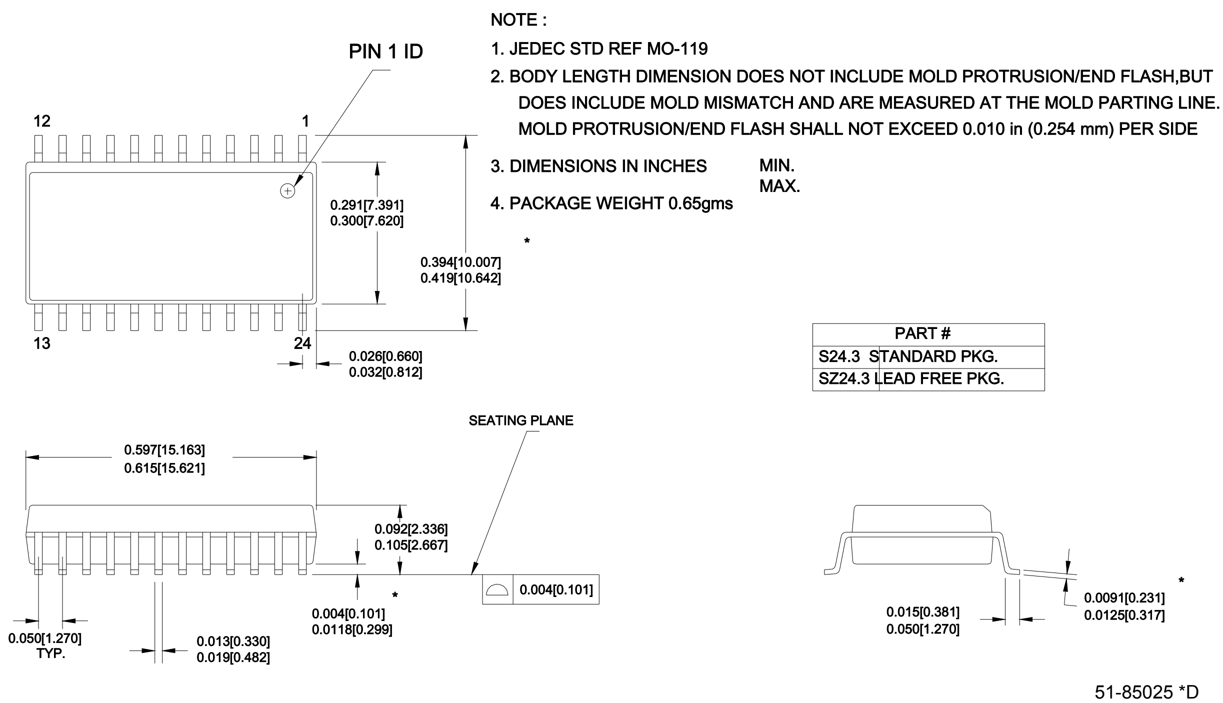
Base part number
7B9910 = Clock buffer with TTL outputs
7B9920 = Clock buffer with CMOS outputs

Company ID: CY = Cypress

Note
49. Not recommended for new design. New designs should use Pb-free devices.

Package Diagram

Figure 6. 24-Pin (300-Mil) Molded SOIC



Acronyms

Acronym	Description
FB	feedback
PLL	phase-locked loop
SOIC	small-outline integrated circuit
VCO	Voltage controlled oscillator

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohms
MHz	megahertz
µA	microamperes
mA	milliamperes
ms	milliseconds
mW	milliwatts
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
ppm	parts per million
ps	picoseconds
V	volts

Document History Page

Document Title: CY7B9910/CY7B9920 Low Skew Clock Buffer Document Number: 38-07135				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110244	SZV	10/28/01	Change from Specification number: 38-00437 to 38-07135
*A	1199925	DPF/AESA	See ECN	Added Pb-free parts in Ordering Information Added Note 20: Not recommended for the new design
*B	1353343	AESA	See ECN	Change status to final
*C	2750166	TSAI	08/10/09	Post to external web
*D	2761988	CXQ	09/10/09	Fixed typo from 100 W resistor to 100 Ω resistor. Added “Not recommended for new designs” note to Pb devices. Fixed incorrect instances of auto-replacement of “lead” to “Pb”.
*E	2896073	CXQ	03/19/10	Removed inactive parts from ordering information table Updated package diagram
*F	3010397	KVM	08/18/2010	Added ordering code definition

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