



## 2M (128K x 16) Static RAM

### Features

- Very high speed: 55 ns and 70 ns
- Voltage range:
  - CY62136CV30: 2.7V–3.3V
  - CY62136CV33: 3.0V–3.6V
  - CY62136CV: 2.7V–3.6V
- Pin-compatible with the CY62136V
- Ultra-low active power
  - Typical active current: 1.5 mA @ f = 1 MHz
  - Typical active current: 5.5 mA @ f = f<sub>max</sub> (70-ns speed)
- Low standby power
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Packages offered in a 48-ball FBGA

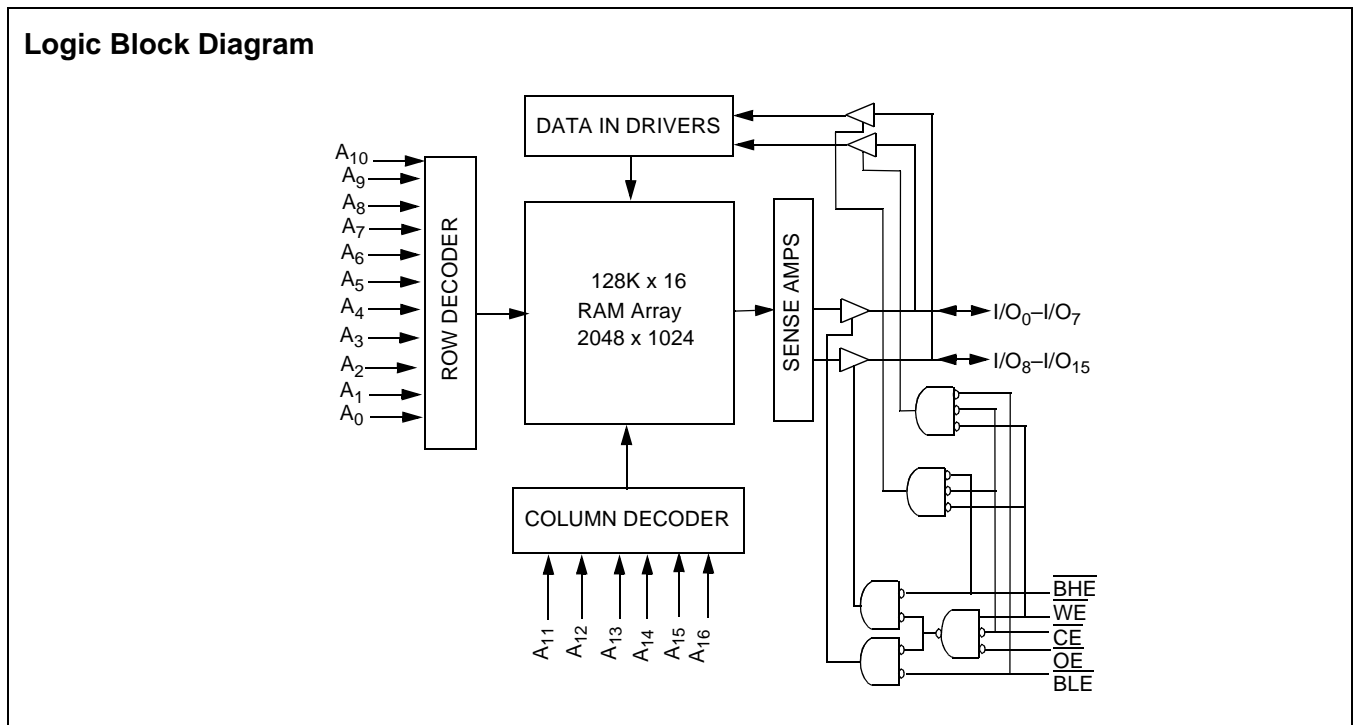
### Functional Description<sup>[1]</sup>

The  $\overline{CE}$  and CY62136CV are high-performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra-low active current.

This is ideal for providing More Battery Life™ (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 80% when addresses are not toggling. The device can also be put into standby mode reducing power consumption by more than 99% when deselected ( $\overline{CE}$  HIGH). The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when: deselected ( $\overline{CE}$  HIGH), outputs are disabled ( $\overline{OE}$  HIGH), both Byte High Enable and Byte Low Enable are disabled ( $\overline{BHE}$ , BLE HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

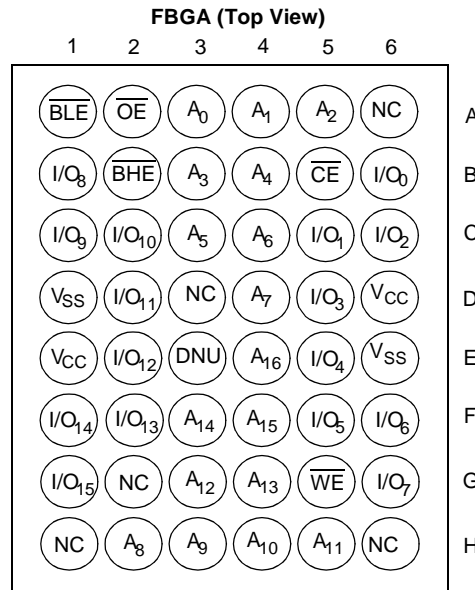
Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the back of this data sheet for a complete description of read and write modes.



**Note:**

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

**Pin Configuration<sup>[2, 3]</sup>**

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential -0.5V to V<sub>CCMAX</sub> + 0.5V

DC Voltage Applied to Outputs in High-Z State<sup>[4]</sup> ..... -0.5V to V<sub>CC</sub> + 0.3V

DC Input Voltage<sup>[4]</sup> ..... -0.5V to V<sub>CC</sub> + 0.3V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

**Operating Range**

| Device      | Range      | Ambient Temperature | V <sub>CC</sub> |
|-------------|------------|---------------------|-----------------|
| CY62136CV30 | Industrial | -40°C to +85°C      | 2.7V to 3.3V    |
| CY62136CV33 |            |                     | 3.0V to 3.6V    |
| CY62136CV   |            |                     | 2.7V to 3.6V    |

**Product Portfolio**

| Product       | V <sub>CC</sub> Range (V) |                                      |                       | Speed (ns) | Power Dissipation               |      |                      |      |                                |      |      |  |
|---------------|---------------------------|--------------------------------------|-----------------------|------------|---------------------------------|------|----------------------|------|--------------------------------|------|------|--|
|               |                           |                                      |                       |            | Operating, I <sub>CC</sub> (mA) |      |                      |      | Standby, I <sub>SB2</sub> (μA) |      |      |  |
|               | V <sub>CC(min.)</sub>     | V <sub>CC(typ.)</sub> <sup>[5]</sup> | V <sub>CC(max.)</sub> |            | f = 1 MHz                       |      | f = f <sub>max</sub> |      | Typ. <sup>[5]</sup>            |      | Max. |  |
|               |                           |                                      |                       |            | Typ. <sup>[5]</sup>             | Max. | Typ. <sup>[5]</sup>  | Max. | Typ. <sup>[5]</sup>            | Max. |      |  |
| CY62136CV30LL | 2.7                       | 3.0                                  | 3.3                   | 55         | 1.5                             | 3    | 7                    | 15   | 2                              | 10   |      |  |
|               |                           |                                      |                       | 70         | 1.5                             | 3    | 5.5                  | 12   |                                |      |      |  |
| CY62136CV33LL | 3.0                       | 3.3                                  | 3.6                   | 55         | 1.5                             | 3    | 7                    | 15   | 5                              | 15   |      |  |
|               |                           |                                      |                       | 70         | 1.5                             | 3    | 5.5                  | 12   |                                |      |      |  |
| CY62136CVLL   | 2.7                       | 3.3                                  | 3.6                   | 70         | 1.5                             | 3    | 5.5                  | 12   | 5                              | 15   |      |  |

**Notes:**

2. NC pins are not connected to the die.
3. E3 (DNU) can be left as NC or V<sub>SS</sub> to ensure proper application.
4. V<sub>IL(min.)</sub> = -2.0V for pulse durations less than 20 ns.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.



**Electrical Characteristics** Over the Operating Range

| Parameter        | Description                                   | Test Conditions                                                                                                                                                               |                                                                  | CY62136CV30-55 |                     |                        | CY62136CV30-70 |                     |                        | Unit |
|------------------|-----------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------|----------------|---------------------|------------------------|----------------|---------------------|------------------------|------|
|                  |                                               |                                                                                                                                                                               |                                                                  | Min.           | Typ. <sup>[5]</sup> | Max.                   | Min.           | Typ. <sup>[5]</sup> | Max.                   |      |
| V <sub>OH</sub>  | Output HIGH Voltage                           | I <sub>OH</sub> = -1.0 mA                                                                                                                                                     | V <sub>CC</sub> = 2.7V                                           |                | 2.4                 |                        |                | 2.4                 |                        | V    |
| V <sub>OL</sub>  | Output LOW Voltage                            | I <sub>OL</sub> = 2.1 mA                                                                                                                                                      | V <sub>CC</sub> = 2.7V                                           |                |                     |                        | 0.4            |                     | 0.4                    | V    |
| V <sub>IH</sub>  | Input HIGH Voltage                            |                                                                                                                                                                               |                                                                  | 2.2            |                     | V <sub>CC</sub> + 0.3V | 2.2            |                     | V <sub>CC</sub> + 0.3V | V    |
| V <sub>IL</sub>  | Input LOW Voltage                             |                                                                                                                                                                               |                                                                  | -0.3           |                     | 0.8                    | -0.3           |                     | 0.8                    | V    |
| I <sub>IX</sub>  | Input Leakage Current                         | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                                                                                                                                        |                                                                  | -1             |                     | +1                     | -1             |                     | +1                     | μA   |
| I <sub>OZ</sub>  | Output Leakage Current                        | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled                                                                                                                      |                                                                  | -1             |                     | +1                     | -1             |                     | +1                     | μA   |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current      | f = f <sub>MAX</sub> = 1/t <sub>RC</sub>                                                                                                                                      | V <sub>CC</sub> = 3.3V<br>I <sub>OUT</sub> = 0 mA<br>CMOS Levels |                | 7                   | 15                     |                | 5.5                 | 12                     | mA   |
|                  |                                               | f = 1 MHz                                                                                                                                                                     |                                                                  |                | 1.5                 | 3                      |                | 1.5                 | 3                      |      |
| I <sub>SB1</sub> | Automatic CE Power-down Current — CMOS Inputs | CE ≥ V <sub>CC</sub> - 0.2V<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = f <sub>max</sub> (Address and Data Only), f = 0 (OE, WE, BHE, and BLE) |                                                                  |                | 2                   | 10                     |                | 2                   | 10                     | μA   |
| I <sub>SB2</sub> | Automatic CE Power-down Current — CMOS Inputs | CE ≥ V <sub>CC</sub> - 0.2V<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.3V                                              |                                                                  |                |                     |                        |                |                     |                        |      |

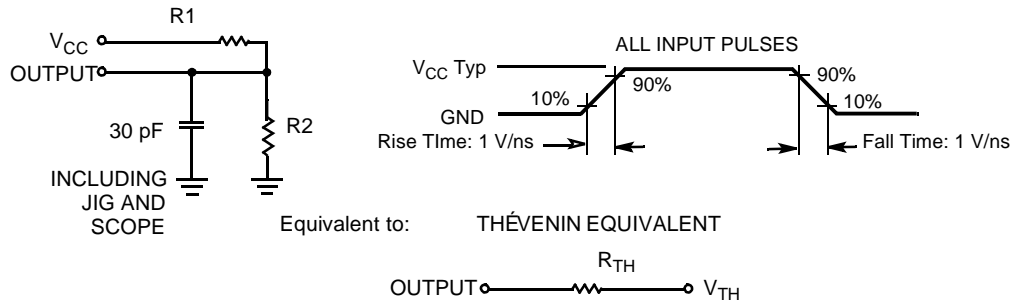
| Parameter        | Description                                   | Test Conditions                                                                                                                                                               |                                                                  | CY62136CV33-55 |                     |                        | CY62136CV33-70<br>CY62136CV-70 |                     |                        | Unit |
|------------------|-----------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------|----------------|---------------------|------------------------|--------------------------------|---------------------|------------------------|------|
|                  |                                               |                                                                                                                                                                               |                                                                  | Min.           | Typ. <sup>[5]</sup> | Max.                   | Min.                           | Typ. <sup>[5]</sup> | Max.                   |      |
| V <sub>OH</sub>  | Output HIGH Voltage                           | I <sub>OH</sub> = -1.0 mA                                                                                                                                                     | V <sub>CC</sub> = 3.0V                                           | 2.4            |                     |                        | 2.4                            |                     |                        | V    |
|                  |                                               |                                                                                                                                                                               | V <sub>CC</sub> = 2.7V                                           |                |                     |                        | 2.4                            |                     |                        | V    |
| V <sub>OL</sub>  | Output LOW Voltage                            | I <sub>OL</sub> = 2.1 mA                                                                                                                                                      | V <sub>CC</sub> = 3.0V                                           |                |                     | 0.4                    |                                |                     | 0.4                    | V    |
|                  |                                               |                                                                                                                                                                               | V <sub>CC</sub> = 2.7V                                           |                |                     |                        |                                |                     | 0.4                    | V    |
| V <sub>IH</sub>  | Input HIGH Voltage                            |                                                                                                                                                                               |                                                                  | 2.2            |                     | V <sub>CC</sub> + 0.3V | 2.2                            |                     | V <sub>CC</sub> + 0.3V | V    |
| V <sub>IL</sub>  | Input LOW Voltage                             |                                                                                                                                                                               |                                                                  | -0.3           |                     | 0.8                    | -0.3                           |                     | 0.8                    | V    |
| I <sub>IX</sub>  | Input Leakage Current                         | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                                                                                                                                        |                                                                  | -1             |                     | +1                     | -1                             |                     | +1                     | μA   |
| I <sub>OZ</sub>  | Output Leakage Current                        | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled                                                                                                                      |                                                                  | -1             |                     | +1                     | -1                             |                     | +1                     | μA   |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current      | f = f <sub>MAX</sub> = 1/t <sub>RC</sub>                                                                                                                                      | V <sub>CC</sub> = 3.6V<br>I <sub>OUT</sub> = 0 mA<br>CMOS Levels |                | 7                   | 15                     |                                | 5.5                 | 12                     | mA   |
|                  |                                               | f = 1 MHz                                                                                                                                                                     |                                                                  |                | 1.5                 | 3                      |                                | 1.5                 | 3                      |      |
| I <sub>SB1</sub> | Automatic CE Power-down Current — CMOS Inputs | CE ≥ V <sub>CC</sub> - 0.2V<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = f <sub>max</sub> (Address and Data Only), f = 0 (OE, WE, BHE, and BLE) |                                                                  |                | 5                   | 15                     |                                | 5                   | 15                     | μA   |
| I <sub>SB2</sub> | Automatic CE Power-down Current — CMOS Inputs | CE ≥ V <sub>CC</sub> - 0.2V<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.6V                                              |                                                                  |                |                     |                        |                                |                     |                        |      |

**Capacitance<sup>[6]</sup>**

| Parameter        | Description        | Test Conditions                                                               | Max. | Unit |
|------------------|--------------------|-------------------------------------------------------------------------------|------|------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = V <sub>CC</sub> (typ.) | 6    | pF   |
| C <sub>OUT</sub> | Output Capacitance |                                                                               | 8    | pF   |

**Thermal Resistance**

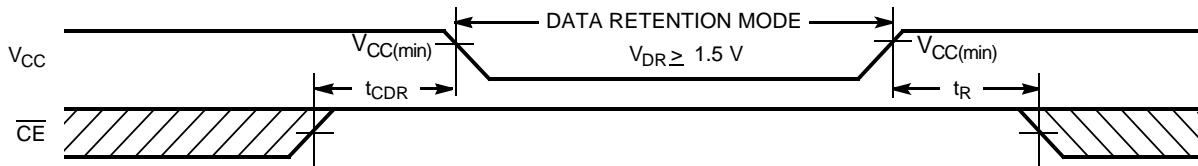
| Parameter     | Description                                             | Test Conditions                                                        | BGA | Unit |
|---------------|---------------------------------------------------------|------------------------------------------------------------------------|-----|------|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) <sup>[6]</sup> | Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board | 55  | °C/W |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case) <sup>[6]</sup>    |                                                                        | 16  | °C/W |

**AC Test Loads and Waveforms**


| Parameters | 3.0V | 3.3V | Unit     |
|------------|------|------|----------|
| R1         | 1105 | 1216 | $\Omega$ |
| R2         | 1550 | 1374 | $\Omega$ |
| $R_{TH}$   | 645  | 645  | $\Omega$ |
| $V_{TH}$   | 1.75 | 1.75 | V        |

**Data Retention Characteristics (Over the Operating Range)**

| Parameter       | Description                          | Conditions                                                                                                | Min.     | Typ. <sup>[5]</sup> | Max.        | Unit    |
|-----------------|--------------------------------------|-----------------------------------------------------------------------------------------------------------|----------|---------------------|-------------|---------|
| $V_{DR}$        | $V_{CC}$ for Data Retention          |                                                                                                           | 1.5      |                     | $V_{CCmax}$ | V       |
| $I_{CCDR}$      | Data Retention Current               | $V_{CC} = 1.5V$ $\overline{CE} \geq V_{CC} - 0.2V$ ,<br>$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ |          | 1                   | 6           | $\mu A$ |
| $t_{CDR}^{[6]}$ | Chip Deselect to Data Retention Time |                                                                                                           | 0        |                     |             | ns      |
| $t_R^{[7]}$     | Operation Recovery Time              |                                                                                                           | $t_{RC}$ |                     |             | ns      |

**Data Retention Waveform**

**Notes:**

- Tested initially and after any design or process changes that may affect these parameters.
- Full Device AC operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} > 100 \mu s$  or stable at  $V_{CC(min.)} > 100 \mu s$ .

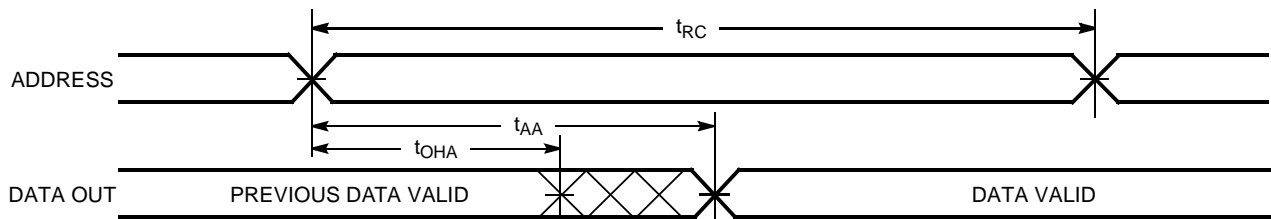


**Switching Characteristics** Over the Operating Range<sup>[8]</sup>

| Parameter                         | Description                                           | 55 ns |      | 70 ns |      | Unit |
|-----------------------------------|-------------------------------------------------------|-------|------|-------|------|------|
|                                   |                                                       | Min.  | Max. | Min.  | Max. |      |
| <b>Read Cycle</b>                 |                                                       |       |      |       |      |      |
| t <sub>RC</sub>                   | Read Cycle Time                                       | 55    |      | 70    |      | ns   |
| t <sub>AA</sub>                   | Address to Data Valid                                 |       | 55   |       | 70   | ns   |
| t <sub>OHA</sub>                  | Data Hold from Address Change                         | 10    |      | 10    |      | ns   |
| t <sub>ACE</sub>                  | CE LOW to Data Valid                                  |       | 55   |       | 70   | ns   |
| t <sub>DOE</sub>                  | OE LOW to Data Valid                                  |       | 25   |       | 35   | ns   |
| t <sub>LZOE</sub>                 | OE LOW to Low-Z <sup>[9]</sup>                        | 5     |      | 5     |      | ns   |
| t <sub>HZOE</sub>                 | OE HIGH to High-Z <sup>[9, 10]</sup>                  |       | 20   |       | 25   | ns   |
| t <sub>LZCE</sub>                 | CE LOW to Low-Z <sup>[9]</sup>                        | 10    |      | 10    |      | ns   |
| t <sub>HZCE</sub>                 | CE HIGH to High-Z <sup>[9, 10]</sup>                  |       | 20   |       | 25   | ns   |
| t <sub>PU</sub>                   | CE LOW to Power-up                                    | 0     |      | 0     |      | ns   |
| t <sub>PD</sub>                   | CE HIGH to Power-down                                 |       | 55   |       | 70   | ns   |
| t <sub>DBE</sub>                  | BHE/BL <sub>E</sub> LOW to Data Valid                 |       | 25   |       | 35   | ns   |
| t <sub>LZBE</sub>                 | BHE/BL <sub>E</sub> LOW to Low-Z <sup>[9]</sup>       | 5     |      | 5     |      | ns   |
| t <sub>HZBE</sub>                 | BHE/BL <sub>E</sub> HIGH to High-Z <sup>[9, 10]</sup> |       | 20   |       | 25   | ns   |
| <b>Write Cycle<sup>[11]</sup></b> |                                                       |       |      |       |      |      |
| t <sub>WC</sub>                   | Write Cycle Time                                      | 55    |      | 70    |      | ns   |
| t <sub>SCE</sub>                  | CE LOW to Write End                                   | 45    |      | 60    |      | ns   |
| t <sub>AW</sub>                   | Address Set-up to Write End                           | 45    |      | 60    |      | ns   |
| t <sub>HA</sub>                   | Address Hold from Write End                           | 0     |      | 0     |      | ns   |
| t <sub>SA</sub>                   | Address Set-up to Write Start                         | 0     |      | 0     |      | ns   |
| t <sub>PWE</sub>                  | WE Pulse Width                                        | 40    |      | 45    |      | ns   |
| t <sub>BW</sub>                   | BHE/BL <sub>E</sub> Pulse Width                       | 50    |      | 60    |      | ns   |
| t <sub>SD</sub>                   | Data Set-up to Write End                              | 25    |      | 30    |      | ns   |
| t <sub>HD</sub>                   | Data Hold from Write End                              | 0     |      | 0     |      | ns   |
| t <sub>HZWE</sub>                 | WE LOW to High-Z <sup>[9, 10]</sup>                   |       | 20   |       | 25   | ns   |
| t <sub>LZWE</sub>                 | WE HIGH to Low-Z <sup>[9]</sup>                       | 10    |      | 10    |      | ns   |

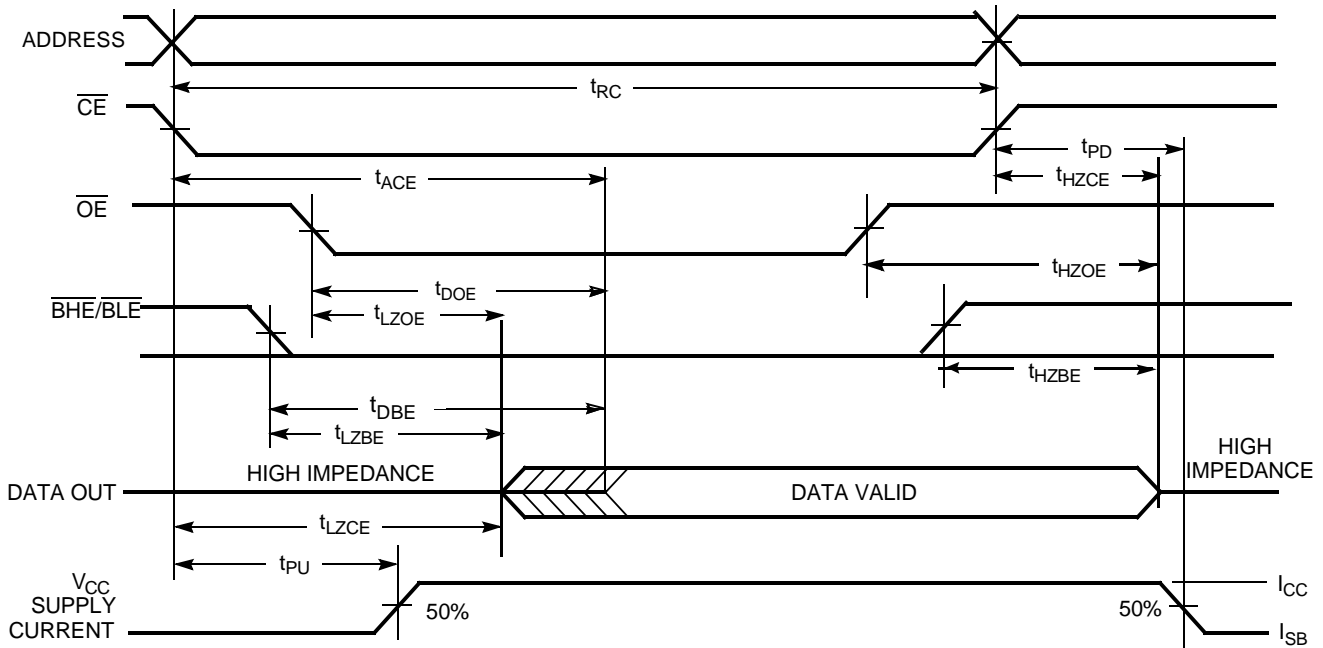
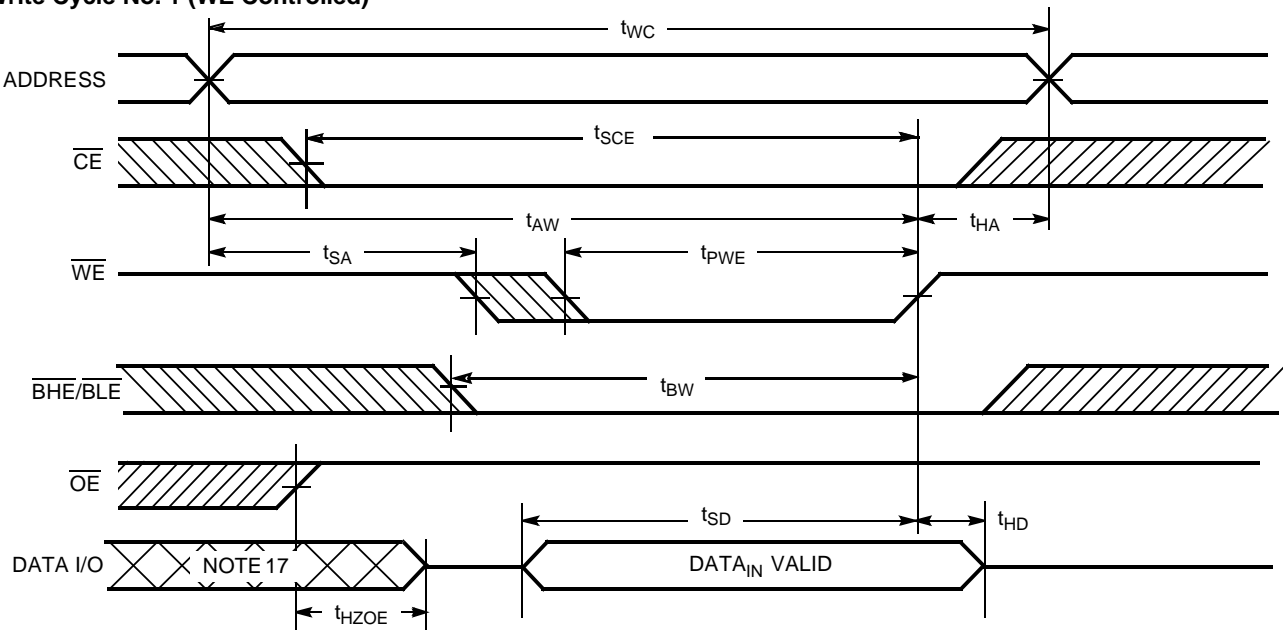
**Switching Waveforms**

**Read Cycle No. 1 (Address Transition Controlled)<sup>[12, 13]</sup>**

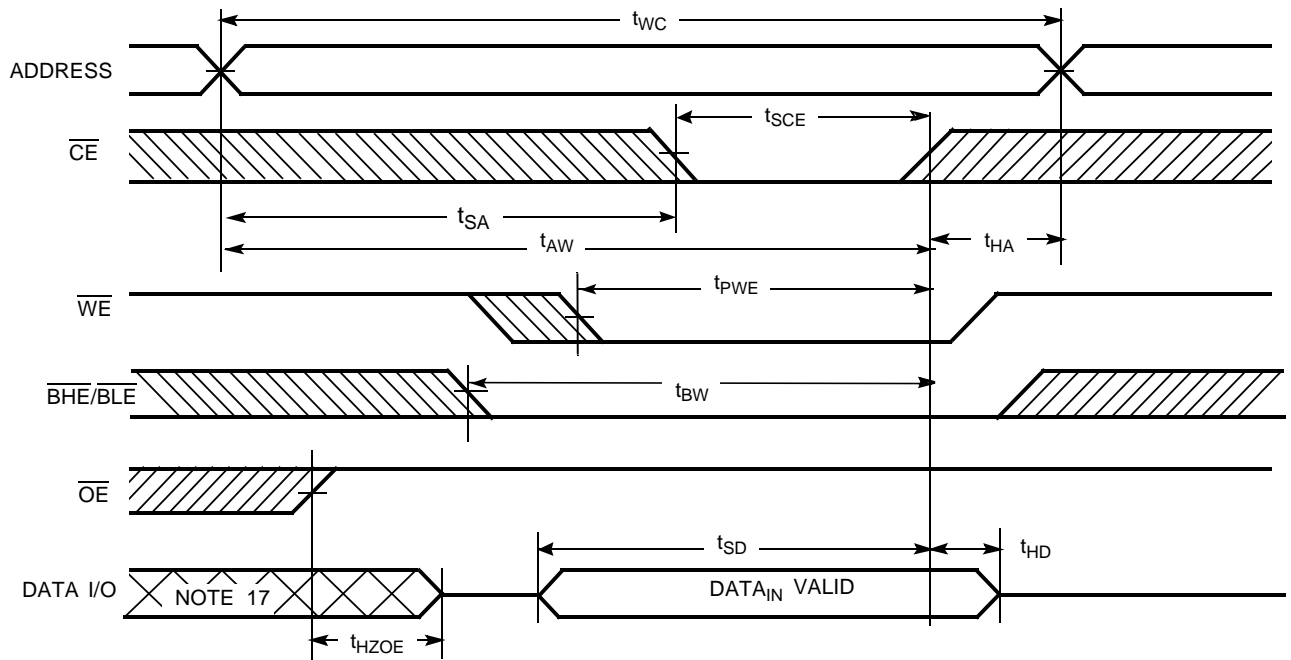
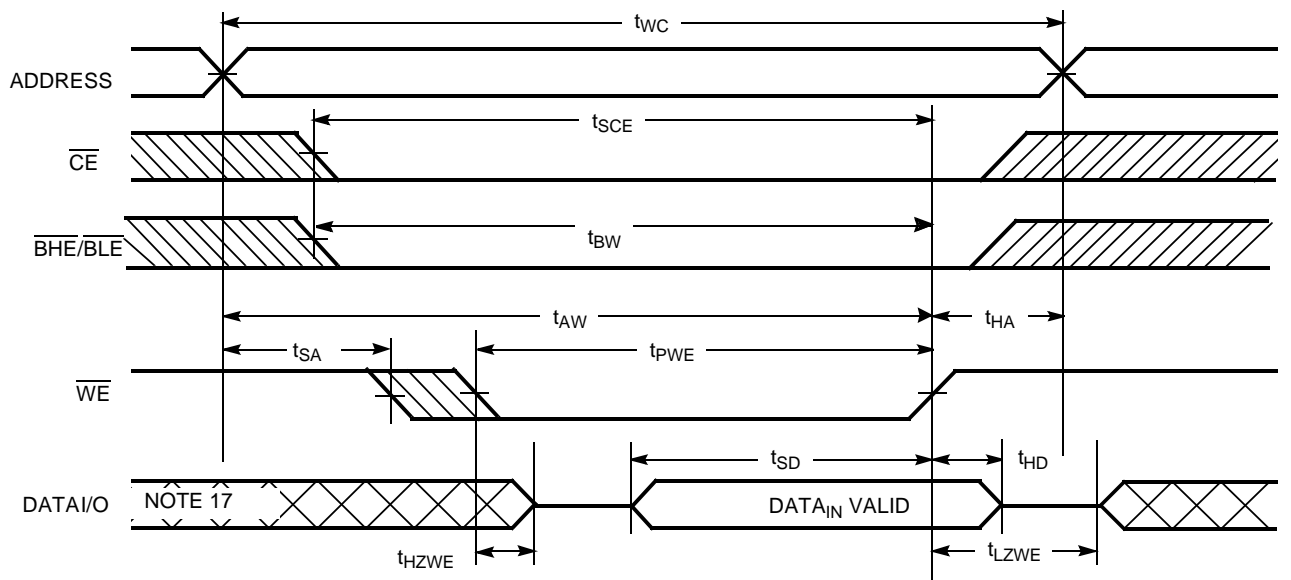


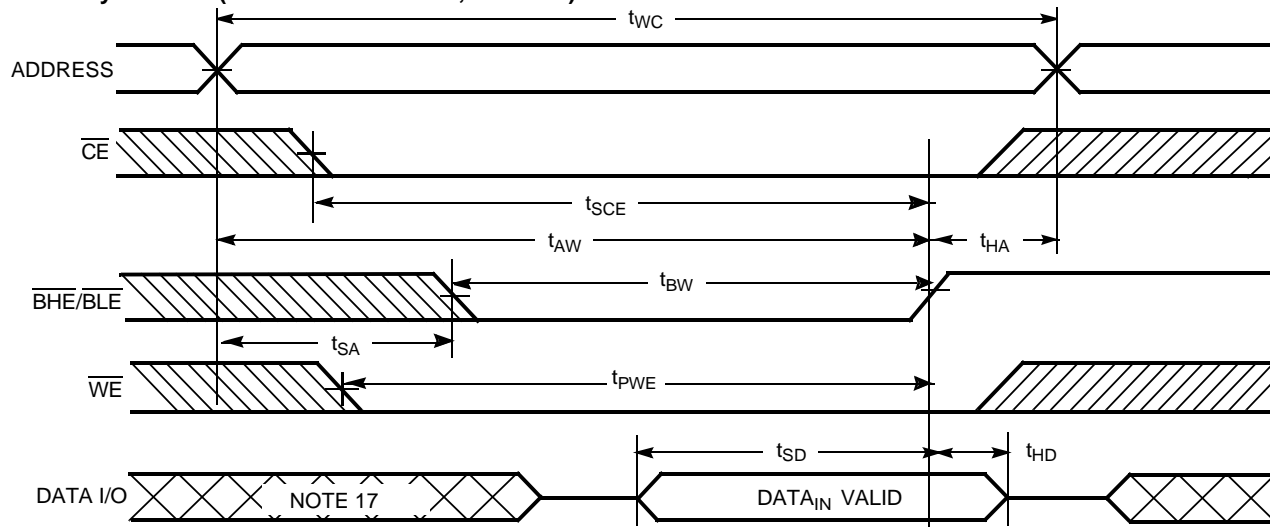
**Notes:**

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of  $V_{CC(typ.)}/2$ , input pulse levels of 0 to  $V_{CC(typ.)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high-impedance state.
- The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
- Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE} = V_{IL}$ .
- $\overline{WE}$  is HIGH for read cycle.

**Switching Waveforms (continued)**
**Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [13, 14]

**Write Cycle No. 1 ( $\overline{WE}$  Controlled)** [11, 15, 16]

**Notes:**

14. Address valid prior to or coincident with  $\overline{CE}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW.
15. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
16. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.

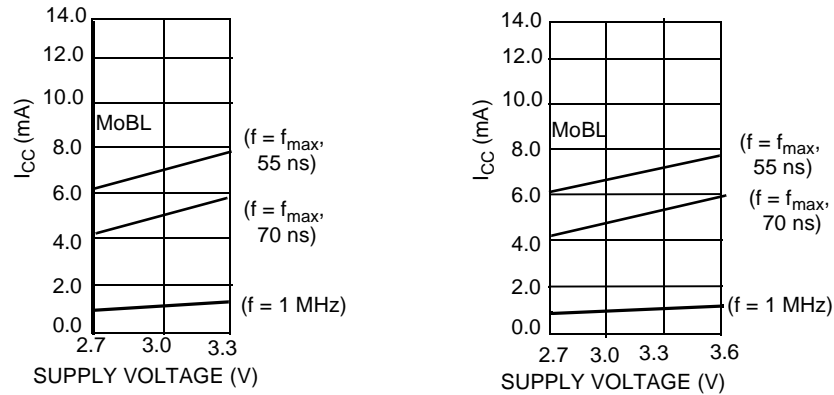
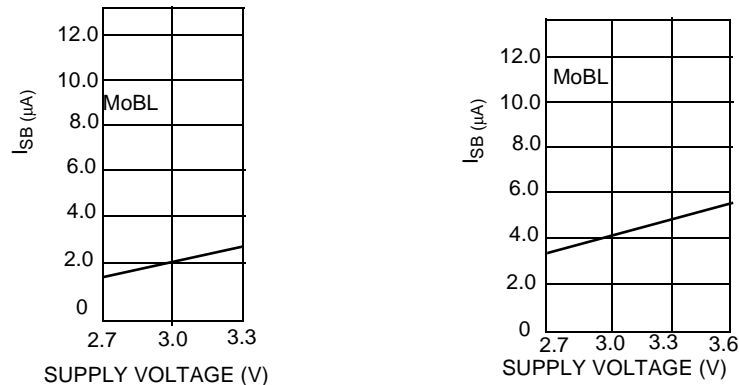
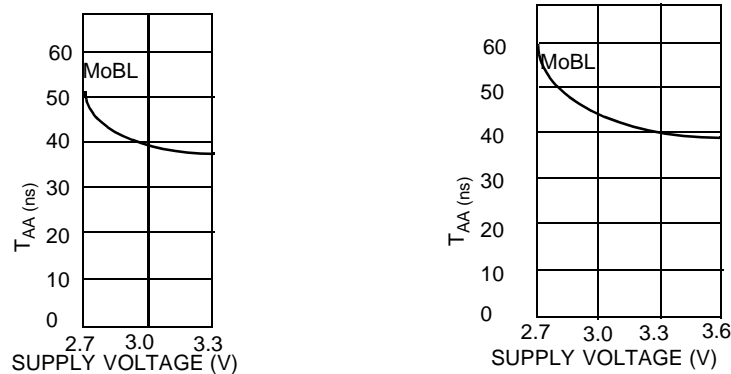
**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{CE}$  Controlled) [11, 15, 16]**

**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [16]**


**Switching Waveforms (continued)**
**Write Cycle No. 4 ( $\overline{\text{BHE}}/\overline{\text{BLE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[16]</sup>**




**Typical DC and AC Parameters**

(Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ.)}$ ,  $T_A = 25^\circ\text{C}$ )

**Operating Current vs. Supply Voltage**

**Standby Current vs. Supply Voltage**

**Access Time vs. Supply Voltage**

**Truth Table**

| $\overline{\text{CE}}$ | $\overline{\text{WE}}$ | $\overline{\text{OE}}$ | $\overline{\text{BHE}}$ | $\overline{\text{BLE}}$ | Inputs/Outputs                                                    | Mode                | Power                |
|------------------------|------------------------|------------------------|-------------------------|-------------------------|-------------------------------------------------------------------|---------------------|----------------------|
| H                      | X                      | X                      | X                       | X                       | High-Z                                                            | Deselect/Power-down | Standby ( $I_{SB}$ ) |
| L                      | X                      | X                      | H                       | H                       | High-Z                                                            | Output Disabled     | Active ( $I_{CC}$ )  |
| L                      | H                      | L                      | L                       | L                       | Data Out ( $I/O_0$ – $I/O_{15}$ )                                 | Read                | Active ( $I_{CC}$ )  |
| L                      | H                      | L                      | H                       | L                       | Data Out ( $I/O_0$ – $I/O_7$ );<br>$I/O_8$ – $I/O_{15}$ in High-Z | Read                | Active ( $I_{CC}$ )  |
| L                      | H                      | L                      | L                       | H                       | Data Out ( $I/O_8$ – $I/O_{15}$ );<br>$I/O_0$ – $I/O_7$ in High-Z | Read                | Active ( $I_{CC}$ )  |
| L                      | H                      | H                      | L                       | L                       | High-Z                                                            | Output Disabled     | Active ( $I_{CC}$ )  |



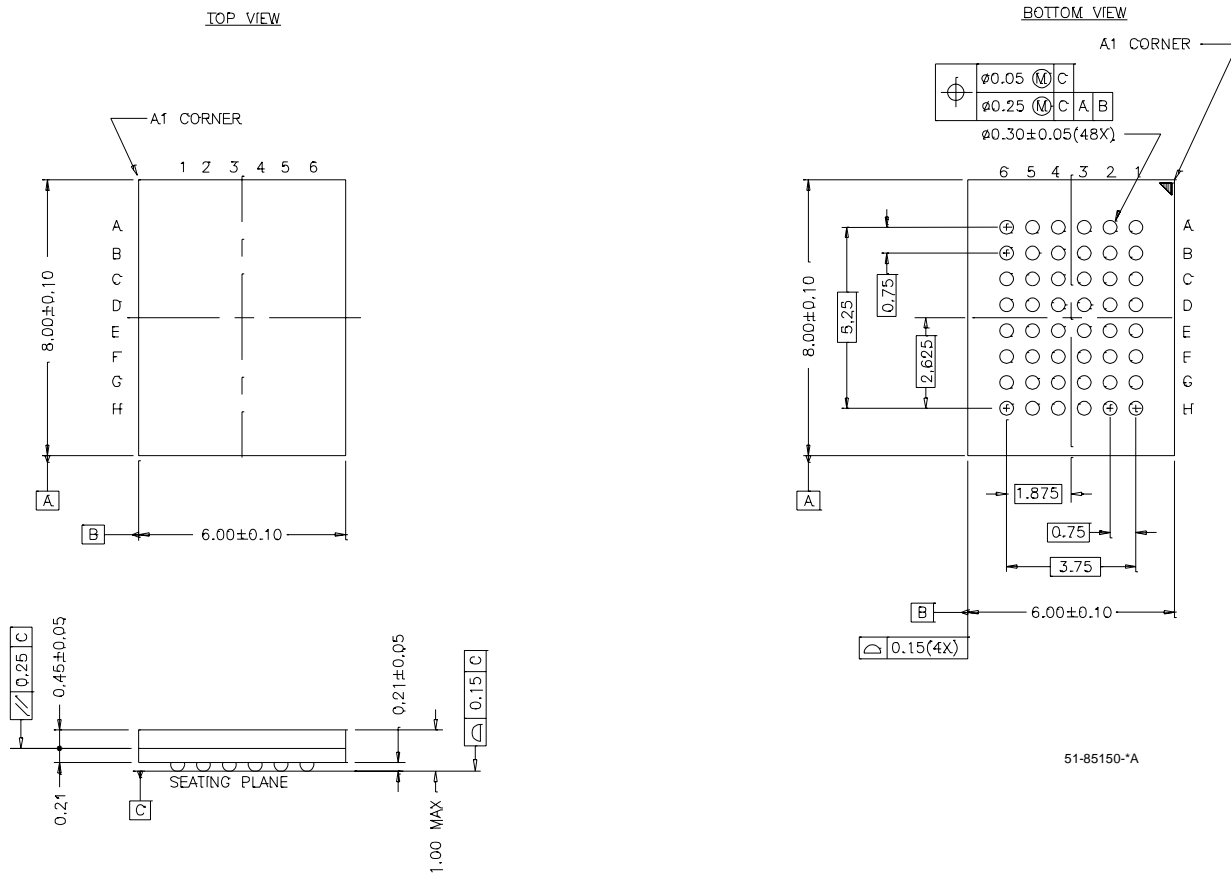
**Truth Table** (continued)

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs/Outputs                                                   | Mode            | Power               |
|-----------------|-----------------|-----------------|------------------|------------------|------------------------------------------------------------------|-----------------|---------------------|
| L               | H               | H               | H                | L                | High-Z                                                           | Output Disabled | Active ( $I_{CC}$ ) |
| L               | H               | H               | L                | H                | High-Z                                                           | Output Disabled | Active ( $I_{CC}$ ) |
| L               | L               | X               | L                | L                | Data In ( $I/O_0$ – $I/O_{15}$ )                                 | Write           | Active ( $I_{CC}$ ) |
| L               | L               | X               | H                | L                | Data In ( $I/O_0$ – $I/O_7$ );<br>$I/O_8$ – $I/O_{15}$ in High-Z | Write           | Active ( $I_{CC}$ ) |
| L               | L               | X               | L                | H                | Data In ( $I/O_8$ – $I/O_{15}$ );<br>$I/O_0$ – $I/O_7$ in High-Z | Write           | Active ( $I_{CC}$ ) |

**Ordering Information**

| Speed (ns) | Ordering Code       | Voltage Range (V) | Package Name | Package Type                                  | Operating Range |
|------------|---------------------|-------------------|--------------|-----------------------------------------------|-----------------|
| 70         | CY62136CV30LL-70BAI | 2.7–3.3           | BA48A        | 48-ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm) | Industrial      |
|            | CY62136CV30LL-70BVI | 2.7–3.3           | BV48A        | 48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)   |                 |
|            | CY62136CV33LL-70BAI | 3.0–3.6           | BA48A        | 48-ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm) |                 |
|            | CY62136CV33LL-70BVI | 3.0–3.6           | BV48A        | 48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)   |                 |
|            | CY62136CVLL-70BAI   | 2.7–3.6           | BA48A        | 48-ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm) |                 |
|            | CY62136CVLL-70BVI   | 2.7–3.6           | BV48A        | 48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)   |                 |
| 55         | CY62136CV30LL-55BAI | 2.7–3.3           | BA48A        | 48-ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm) |                 |
|            | CY62136CV30LL-55BVI | 2.7–3.3           | BV48A        | 48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)   |                 |
|            | CY62136CV33LL-55BAI | 3.0–3.6           | BA48A        | 48-ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm) |                 |
|            | CY62136CV33LL-55BVI | 3.0–3.6           | BV48A        | 48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)   |                 |



**Package Diagrams (continued)**
**48-ball VFBGA (6 x 8 x 1 mm) BV48A**


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## Document History Page

| Document Title: CY62136CV30/33/CY62136CV/CY62136CV30/33 2M (128K x 16) Static RAM |         |            |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----------------------------------------------------------------------------------|---------|------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Document Number: 38-05199                                                         |         |            |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| REV.                                                                              | ECN NO. | Issue Date | Orig. of Change | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| **                                                                                | 112379  | 02/19/02   | GAV             | New Data Sheet (advance information)                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| *A                                                                                | 114023  | 04/25/02   | JUI             | Added BV package diagram<br>Changed Advance Information to Preliminary                                                                                                                                                                                                                                                                                                                                                                                                |
| *B                                                                                | 117063  | 07/12/02   | MGN             | Changed Preliminary to Final                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| *C                                                                                | 118121  | 08/26/02   | MGN             | Added new part numbers: CY62136CV with wider voltage (2.7V – 3.6V);<br>CY62136CV33 narrower voltage range (3.0V – 3.6V)<br>For T <sub>AA</sub> = 55 ns, improved t <sub>PWE</sub> Min from 45 ns to 40 ns<br>For T <sub>AA</sub> = 70 ns, improved t <sub>PWE</sub> Min from 50 ns to 45 ns<br>For T <sub>AA</sub> = 70 ns, improved t <sub>LZWE</sub> Min from 5 ns to 10 ns                                                                                         |
| *D                                                                                | 118622  | 10/3/02    | MGN             | Improved Typ. I <sub>CC</sub> spec. to 7 mA (for 55 ns) and 5.5 mA (for 70 ns)<br>Improved Max I <sub>CC</sub> spec. to 15 mA (for 55 ns) and 12 mA (for 70 ns)<br>For T <sub>AA</sub> = 55 ns, improved t <sub>LZWE</sub> min. from 5 ns to 10 ns<br>Changed upper spec. for Supply Voltage to Ground Potential to V <sub>CCMAX</sub> + 0.5V<br>Changed upper spec. for DC Voltage Applied to Outputs in High-Z State and DC Input Voltage to V <sub>CC</sub> + 0.3V |