

512K x 16 Static RAM

Features

- **Temperature Ranges**
 - Commercial: 0°C to 70°C
 - Industrial: -40°C to 85°C
 - Automotive: -40°C to 125°C
- **High speed**
 - 55 ns and 70 ns availability
- **Voltage range:**
 - CY62157CV25: 2.2V–2.7V
 - CY62157CV30: 2.7V–3.3V
 - CY62157CV33: 3.0V–3.6V
- **Ultra-low active power**
 - Typical active current: 1.5 mA @ f = 1 MHz
 - Typical active current: 5.5 mA @ f = f_{max} (70 ns speed)
- **Low standby power**
- **Easy memory expansion with \overline{CE}_1 , \overline{CE}_2 and \overline{OE} features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

Functional Description^[1]

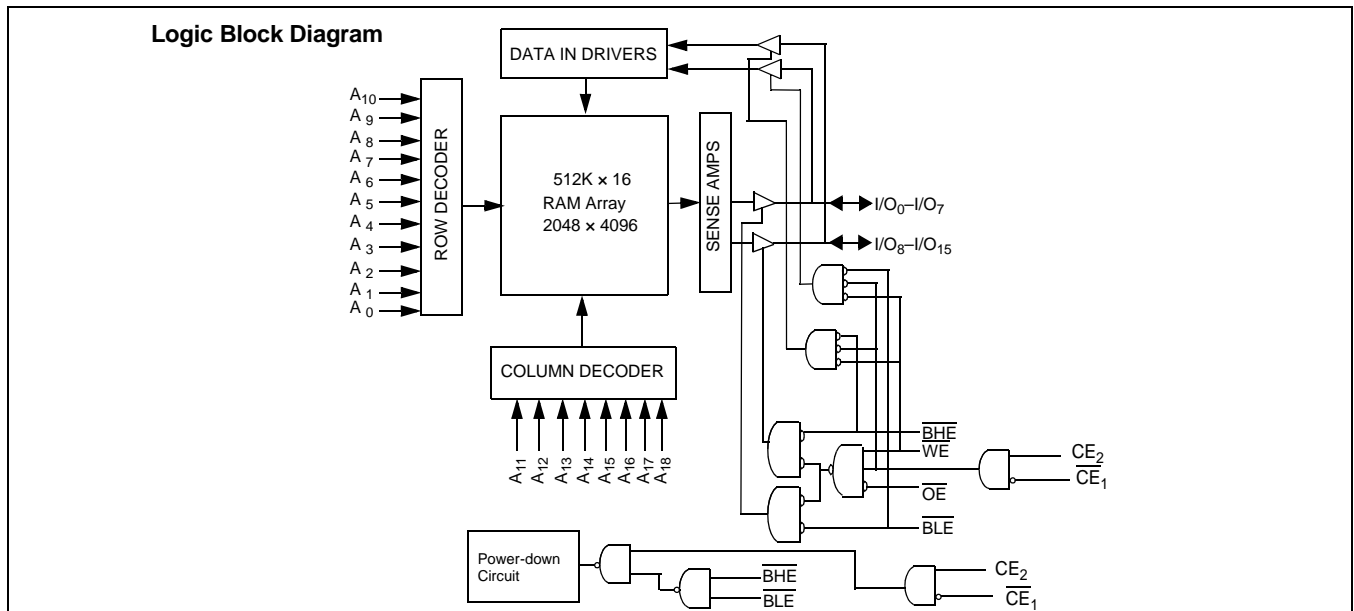
The CY62157CV25/30/33 are high-performance CMOS static RAMs organized as 512K words by 16 bits. These devices feature advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™

(MoBL™) in portable applications such as cellular telephones. The devices also have an automatic power-down feature that significantly reduces power consumption by 80% when addresses are not toggling. The device can also be put into standby mode reducing power consumption by more than 99% when deselected (\overline{CE}_1 HIGH or \overline{CE}_2 LOW or both BLE and BHE are HIGH). The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when: deselected (\overline{CE}_1 HIGH or \overline{CE}_2 LOW), outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , BLE HIGH), or during a write operation (\overline{CE}_1 LOW and \overline{CE}_2 HIGH and WE LOW).

Writing to the device is accomplished by taking Chip Enable 1 (\overline{CE}_1) and Write Enable (WE) inputs LOW and Chip Enable 2 (\overline{CE}_2) HIGH. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₈). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₈).

Reading from the device is accomplished by taking Chip Enable 1 (\overline{CE}_1) and Output Enable (\overline{OE}) LOW and Chip Enable 2 (\overline{CE}_2) HIGH while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the truth table at the back of this data sheet for a complete description of read and write modes.

The CY62157CV25/30/33 are available in a 48-ball FBGA package.

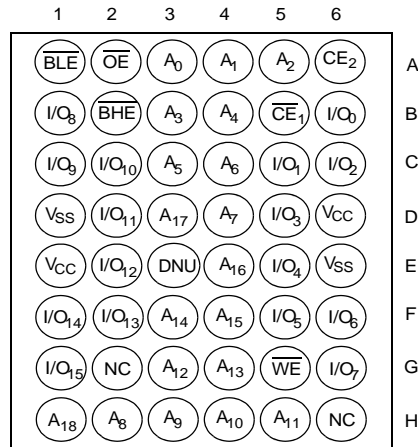


Note:

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Product Portfolio

Product	Range	V _{CC} Range			Speed	Power Dissipation					
						Operating (I _{CC}) mA				Standby (I _{SB2}) μA	
		Min.	Typ. ^[2]	Max.		f = 1 MHz		f = f _{max}			
CY62157CV25	Industrial	2.2V	2.5V	2.7V	55 ns	1.5	3	7	15	6	25
	Industrial				70 ns	1.5	3	5.5	12		
CY62157CV30	Industrial	2.7V	3.0V	3.3V	55 ns	1.5	3	7	15	8	25
	Industrial				70 ns	1.5	3	5.5	12	8	25
	Automotive				70 ns					8	70
CY62157CV33	Industrial	3.0V	3.3V	3.6V	55 ns	1.5	3	7	15	10	30
	Industrial				70 ns	1.5	3	5.5	12	10	30
	Automotive				70 ns					10	80

Pin Configurations^[2, 3, 4]
FBGA (Top View)

Pin Definitions

Name	Definition
Input	A₀-A₁₈ . Address Inputs
Input/Output	I/O₀-I/O₁₅ . Data lines. Used as input or output lines depending on operation
Input/Control	WE . Write Enable, Active LOW. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
Input/Control	CE₁ . Chip Enable 1, Active LOW.
Input/Control	CE₂ . Chip Enable 2, Active HIGH.
Input/Control	OE . Output Enable, Active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins
Ground	V_{SS} . Ground for the device
Power Supply	V_{CC} . Power supply for the device

Notes:

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25°C.
- NC pins are not connected on the die.
- E3 (DNU) can be left as NC or V_{SS} to ensure proper application.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied.....-55°C to +125°C

Supply Voltage to Ground Potential ...-0.5V to $V_{CCmax} + 0.5V$

DC Voltage Applied to Outputs in High-Z State^[5].....-0.5V to $V_{CC} + 0.3V$

DC Input Voltage^[5].....-0.5V to $V_{CC} + 0.3V$

Output Current into Outputs (LOW)20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range

Device	Range	Ambient Temperature [T _A] ^[6]	V _{CC}
CY62157CV25	Industrial	-40°C to +85°C	2.2V – 2.7V
CY62157CV30	Industrial	-40°C to +85°C	2.7V – 3.3V
	Automotive	-40°C to +125°C	2.7V – 3.3V
CY62157CV33	Industrial	-40°C to +85°C	3.0V – 3.6V
	Automotive	-40°C to +125°C	3.0V – 3.6V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62157CV25-55			CY62157CV25-70			Unit
			Min.	Typ. ^[2]	Max.	Min.	Typ. ^[2]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA V _{CC} = 2.2V	2.0			2.0			V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA V _{CC} = 2.2V			0.4			0.4	V
V _{IH}	Input HIGH Voltage		1.8		V _{CC} + 0.3V	1.8		V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage		-0.3		0.6	-0.3		0.6	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-1		+1	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC} f = 1 MHz	V _{CC} = 2.7V I _{OUT} = 0 mA CMOS Levels	7	15		5.5	12	mA
				1.5	3		1.5	3	
I _{SB1}	Automatic CE Power-Down Current—CMOS Inputs	CE ₁ ≥ V _{CC} - 0.2V or CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = f _{max} (Address and Data Only), f = 0 (OE, WE, BHE and BLE)		6	25		6	25	μA
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	CE ₁ ≥ V _{CC} - 0.2V or CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0, V _{CC} = 2.7V							

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62157CV30-55			CY62157CV30-70			Unit	
			Min.	Typ. ^[2]	Max.	Min.	Typ. ^[2]	Max.		
V _{OH}	Output HIGH Voltage	I _{OH} = -1.0 mA V _{CC} = 2.7V	2.4			2.4			V	
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA V _{CC} = 2.7V			0.4			0.4	V	
V _{IH}	Input HIGH Voltage		2.2		V _{CC} + 0.3V	2.2		V _{CC} + 0.3V	V	
V _{IL}	Input LOW Voltage		-0.3		0.8	-0.3		0.8	V	
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	Industrial	-1		+1	-1		+1	μA
			Automotive				-10		+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	Industrial	-1		+1	-1		+1	μA
			Automotive				-10		+10	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC} f = 1 MHz	V _{CC} = 3.3V I _{OUT} = 0 mA CMOS Levels	7	15		5.5	12	mA	
				1.5	3		1.5	3		

Notes:

- V_{IL(min.)} = -2.0V for pulse durations less than 20 ns.
- T_A is the "Instant-On" case temperature.

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions	CY62157CV30-55			CY62157CV30-70			Unit	
			Min.	Typ. ^[2]	Max.	Min.	Typ. ^[2]	Max.		
I _{SB1}	Automatic CE Power-Down Current—CMOS Inputs	CE ₁ ≥ V _{CC} - 0.2V or CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = f _{max} (Address and Data Only), f = 0 (OE, WE, BHE and BLE)	Industrial		8	25		8	25	μA
			Automotive					8	70	μA
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	CE ₁ ≥ V _{CC} - 0.2V or CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0, V _{CC} = 3.3V	Industrial		8	25		8	25	μA
			Automotive					8	70	μA

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62157CV33-55			CY62157CV33-70			Unit	
			Min.	Typ. ^[2]	Max.	Min.	Typ. ^[2]	Max.		
V _{OH}	Output HIGH Voltage	I _{OH} = -1.0 mA	V _{CC} = 3.0V	2.4			2.4		V	
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA	V _{CC} = 3.0V			0.4		0.4	V	
V _{IH}	Input HIGH Voltage			2.2		V _{CC} + 0.3V	2.2		V _{CC} + 0.3V	
V _{IL}	Input LOW Voltage			-0.3		0.8	-0.3		0.8	
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	Industrial	-1		+1	-1		+1	μA
			Automotive				-10		+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	Industrial	-1		+1	-1		+1	μA
			Automotive				-10		+10	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC} f = 1 MHz	V _{CC} = 3.6V I _{OUT} = 0 mA CMOS Levels		7	15		5.5	12	mA
					1.5	3		1.5	3	
I _{SB1}	Automatic CE Power-Down Current—CMOS Inputs	CE ₁ ≥ V _{CC} - 0.2V or CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = f _{max} (Address and Data Only), f = 0 (OE, WE, BHE, and BLE)	Industrial		10	30		10	30	μA
			Automotive					10	80	μA
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	CE ₁ ≥ V _{CC} - 0.2V or CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0, V _{CC} = 3.6V	Industrial		10	30		10	30	μA
			Automotive					10	80	μA

Thermal Resistance

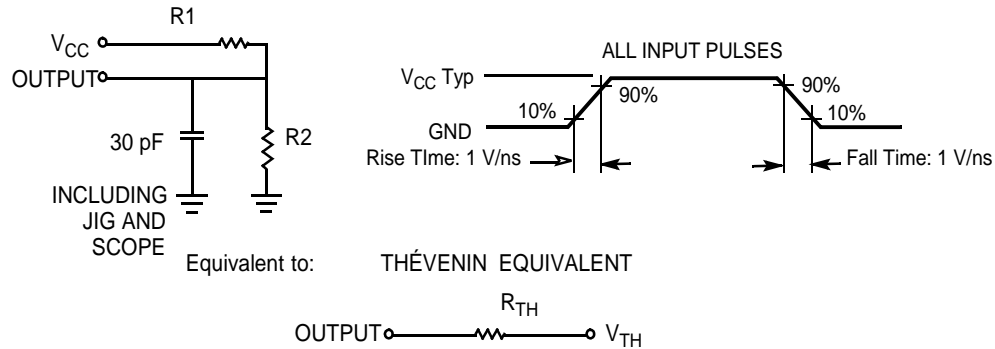
Parameter	Description	Test Conditions	BGA	Unit
Θ _{JA}	Thermal Resistance (Junction to Ambient) ^[7]	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	55	°C/W
Θ _{JC}	Thermal Resistance (Junction to Case) ^[7]		16	°C/W

Note:

7. Tested initially and after any design or process changes that may affect these parameters.

Capacitance^[7]

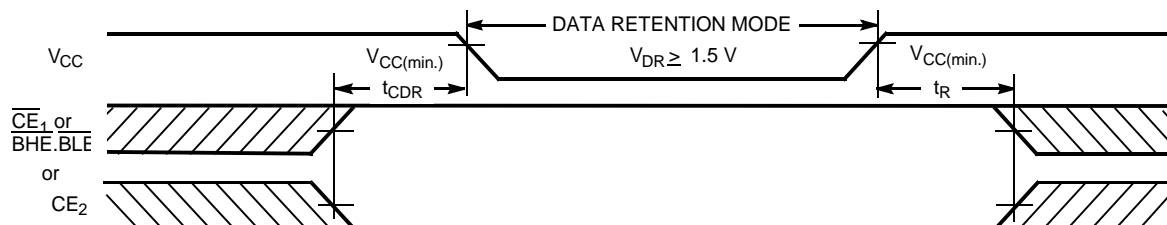
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC(\text{typ.})}$	6	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms


Parameters	2.5V	3.0V	3.3V	Unit
R1	16.6	1.105	1.216	$\text{K}\Omega$
R2	15.4	1.550	1.374	$\text{K}\Omega$
R_{TH}	8.0	0.645	0.645	$\text{K}\Omega$
V_{TH}	1.20	1.75	1.75	V

Data Retention Characteristics (Over the Operating Range)

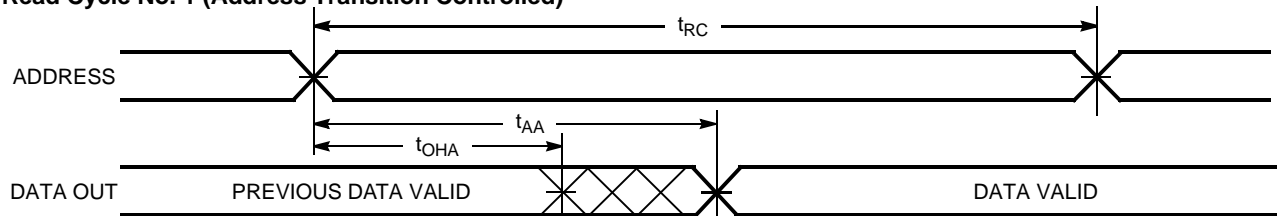
Parameter	Description	Conditions	Min.	Typ. ^[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.5			V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.5\text{V}$, $\overline{CE}_1 \geq V_{CC} - 0.2\text{V}$ or $\overline{CE}_2 \leq 0.2\text{V}$, $V_{IN} \geq V_{CC} - 0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$	Industrial	4	20	μA
			Automotive	4	60	μA
$t_{CDR}^{[8]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[8]}$	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform^[9]

Notes:

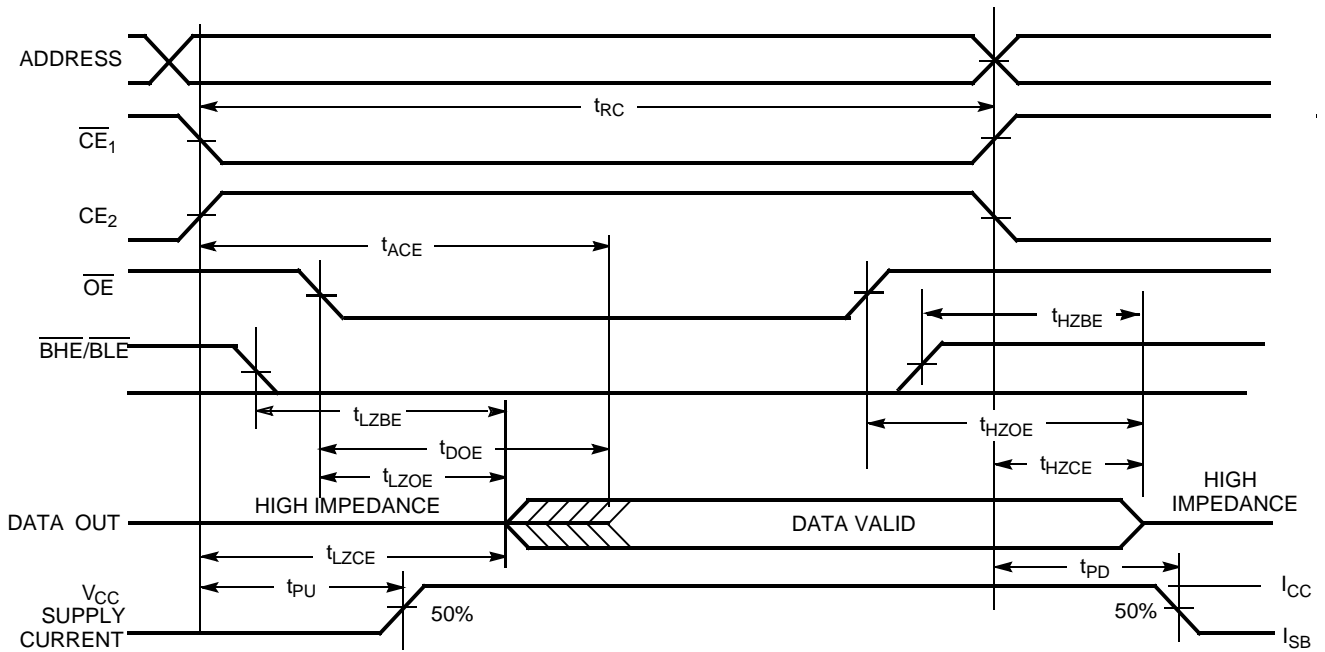
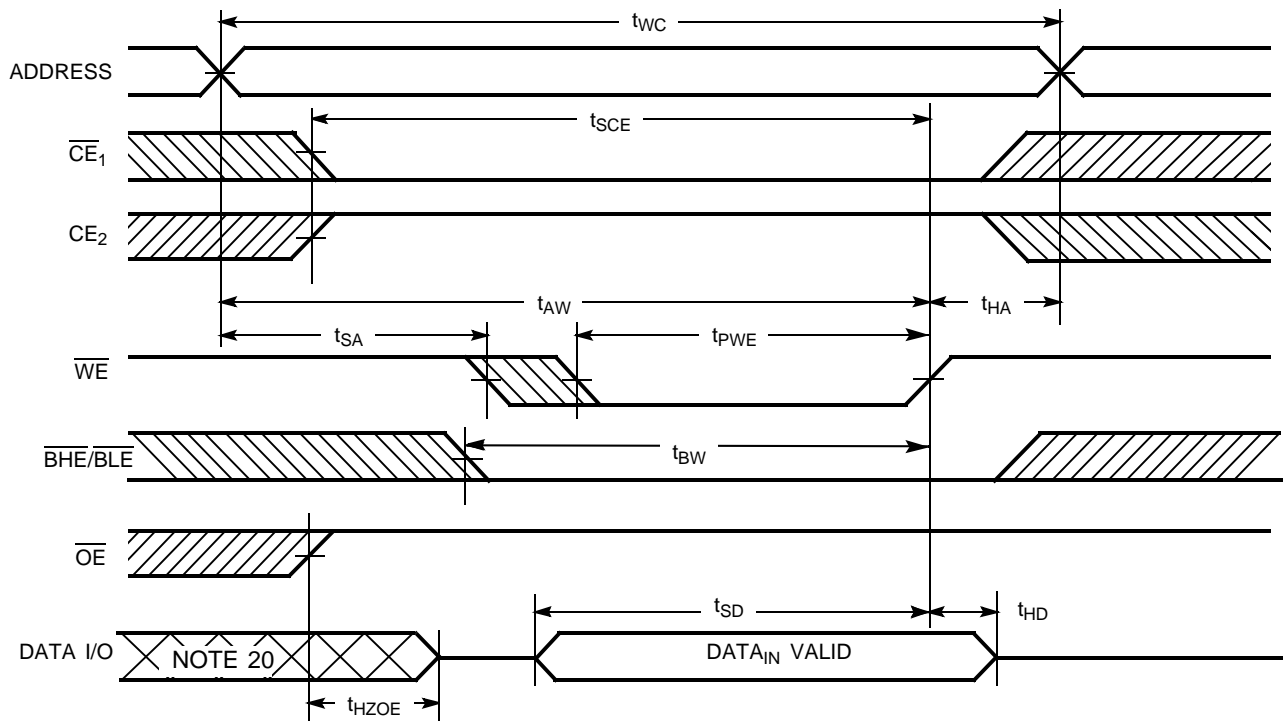
- Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(\text{min.})} > 100\ \mu\text{s}$ or stable at $V_{CC(\text{min.})} > 100\ \mu\text{s}$.
- $\overline{BHE.BLE}$ is the AND of both \overline{BHE} and \overline{BLE} . Chip can be deselected by either disabling the chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .

Switching Characteristics Over the Operating Range ^[10]

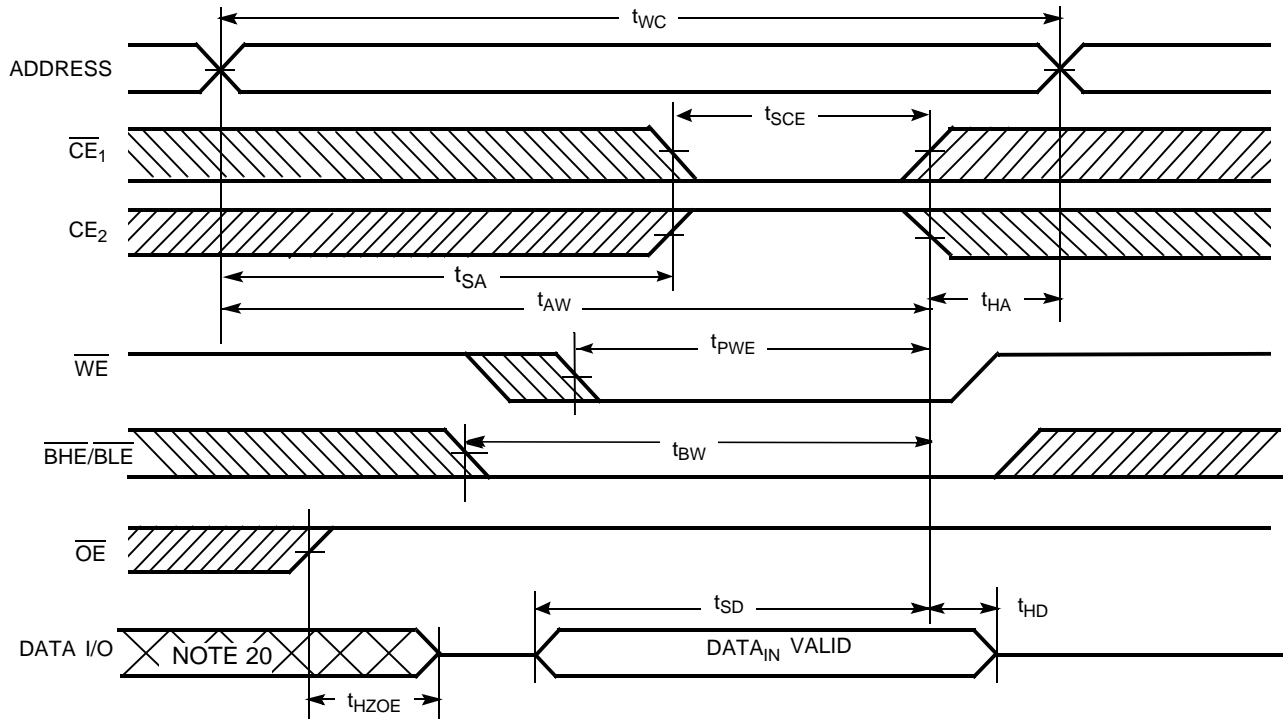
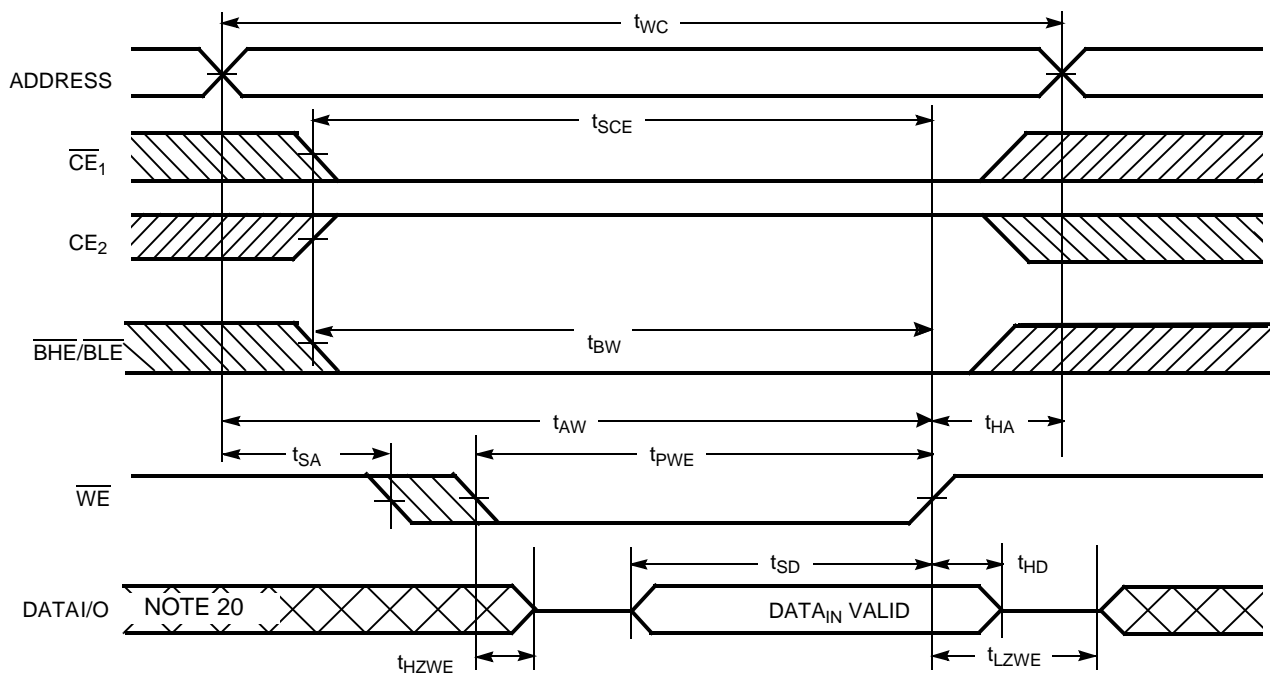
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	\overline{CE}_1 LOW and \overline{CE}_2 HIGH to Data Valid		55		70	ns
t_{DOE}	OE LOW to Data Valid		25		35	ns
t_{LZOE}	OE LOW to Low-Z ^[11]	5		5		ns
t_{HZOE}	OE HIGH to High-Z ^[11, 12]		20		25	ns
t_{LZCE}	\overline{CE}_1 LOW and \overline{CE}_2 HIGH to Low-Z ^[11]	10		10		ns
t_{HZCE}	\overline{CE}_1 HIGH or \overline{CE}_2 LOW to High-Z ^[11, 12]		20		25	ns
t_{PU}	\overline{CE}_1 LOW and \overline{CE}_2 HIGH to Power-up	0		0		ns
t_{PD}	\overline{CE}_1 HIGH or \overline{CE}_2 LOW to Power-down		55		70	ns
t_{DBE}	BHE/ \overline{BLE} LOW to Data Valid		55		70	ns
$t_{LZBE}^{[11]}$	BHE/ \overline{BLE} LOW to Low-Z ^[13]	5		5		ns
t_{HZBE}	BHE/ \overline{BLE} HIGH to High-Z ^[11, 12]		20		25	ns
Write Cycle^[14]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	\overline{CE}_1 LOW and \overline{CE}_2 HIGH to Write End	45		60		ns
t_{AW}	Address Set-up to Write End	45		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	\overline{WE} Pulse Width	45		50		ns
t_{BW}	BHE/ \overline{BLE} Pulse Width	50		60		ns
t_{SD}	Data Set-up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	\overline{WE} LOW to High-Z ^[11, 12]		20		25	ns
t_{LZWE}	\overline{WE} HIGH to Low-Z ^[11]	5		5		ns

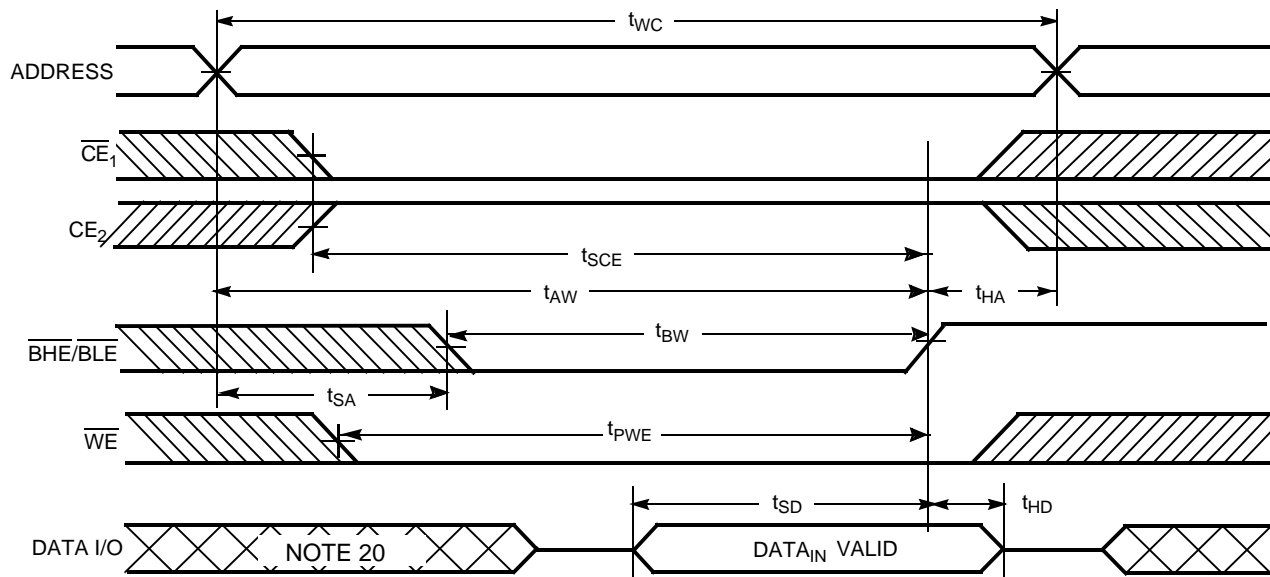
Switching Waveforms
Read Cycle No. 1 (Address Transition Controlled)^[15, 16]

Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
- When both byte enables are toggled together this value is 10 ns.
- The internal Write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, $\overline{CE}_2 = V_{IH}$. All signals must be ACTIVE to initiate a Write and any of these signals can terminate a Write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the Write.
- Device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, $\overline{CE}_2 = V_{IH}$.
- \overline{WE} is HIGH for Read cycle.

Switching Waveforms (continued)
Read Cycle No. 2 (\overline{OE} Controlled) [16, 17]

Write Cycle No. 1 (\overline{WE} Controlled) [14, 18, 19]

Notes:

17. Address valid prior to or coincident with \overline{CE}_1 , \overline{BHE} , \overline{BLE} transition LOW and CE_2 transition HIGH.
18. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
19. If \overline{CE}_1 goes HIGH or CE_2 goes LOW simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
20. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)
Write Cycle No. 2 (\overline{CE}_1 or \overline{CE}_2 Controlled) [14, 18, 19]

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [19]


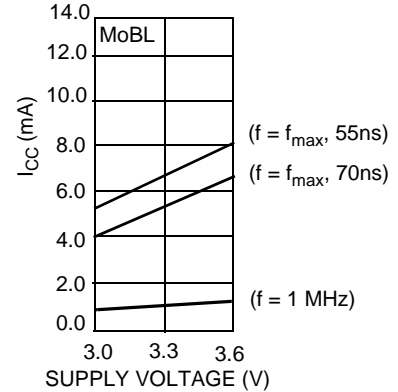
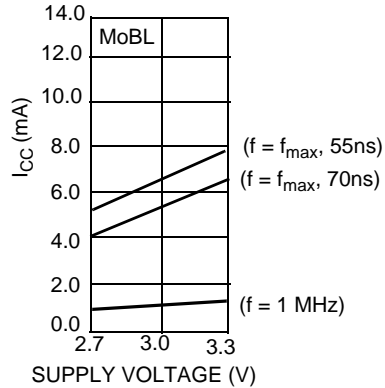
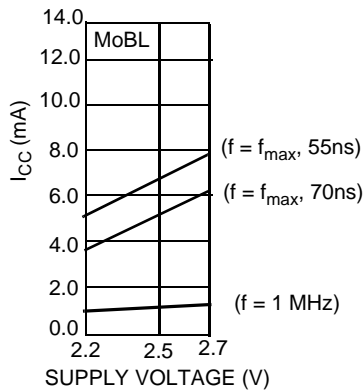
Switching Waveforms (continued)
Write Cycle No. 4 ($\overline{\text{BHE}}/\overline{\text{BLE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[19]

Truth Table

$\overline{\text{CE}}_1$	$\overline{\text{CE}}_2$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Read	Active (I_{CC})
L	H	H	L	L	H	Data Out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Write	Active (I_{CC})
L	H	L	X	L	H	Data In (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Write	Active (I_{CC})

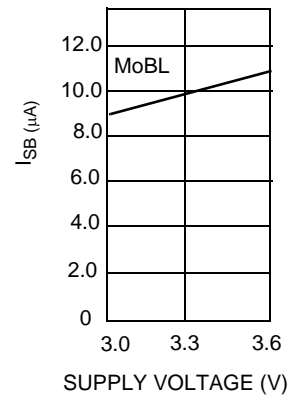
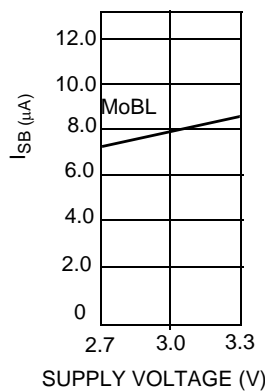
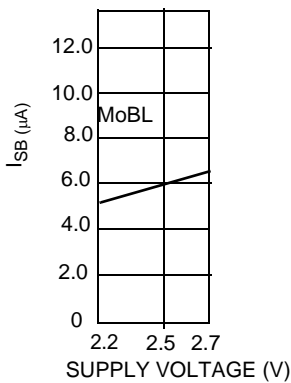
Typical DC and AC Characteristics

(Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25^\circ\text{C}$.)

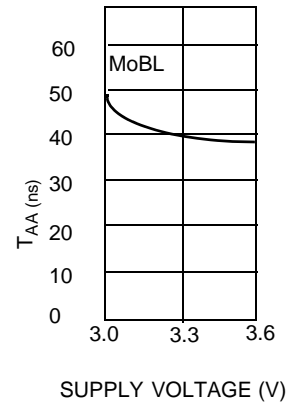
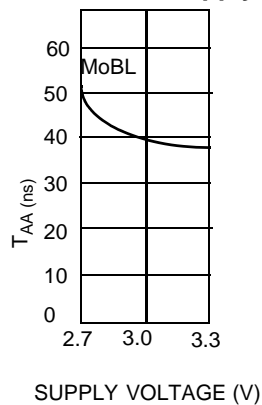
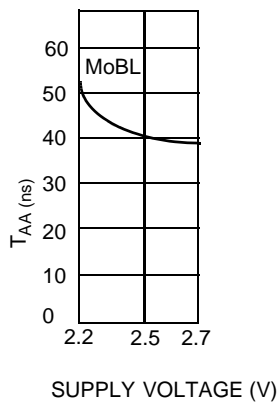
Operating Current vs. Supply Voltage



Standby Current vs. Supply Voltage



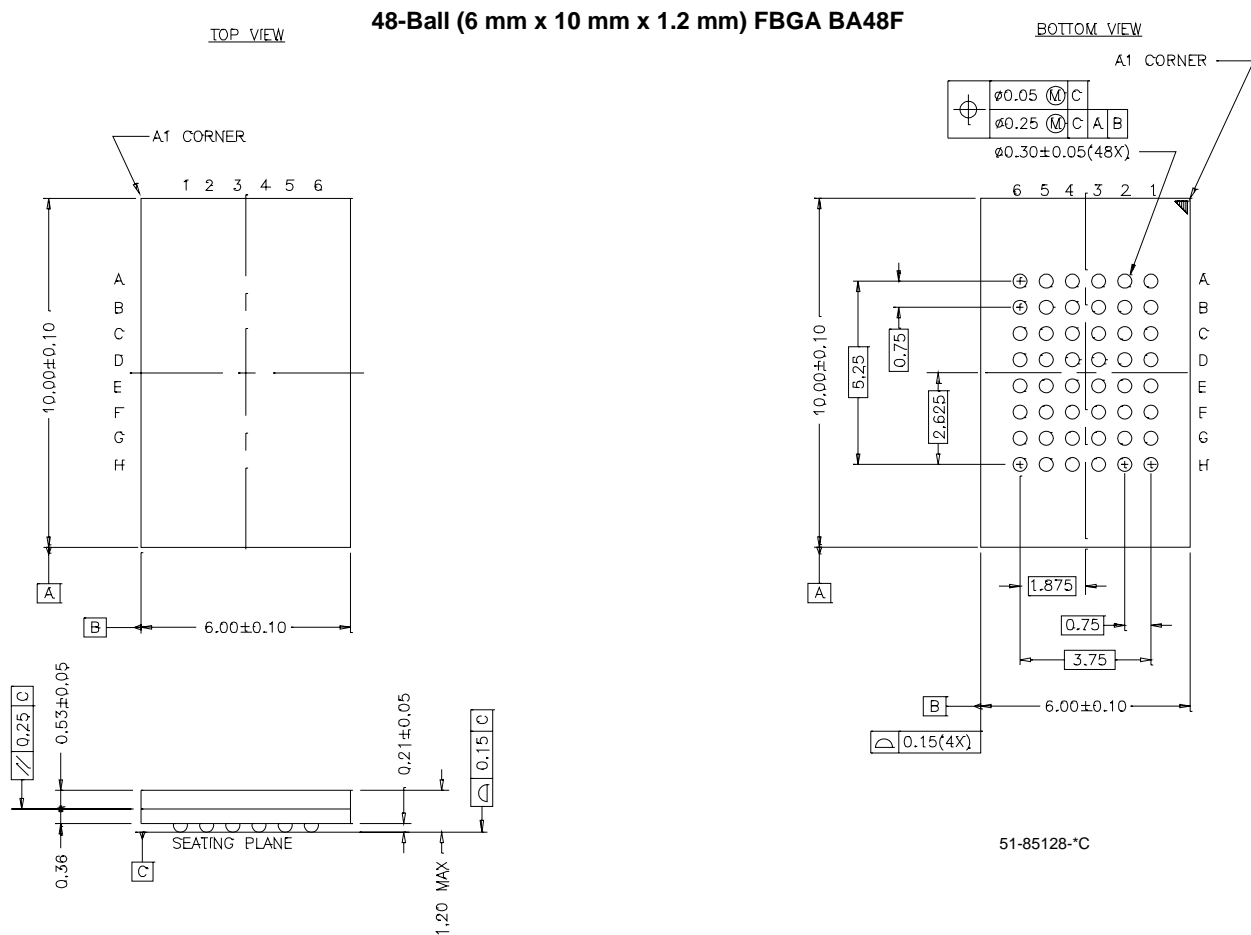
Access Time vs. Supply Voltage



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62157CV25LL-55BAI	BA48F	48-ball Fine-pitch BGA	Industrial
	CY62157CV30LL-55BAI			
	CY62157CV33LL-55BAI			
70	CY62157CV25LL-70BAI			Industrial
	CY62157CV30LL-70BAI			Industrial
	CY62157CV30LL-70BAE			Automotive
	CY62157CV33LL-70BAI	Industrial		
	CY62157CV33LL-70BAE	Automotive		

Package Diagram



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Document History Page

Document Title: CY62157CV25/30/33 512K x 16 Static Ram				
Document Number: 38-05014				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106184	05/10/01	HRT/MGN	New data sheet – Advance Information
*A	107241	07/24/01	MGN	Made corrections to Advance Information Added 55 ns bin
*B	109621	03/11/02	MGN	Changed from Advance Information to Final
*C	114218	05/01/02	GUG/MGN	Improved Typical and Max I _{CC} values
*D	238448	See ECN	AJU	Added Automotive Product information
*E	269729	See ECN	SYT	Added Automotive Product information for CY62157CV30 – 70 ns Added I _{LX} and I _{OZ} values for Automotive range of CY62157CV33 – 70 ns