



CYPRESS

CY28159

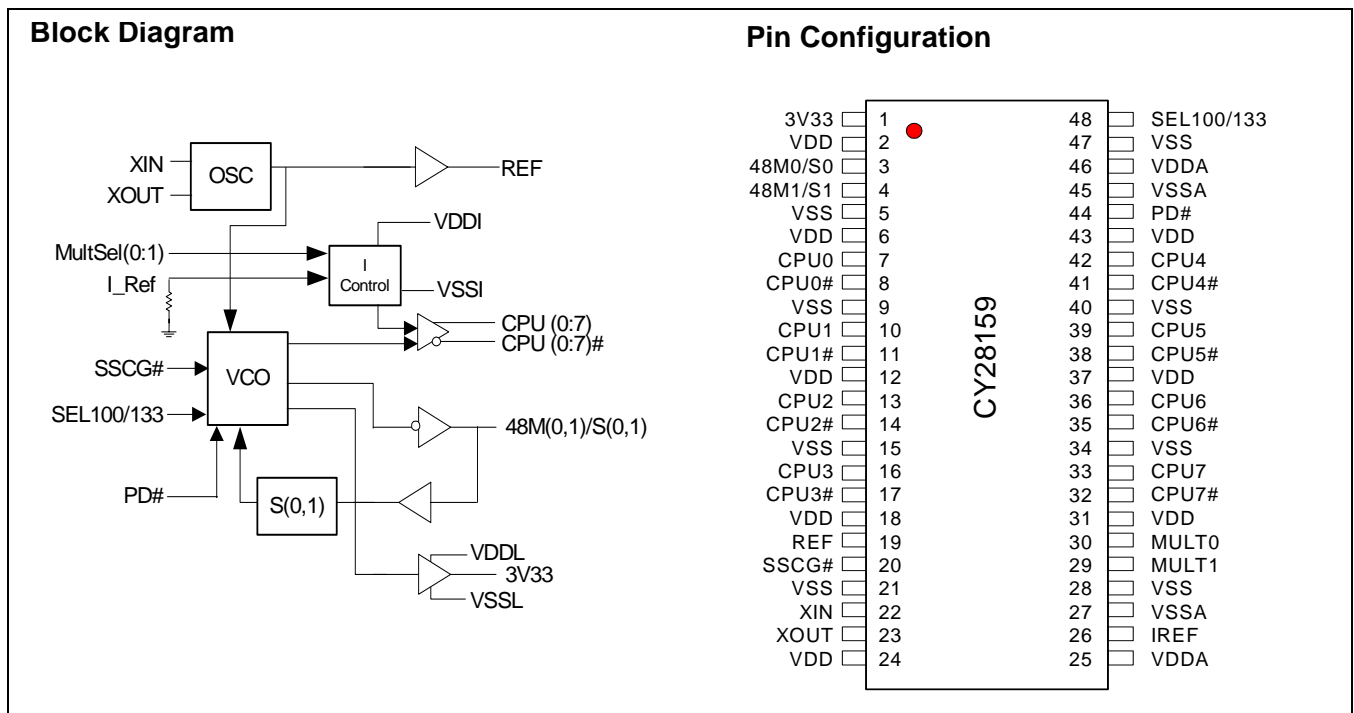
Clock Generator for Serverworks Grand Champion Chipset Applications

Features

- Eight differential CPU clock outputs
- One PCI output
- One 14.31818-MHz reference clock
- Two 48-MHz clocks
- All outputs compliant with Intel® specifications
- External resistor for current reference
- Selection logic for differential swing control, test mode, Hi-Z, power-down and spread spectrum
- 48-pin SSOP and TSSOP packages

Table 1. Frequency Selection

SEL 100/133	S0	S1	CPU(0:7), CPU#(0:7)	3V33	48M(0,1)	Notes
0	0	0	100 MHz	33.3MHz	48 MHz	Normal Operation
0	0	1	100 MHz	33.3MHz	Disable	Test Mode(recommended)
0	1	0	100 MHz	Disable	Disable	Test Mode (optional)
0	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z all outputs
1	0	0	133.3MHz	33.3MHz	48 MHz	Optional
1	0	1	133.3MHz	33.3MHz	Disable	Optional
1	1	0	200MHz	33.3MHz	48 MHz	Optional
1	1	1	N/A	N/A	N/A	Reserved



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Pin Description

Pin	Name	I/O ^[1]	Description
20	SSCG	PU I	When asserted LOW, this pin invokes Spread Spectrum functionality. Spread spectrum is applicable to CPU(0:7), CPU(0:7)#. This pin has a 250-kΩ internal pull-up.
7, 10, 13, 16, 42, 39, 36, 33	CPU(0:7)	O	Differential host clock outputs. These outputs are used in pairs, (CPU0-0#, CPU1-1#, CPU2-2#, CPU3-3#, CPU4-4#, CPU5-5#, CPU6-6#, and CPU7-7#) for differential clocking of the host bus. CPU(0:7) are 180 degrees out of phase with their complements, CPU(0:7)#. See <i>Table 1</i> on page 1
8, 11, 14, 17, 41, 38, 35, 32	CPU(0:7)#		
26	IRef	P	This pin establishes the reference current for the internal current steering buffers of the CPU clocks. A resistor is connected from this pin to ground to set the value of this current.
1	3V33	O	Fixed 33.3-MHz clock output.
44	PD#	PU I	When asserted LOW, this pin invokes a power-down mode by shutting off all the clocks, disabling all internal circuitry, and shutting down the crystal oscillator. The 48M(0:1) and REF clocks are driven LOW during this condition and the CPU clocks are driven HIGH and programmed with an 2X IREF current. It has a 250-kΩ internal pull-up.
3, 4	48M(0,1), S(0,1)	IO	S0 and S1 inputs are sensed on power-up and then internally latched. Afterwards the pins are 3V 48-MHz clocks.
48	SEL100/133	PU I	Input select pin. See <i>Table 1</i> on page 1. It has a 250-kΩ internal Pull-up
23	XOUT	O	Crystal Buffer output pin. Connects to a crystal only. When an external signal other than a crystal is used or when in Test mode, this pin is kept unconnected.
22	XIN	I	Crystal Buffer input pin. Connects to a crystal, or an external single ended input clock signal.
19	REF	O	A buffered output clock of the signal applied at Xin. Typically, 14.31818 MHz.
30, 29	Mult(0,1)	I	These input select pins configure the Ioh current (and thus the Voh swing amplitude) of the CPU clock output pairs. Each pin has a 250-kΩ internal Pull-up. See <i>Table 5</i> for current and resistor values.
25, 46	VDDA	P	3.3V power supply pins.
2, 6, 12, 18, 24, 31, 37, 43	VDD	P	3.3V power supply pins for common supply to the core.
5, 9, 15, 21, 28, 34, 40, 47	VSS	P	Ground pins for common supply to the core.
27, 45	VSSA	P	Ground pins.

Note:

1. Definition of I/O column mnemonic on pin description table above 1= Input pin, O = output pin, P = power supply pin, PU = indicates that a bidirectional pin contains pull-up resistor. This will insure that this pin of the device will be seen by the internal logic as a logic 1 level. Likewise pins with a PD designation are guaranteed to be seen as a logic 0 level if no external level setting circuitry is present at power up.

Table 2. Group Offset Specifications

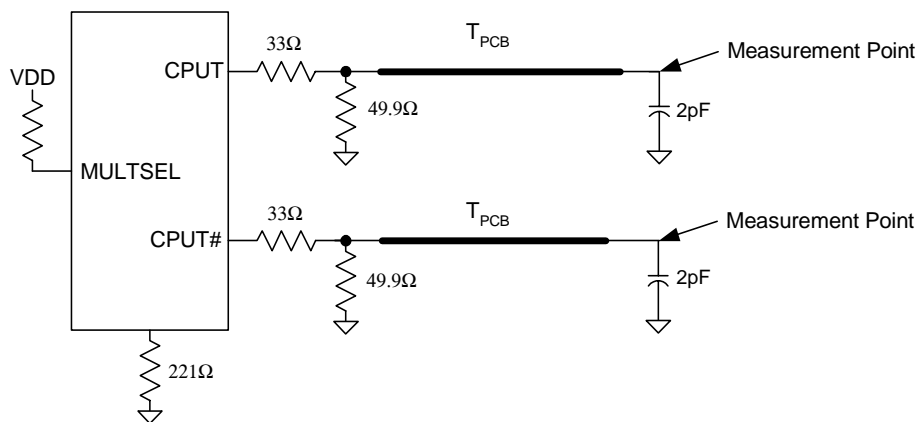
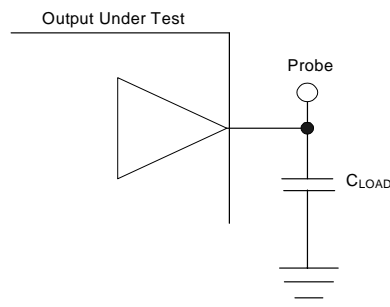
Group	Offset	Comments
CPU to 3V33	No requirement	
CPU to REF	No requirement	

Table 3. Group Limits and Parameters (Applicable to all settings: Sel133/100#=x)

Output Name	Max Load
CPU[(0:7)#]	See <i>Figure 1</i>
REF	20 pF
3V33	30 pF

Test Load Configuration

The following shows test load configurations for the different Host Clock Outputs.(MULTsel1 = 0, MULTsel0 = 1)


Figure 1. 0.7V Test Load Termination

Figure 2. Lumped Load Termination

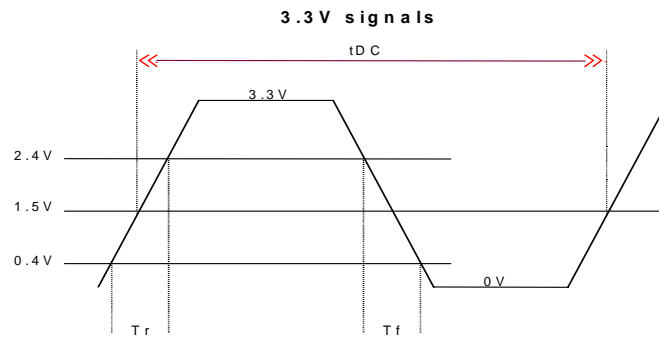


Figure 3. 3.3V Measurement Points

Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is a modulation technique applied here for maximum efficiency in minimizing Electro-Magnetic Interfer-

ence radiation generated from repetitive digital signals mainly clocks. For a detailed explanation of Spread Spectrum Clock Generation.

Table 4. Spectrum Spreading Selection Table

Unspread Frequency in MHz	Spread Spectrum Parameter			
	Downspreading			
	F Min(MHz)	F Center(MHz)	F Max(MHz)	Spread (%)
100	99.5	99.75	100	-0.5%
133.3	132.66	132.67	133	-0.5%
200	199.5	199.75	200	-0.5%

Power Management Functions

Table 5. Host Swing Select Functions^[2]

Multsel0	MultSel1	Board Target Trace/TermZ	Reference Rr, Iref = Vdd(3*Rr) Note 3	Output Current	Voh@Z, Iref = 2.32 mA
0	0	60 Ohms	Rf = 475 1%, Iref = 2.32 mA	Ioh = 5*Iref	07V @60
0	0	50 Ohms	Rr = 475 1%,Iref = 2.32 mA	Ioh = 5*Iref	0.59V @ 50
0	1	60 Ohms	Rr = 475 1%,Iref = 2.32 mA	Ioh = 6*Iref	0.85V @ 60
0	1	50 Ohms	Rr = 475 1%,Iref = 2.32 mA	Ioh = 6*Iref	0.71V @ 50
1	0	60 Ohms	Rr = 475 1%,Iref = 2.32 mA	Ioh = 4*Iref	0.56V @ 60
1	0	50 Ohms	Rr = 475 1%,Iref = 2.32 mA	Ioh = 4*Iref	0.47V @ 50
1	1	60 Ohms	Rr = 475 1%,Iref = 2.32 mA	Ioh = 7*Iref	0.99V @ 60
1	1	50 Ohms	Rr = 475 1%,Iref = 2.32 mA	Ioh = 7*Iref	0.82V @ 50

Notes:

2. The entries in boldface are the primary system configurations of interest. The outputs should be optimized for these configurations.
3. Rr refers to the resistance placed in series with the Iref input and V_{SS}.

Buffer Characteristics

Current Mode CPU Clock Buffer Characteristics

The current mode output buffer detail and current reference circuit details are contained elsewhere in this datasheet. The following parameters are used to specify output buffer characteristics:

1. Output impedance of the current mode buffer circuit - R_o (see *Figure 4*)
2. Minimum and maximum required voltage operation range of the circuit - V_{op} (see *Figure 4*).
3. Series resistance in the buffer circuit - R_{os} (see *Figure 4*)
4. Current accuracy at given configuration into nominal test load for given configuration

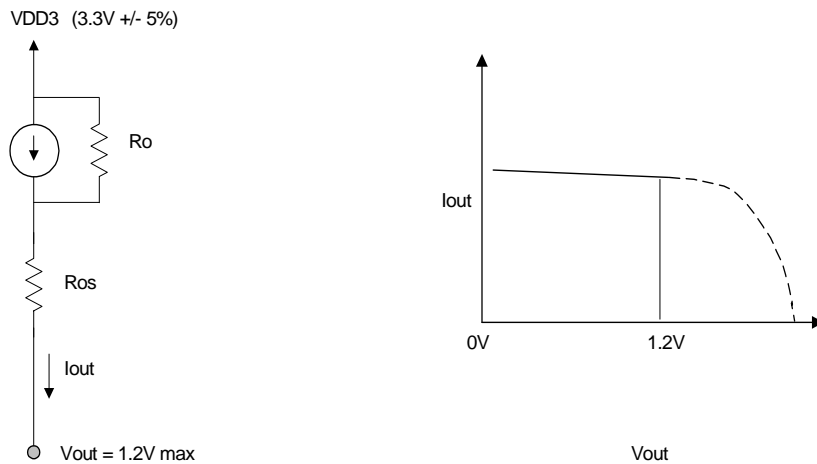


Figure 4.

Table 6. Host Clock (HSCL) Buffer Characteristics

Characteristics	Minimum	Maximum
R_o	3000 Ohms (recommended)	N/A
R_{os}	Unspecified	Unspecified
V_{out}	N/A	1.2 Volt

I_{out} is selectable depending on implementation. The parameters above supply to all configurations. V_{out} is the voltage at the pin of the device.

The various output current configurations are shown in the host swing select functions table. For all configurations, the deviation from the expected output current is $\pm 7\%$ as shown in the table current accuracy.

Table 7. Current Accuracy

	Conditions	Configuration	Load	Min.	Max.
I _{out}	V _{DD} = nominal (3.30V)	All combinations of M0, M1 and Rr shown in Host Swing Select Function, <i>Table 5</i> on page 5	Nominal test load for given configuration	-7% I _{nom}	+7% I _{nom}
I _{out}	V _{DD} = 3.30 ± 5%	All combinations of M0, m1 and Rr shown in Host Swing Select Function, <i>Table 5</i> on page 5	Nominal test load for given configuration	-12% I _{nom}	+12% I _{nom}

Table 8. Buffer Characteristics for REF, 48M(0,1)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I _{OH} _{min}	Pull-Up Current Min.	V _{OH} = V _{DDmin} - 0.5V (2.64V)	-12		-53	mA
I _{OH} _{max}	Pull-Up Current Max.	V _{OH} = V _{DDmin} /2 (1.56V)	-27		-92	mA
I _{OL} _{min}	Pull-Down Current Min.	V _{OL} = 0.4V	9		27	mA
I _{OL} _{max}	Pull-Down Current Max.	V _{OL} = V _{DDmin} /2 (1.56V)	26		79	mA
Trh	3.3V Output Rise Edge Rate	3.3V ± 5% @ 0.4V-2.4V	0.5		2.0	V/ns
Tfh	3.3V Output Fall Edge Rate	3.3V ± 5% @ 2.4V-0.4V	0.5		2.0	V/ns

Table 9. Buffer Characteristics for 3V33^[4]

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I _{OH} _{min}	Pull-Up Current Min.	V _{OH} = V _{DDmin} - 0.5V (2.64V)	-11		-83	mA
I _{OH} _{max}	Pull-Up Current Max.	V _{OH} = V _{DDmin} /2 (1.56V)	-30		-184	mA
I _{OL} _{min}	Pull-Up Current Max.	V _{OL} = 0.4V	9		38	mA
I _{OL} _{max}	Pull-Down Current Max.	V _{OL} = V _{DDmin} /2 (1.56V)	28		148	mA
Trh	3.3V Output Rise Edge Rate	3.3V ± 5% @ 0.4V-2.4V	1/1		4/1	V/ns
Tfh	3.3V Output Fall Edge Rate	3.3V ± 5% @ 2.4V-0.4V	1/1		4/1	V/ns

Note:

4. I_{nom} refers to the expected current based on the configuration of the device.

Maximum Ratings^[5]

Input Voltage Relative to V_{SS} : $V_{SS} - 0.3V$
 Input Voltage Relative to V_{DDQ} or AV_{DD} : $V_{DD} + 0.3V$
 Storage Temperature: $-65^{\circ}C$ to $+150^{\circ}C$
 Operating Temperature: $0^{\circ}C$ to $+70^{\circ}C$
 Maximum ESD 2000V
 Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field. However, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range.

$$V_{SS} < (V_{IN} \text{ or } V_{OUT}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters ($V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VIL1	Input Low Voltage	Note 6			0.8	Vdc
VIH1	Input High Voltage		2.0			Vdc
IIL	Input Low Current (@ $V_{IN} - V_{DD}$)	For internal pull-up resistors ^[6]	-16		-4	μA
IIH	Input High Current (@ $V_{IN} - V_{DD}$)		0		5	μA
IIL	Input Low Current (@ $V_{IN} - V_{SS}$)	For internal pull-down resistors ^[6]	0			μA
IIH	Input High Current (@ $V_{IN} - V_{SS}$)		4		16	μA
Ioz	Three-State leakage current				10	μA
Idd	Static Supply Current	PwrDwn = Low			80	mA
Issd	Dynamic Supply Current	133 MHz CPU ^[8]			200	mA
Cin	Input Pin Capacitance				5	pF
Cout	Output Pin Capacitance				6	pF
Lpin	Pin Inductance				7	nH
Cxtal	Crystal Pin Capacitance	Measured from Pin to Ground.	34	36	38	pH
Txs	Crystal Startup Time	From stable 3.3V power supply			40	μS
Rpi	Internal Pull-up and Pull-down Resistor Value ^[7]		200	250	500	k Ω

Notes:

5. The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
6. Applicable to input signals: Sel100/133, Sel(0:1), Spread#, PWRDN#, Mult(0:1)
7. Although internal pull-up or pull-down resistors have a typical value of 250k, this value may vary between 200k and 500k.
8. All outputs loaded as per Table 3.

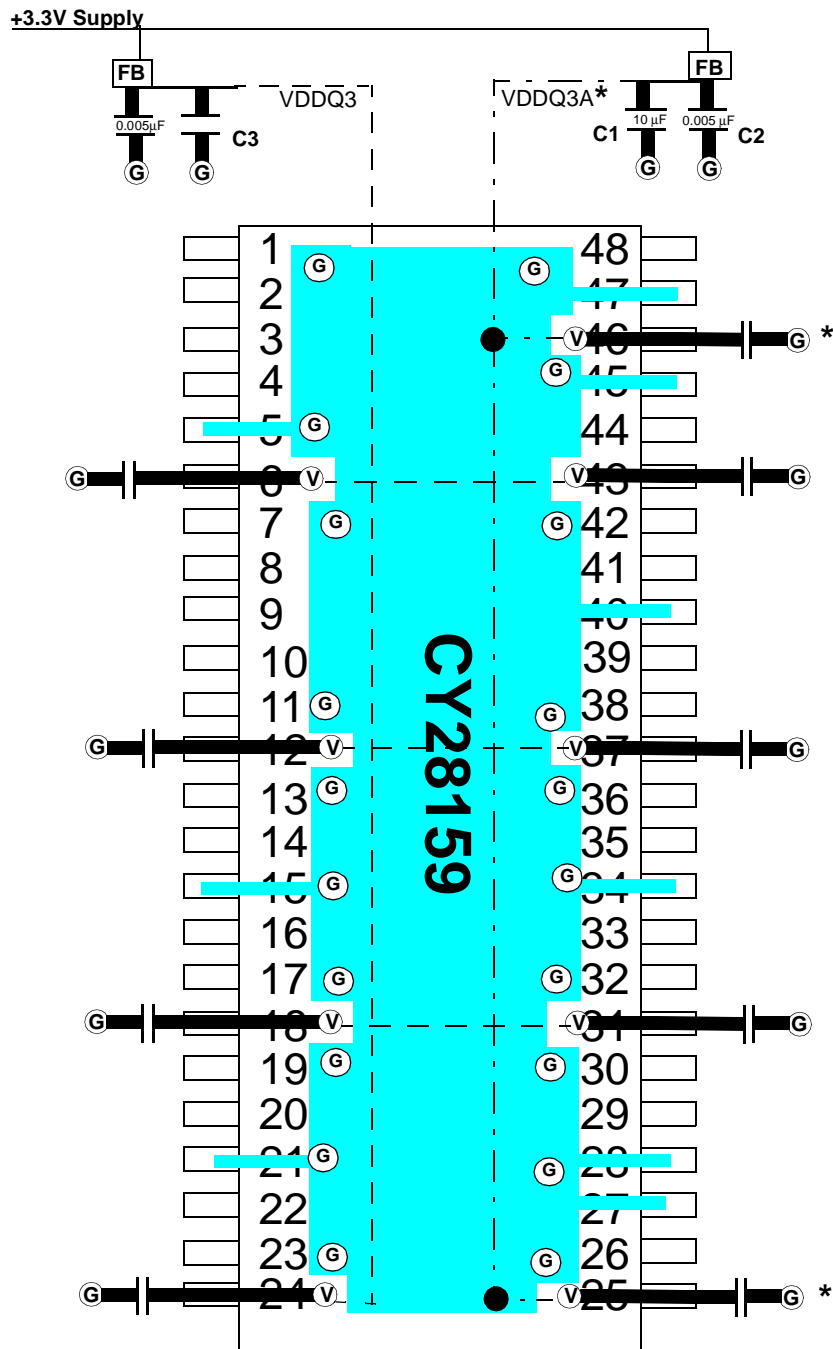
AC Parameters ($V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$)

Symbol	Description	133 MHz Host		100 MHz Host		Unit	Notes
		Min.	Max.	Min.	Max.		
CPU							
TPeriod	CPU(0:7), (0:7)# Period	7.35	7.65	9.85	10.2	ns	10,12
Tr/Tf	CPU[(0:7), (0:7)#] Rise and Fall Times	175	700	175	700	ps	10,11
TSKEW1	Skew from Any CPU Pair to Any CPU Pair		100		100	ps	10,12,13
TCJJ	CPU[(0:7), (0:7)#] Cycle to Cycle Jitter		150		150	ps	10,12,13
Vover	CPU[(0:7), (0:7)#] Overshoot		Voh + 0.2		Voh + 0.2	V	10,17
Vunder	CPU[(0:7), (0:7)#] Undershoot		-0.2		-0.2	V	10,17
Vcrossover	CPU(0:7), to CPU(0:7)# Crossover Point	45%Voh	55%Voh	45%Voh	55%Voh	V	9, 10,12
Tduty	Duty Cycle	45	55	45	55	%	10,12
33MHz							
Tperiod	3V33 Period	15.0	16.0	15.0	15.2	ns	10,12
THIGH	3V33 High Time	5.25		5.25		ns	10,14
TLOW	3V33 Low Time	5.05		5.05		ns	10,15
Tr/Tf	3V33 Rise and Fall Times	0.5	2.0	0.5	2.0	ns	10,11
TCCJ	3V33 Cycle to Cycle Jitter		300	-	300	ps	10,12,13
Tduty	Duty Cycle	45	55	45	55	%	10,12
REF							
Tperiod	REF Period	69.8412	71.0	69.8413	71.0	nS	10,12
Tr/Tf	REF Rise and Fall Times	1.0	4.0	1.0	4.0	nS	10,11
TCCj	REF Cycle to Cycle Jitter		1000		1000	pS	10,12
Tduty	Duty Cycle	45	55	45	55	%	10,12
48MHz							
TDC	48MHz(0,1) Duty Cycle	45	55	45	55	%	10,12
Tperiod	48MHz(0,1) Period	20.8299	20.8333	20.8299	20.8333	ns	10,12
Tr/Tf	48MHz(0,1) Rise and Fall Times	1.0	4.0	1.0	4.0	ps	10,11
TCCJ	48MHz(0,1) Cycle to Cycle Jitter		500		500	ps	10,12
Zout	48MHz Buffer Output Impedance	20		20		Ω	
tpZL, tpZH	Output Enable Delay (all outputs)	1.0	10.0	1.0	10.0	ns	16
tpLZ, tpZH	Output Disable Delay (all outputs)	1.0	10.0	1.0	10.0	ns	16
tstable	All Clock Stabilization from Power-up		3		3	ms	

Notes:

9. This parameter is measured at the crossing points of the differential signals, and acquired as an average over 1 μ s duration, with a crystal center frequency of 14.31818 MHz.
10. All outputs loaded as per Table 3, see Figure 2.
11. Probes are placed on the pins, and measurements are acquired between 0.4V and 2.4V for 3.3V signals and at 20% and 80% for CPU[(0:7), (0:7)#] signals (see Figure 3).
12. Probes are placed on the pins, and measurements are acquired at 1.5V for 3.3V signals and at crossing points for CPU clocks (see Figure 3).
13. This measurement is applicable with Spread ON or Spread OFF.
14. Probes are placed on the pins, and measurements are acquired at 2.4V (see Figure 3).
15. Probes are placed on the pins, and measurements are acquired at 0.4V. (see Figure 3).
16. As this function is available through SEL(0,1), therefore, the time specified is guaranteed by design.
17. Determined as a fraction of $2 \cdot (Trp - Trn) / (Trp + Trn)$ where Trp is a rising edge and Trn is an intersecting falling edge.

Sample Layout



FB = Dale ILB1206 - 300 (300Ω @ 100 MHz)

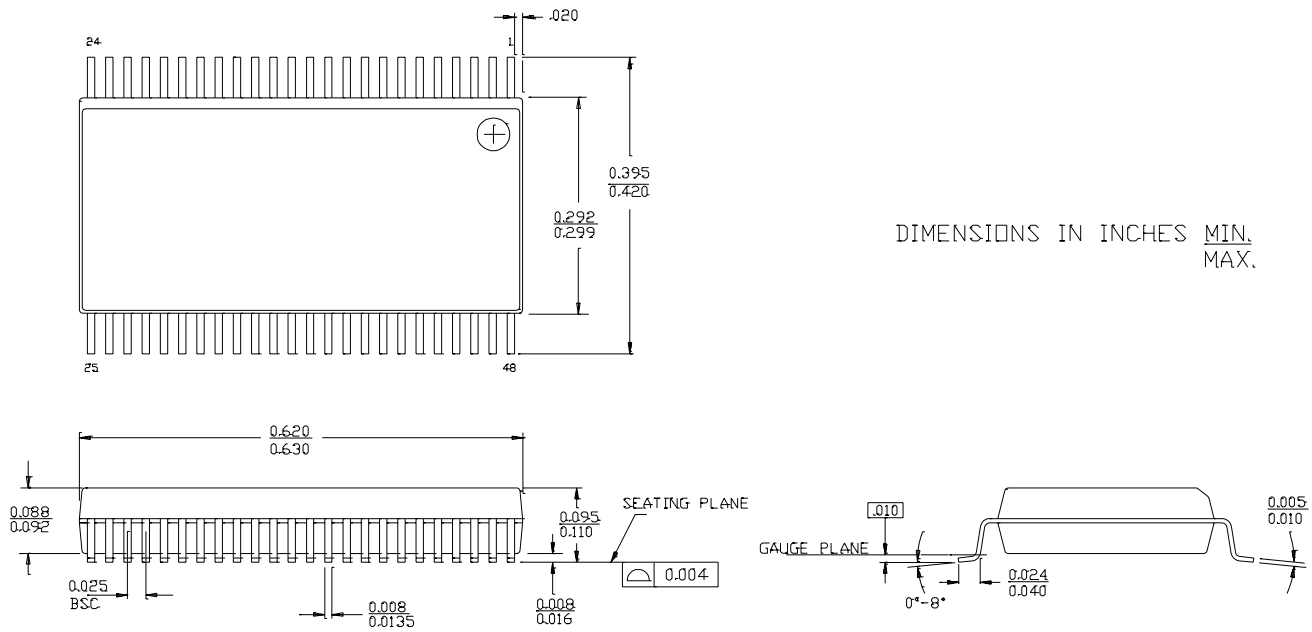
Ceramic Caps C1 & C3 = 10–22 µF C2 & C4 = 0.005 µF

ⓐ = VIA to GND plane layer ⓑ = VIA to respective supply plane layer

Note: Each supply plane or strip should have a ferrite bead and capacitors
All bypass caps = 0.1 µF ceramic. Low ESR

Ordering Information

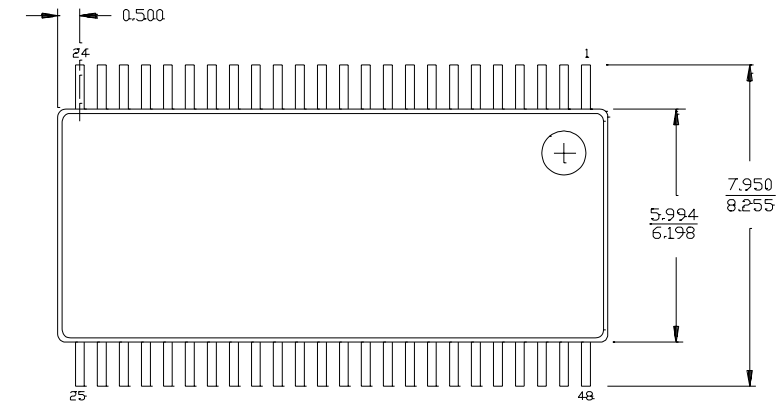
Part Number	Package Type	Product Flow
CY28159PVC	48-Pin SSOP	Commercial, 0° to 70°C
CY28159PVCT	48-Pin SSOP - Tape and Reel	Commercial, 0° to 70°C
CY28159ZC	48-Pin TSSOP	Commercial, 0° to 70°C
CY28159ZCT	48-Pin TSSOP - Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions
48-Lead Shrunken Small Outline Package O48


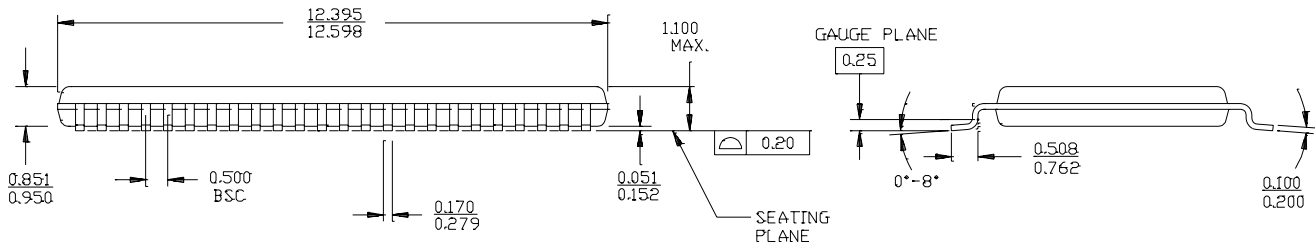
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Package Drawing and Dimensions (continued)

48-Lead Thin Shrink Small Outline Package, Type II (6 mm x 12 mm) Z48



DIMENSIONS IN MM MIN.
MAX.



51-85059-B

Document Title: CY28159 Clock Generator for Serverworks Grand Champion Chipset Applications				
Document Number: 38-07118				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	111426	01/22/02	DMG	New data sheet
*A	122789	12/27/02	RBI	Add power up requirements to maximum ratings information