



CYPRESS

CY29658

2.5V or 3.3V 200-MHz 10-Output Zero Delay Buffer

Features

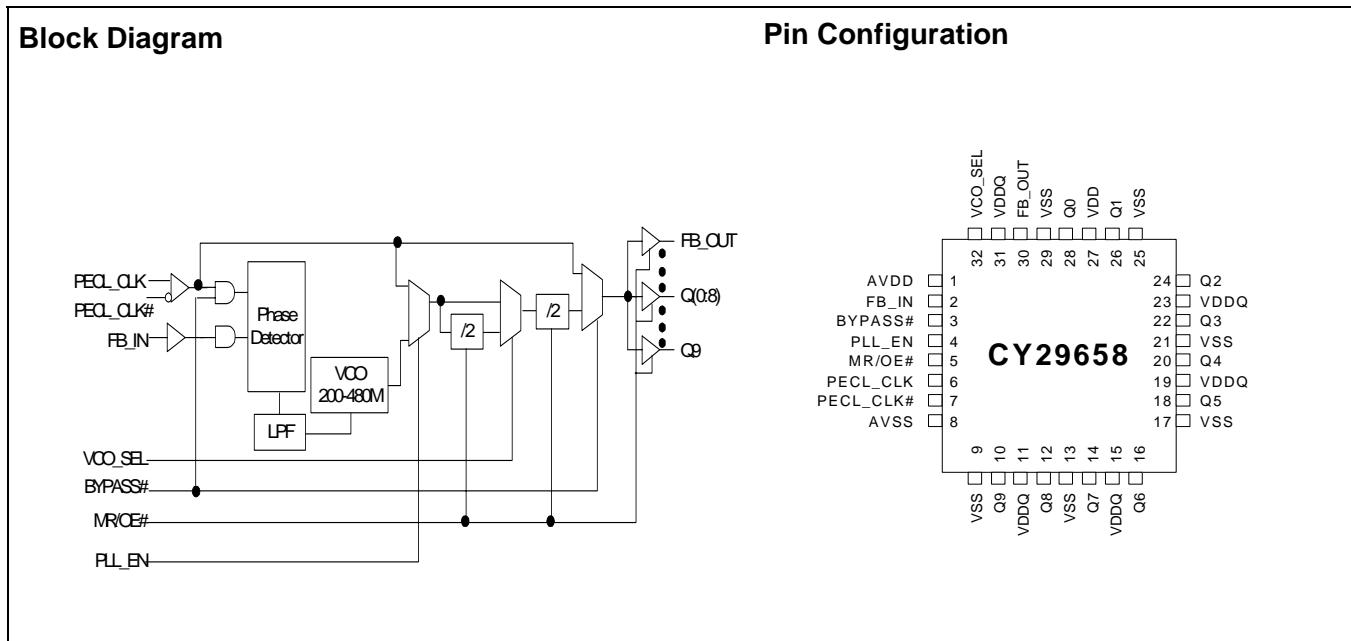
- Output frequency range: 50 MHz to 200 MHz
- Input frequency range: 50 MHz to 200 MHz
- 2.5V or 3.3V operation
- Ten clock outputs: drive up to 20 clock lines
- One Feedback output
- LVPECL reference clock input
- 150-ps max output-output skew
- Phase-locked loop (PLL) bypass mode
- Spread Aware™
- Output enable/disable
- Pin-compatible with MPC9658 and MPC958
- Industrial temperature range: -40°C to +85°C
- 32-Pin 1.0mm TQFP package

Description

The CY29658 is a low-voltage high-performance 200-MHz PLL-based zero delay buffer designed for high-speed clock distribution applications. The CY29658 features an LVPECL reference clock input and provides ten outputs plus one feedback output. VCO output divides by two or four per VCO_SEL setting (see *Function Table*). Each LVCMOS-compatible output can drive 50Ω series- or parallel-terminated transmission lines. For series-terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:20.

The PLL is ensured stable given that the VCO is configured to run between 200 MHz to 500 MHz. This allows a wide range of output frequencies from 50 MHz to 200 MHz. For normal operation, the external feedback input, FB_IN, is connected to the feedback output, FB_OUT. The internal VCO is running at multiples of the input reference clock set by the feedback divider (see *Frequency Table*).

When PLL_EN is LOW, PLL is bypassed and the reference clock directly feeds the output dividers. This mode is fully static and the minimum input clock frequency specification does not apply. When BYPASS# is set LOW, PLL and output dividers are bypassed resulting in a 1:11 LVPECL to LVCMOS high performance fanout buffer. For normal PLL operation, both PLL_EN and BYPASS# are set HIGH.



Pin Description^[1]

| Pin | Name | I/O | Type | Description |
|--|-----------|--------|---------|---|
| 6 | PECL_CLK | I, PU | LVPECL | LVPECL reference clock input. |
| 7 | PECL_CLK# | I, PU | LVPECL | LVPECL reference clock input. Pull-up to VDD/2. |
| 10, 12, 14, 16, 18, 20, 22, 24, 26, 28 | Q(9:0) | O | LVC MOS | Clock output. |
| 30 | FB_OUT | O | LVC MOS | Feedback clock output. Connect to FB_IN for normal operation. |
| 2 | FB_IN | I, PU | LVC MOS | Feedback clock input. Connect to FB_OUT for normal operation. This input should be at the same voltage rail as input reference clock. See <i>Table 1</i> . |
| 5 | MR/OE# | I, PD | LVC MOS | Output enable/disable input. See <i>Table 2</i> . |
| 4 | PLL_EN | I, PU | LVC MOS | PLL enable/disable input. See <i>Table 2</i> . |
| 3 | BYPASS# | I, PU | LVC MOS | PLL and output divider bypass select input. See <i>Table 2</i> . |
| 32 | VCO_SEL | I, PU | LVC MOS | VCO divider select input. See <i>Table 2</i> . |
| 11, 15, 19, 23, 31 | VDDQ | Supply | VDD | 2.5V or 3.3V power supply for output clocks. ^[2,3] |
| 1 | AVDD | Supply | VDD | 2.5V or 3.3V power supply for PLL. ^[2,3] |
| 27 | VDD | Supply | VDD | 2.5V or 3.3V power supply for core and inputs. ^[2,3] |
| 8 | AVSS | Supply | Ground | Analog ground. |
| 9, 13, 17, 21, 25, 29 | VSS | Supply | Ground | Common ground. |

Table 1. Frequency Table

| Feedback Output Divider | VCO | Input Frequency Range (AVDD = 3.3V) | Input Frequency Range (AVDD = 2.5V) |
|-------------------------|-----------------|-------------------------------------|-------------------------------------|
| ÷2 | Input Clock * 2 | 100 MHz to 200 MHz | 100 MHz to 200 MHz |
| ÷4 | Input Clock * 4 | 50 MHz to 125 MHz | 50 MHz to 100 MHz |

Table 2. Function Table

| Control | Default | 0 | 1 |
|---------|---------|---|--|
| VCO_SEL | 1 | VCO ÷ 1 | VCO ÷ 2 |
| PLL_EN | 1 | Bypass mode, PLL disabled. The input clock connects to the output dividers | PLL enabled. The VCO output connects to the output dividers |
| BYPASS# | 1 | Bypass mode with PLL and output dividers bypassed. The input clock connects to the outputs. | Selects the output dividers |
| MR/OE# | 0 | Outputs enabled | Outputs disabled (three-state), VCO running at its minimum frequency |

Notes:

1. PU = Internal pull-up, PD = Internal pull-down.
2. A 0.1-μF bypass capacitor should be placed as close as possible to each positive power pin (<0.2"). If these bypass capacitors are not close to the pins their high-frequency filtering characteristics will be cancelled by the lead inductance of the traces.
3. AVDD and VDD pins must be connected to a power supply level that is at least equal or higher than that of VDDQ power supply pin.

Absolute Maximum Conditions

| Parameter | Description | Condition | Min. | Max. | Unit |
|------------------|-----------------------------------|-----------------------------|-------|-----------------------|-------|
| V _{DD} | DC Supply Voltage | | -0.3 | 5.5 | V |
| V _{DD} | DC Operating Voltage | Functional | 2.375 | 3.465 | V |
| V _{IN} | DC Input Voltage | Relative to V _{SS} | -0.3 | V _{DD} + 0.3 | V |
| V _{OUT} | DC Output Voltage | Relative to V _{SS} | -0.3 | V _{DD} + 0.3 | V |
| V _{TT} | Output termination Voltage | | | V _{DD} ÷ 2 | V |
| LU | Latch Up Immunity | Functional | 200 | | mA |
| R _{PS} | Power Supply Ripple | Ripple frequency < 100 kHz | | 150 | mVp-p |
| T _S | Temperature, Storage | Non-functional | -65 | +150 | °C |
| T _A | Temperature, Operating Ambient | Functional | -40 | +85 | °C |
| T _J | Temperature, Junction | Functional | | 150 | °C |
| ∅ _{JC} | Dissipation, Junction to Case | Functional | | 42 | °C/W |
| ∅ _{JA} | Dissipation, Junction to Ambient | Functional | | 105 | °C/W |
| ESD _H | ESD Protection (Human Body Model) | | 2000 | | V |
| FIT | Failure in Time | Manufacturing test | | 10 | ppm |

DC Electrical Specifications (V_{DD} = 2.5V ± 5%, T_A = -40°C to +85°C)

| Parameter | Description | Condition | Min. | Typ. | Max. | Unit |
|------------------|-------------------------------------|-----------------------------------|------|------|-----------------------|------|
| V _{IL} | Input Voltage, Low | LVC MOS | - | - | 0.7 | V |
| V _{IH} | Input Voltage, High | LVC MOS | 1.7 | - | V _{DD} + 0.3 | V |
| V _{PP} | Peak-Peak Input Voltage | LVPECL | 250 | - | 1000 | mV |
| V _{CMR} | Common Mode Range ^[4] | LVPECL | 1.0 | - | V _{DD} - 0.6 | V |
| V _{OL} | Output Voltage, Low ^[5] | I _{OL} = 15 mA | - | - | 0.6 | V |
| V _{OH} | Output Voltage, High ^[5] | I _{OH} = -15 mA | 1.8 | - | - | V |
| I _{IL} | Input Current, Low ^[6] | V _{IL} = V _{SS} | - | - | -100 | μA |
| I _{IH} | Input Current, High ^[6] | V _{IL} = V _{DD} | - | - | 100 | μA |
| I _{DDA} | PLL Supply Current | AVDD only | - | - | 7 | mA |
| I _{DDQ} | Quiescent Supply Current | All VDD pins except AVDD | - | - | 4 | mA |
| I _{DD} | Dynamic Supply Current | Outputs loaded @ 100 MHz | - | 245 | - | mA |
| C _{IN} | Input Pin Capacitance | | - | 4 | - | pF |
| Z _{OUT} | Output Impedance | | 14 | 18 | 22 | Ω |

DC Electrical Specifications (V_{DD} = 3.3V ± 5%, T_A = -40°C to +85°C)

| Parameter | Description | Condition | Min. | Typ. | Max. | Unit |
|------------------|-------------------------------------|--------------------------|------|------|-----------------------|------|
| V _{IL} | Input Voltage, Low | LVC MOS | - | - | 0.8 | V |
| V _{IH} | Input Voltage, High | LVC MOS | 2.0 | - | V _{DD} + 0.3 | V |
| V _{PP} | Peak-Peak Input Voltage | LVPECL | 250 | - | 1000 | mV |
| V _{CMR} | Common Mode Range ^[4] | LVPECL | 1.0 | - | V _{DD} - 0.6 | V |
| V _{OL} | Output Voltage, Low ^[5] | I _{OL} = 24 mA | - | - | 0.55 | V |
| | | I _{OL} = 12 mA | - | - | 0.30 | |
| V _{OH} | Output Voltage, High ^[5] | I _{OH} = -24 mA | 2.4 | - | - | V |

Notes:

- V_{CMR} (DC) is the crossing point of the differential input signal. Normal operation is obtained when the crossing point is within the V_{CMR} range and the input swing is within the V_{PP} (DC) specification.
- Driving one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, each output drives up to two 50Ω series terminated transmission lines.
- Inputs have pull-up or pull-down resistors that affect the input current.

DC Electrical Specifications ($V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$) (continued)

| Parameter | Description | Condition | Min. | Typ. | Max. | Unit |
|-----------|------------------------------------|--------------------------|------|------|------|---------------|
| I_{IL} | Input Current, Low ^[6] | $V_{IL} = V_{SS}$ | – | – | –100 | μA |
| I_{IH} | Input Current, High ^[6] | $V_{IL} = V_{DD}$ | – | – | 100 | μA |
| I_{DDA} | PLL Supply Current | AVDD only | – | – | 7 | mA |
| I_{DDQ} | Quiescent Supply Current | All VDD pins except AVDD | – | – | 4 | mA |
| I_{DD} | Dynamic Supply Current | Outputs loaded @ 100 MHz | – | 330 | – | mA |
| C_{IN} | Input Pin Capacitance | | – | 4 | – | pF |
| Z_{OUT} | Output Impedance | | 12 | 15 | 18 | Ω |

AC Electrical Specifications ($V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$) ^[7]

| Parameter | Description | Condition | Min. | Typ. | Max. | Unit |
|-----------------|--|--------------------------------|------|-----------|----------------|------|
| f_{VCO} | VCO Frequency | | 200 | – | 400 | MHz |
| f_{in} | Input Frequency | ± 2 Feedback | 100 | – | 200 | MHz |
| | | ± 4 Feedback | 50 | – | 100 | |
| | | Bypass mode (BYPASS# = 0) | 0 | – | 200 | |
| f_{refDC} | Input Duty Cycle | | 40 | – | 60 | % |
| V_{PP} | Peak-Peak Input Voltage | LVPECL | 500 | – | 1000 | mV |
| V_{CMR} | Common Mode Range ^[8] | LVPECL | 1.2 | – | $V_{DD} - 0.6$ | V |
| f_{MAX} | Maximum Output Frequency | ± 2 Output | 100 | – | 200 | MHz |
| | | ± 4 Output | 50 | – | 100 | |
| DC | Output Duty Cycle | | 45 | – | 55 | % |
| t_r, t_f | Output Rise/Fall times | 0.6V to 1.8V | 0.1 | – | 1.0 | ns |
| $t_{(\phi)}$ | Propagation Delay (static phase offset) | PCLK to FB_IN, same VDD | –200 | – | 225 | ps |
| t_{PD} | Propagation Delay (PLL and divider bypass) | PCLK to Q0 – Q9 BYPASS# = 0 | 4.1 | 5.5 | 6.9 | ns |
| $t_{sk(O)}$ | Output-to-Output Skew | | – | – | 150 | ps |
| $t_{PLZ, HZ}$ | Output Disable Time | | – | – | 6 | ns |
| $t_{PZL, ZH}$ | Output Enable Time | | – | – | 6 | ns |
| BW | PLL Closed Loop Bandwidth (–3dB) | ± 2 Feedback | – | 1.9 – 2.2 | – | MHz |
| | | ± 4 Feedback | – | 1.8 – 2.1 | – | |
| $t_{JIT(CC)}$ | Cycle-to-Cycle Jitter | | – | – | 100 | ps |
| $t_{JIT(PER)}$ | Period Jitter | | – | – | 75 | ps |
| $t_{JIT(\phi)}$ | I/O Phase Jitter | I/O same VDD | – | – | 150 | ps |
| t_{LOCK} | Maximum PLL Lock Time | | – | – | 1 | ms |

AC Electrical Specifications ($V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$) ^[7]

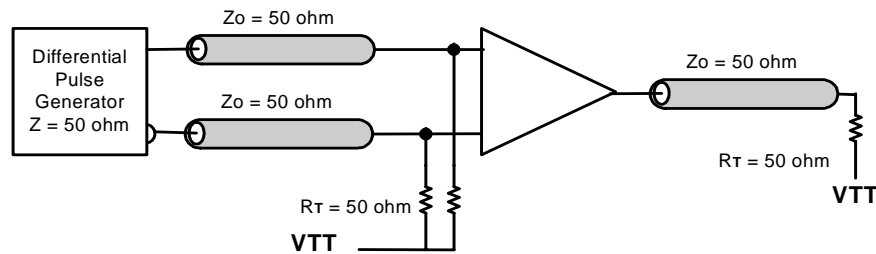
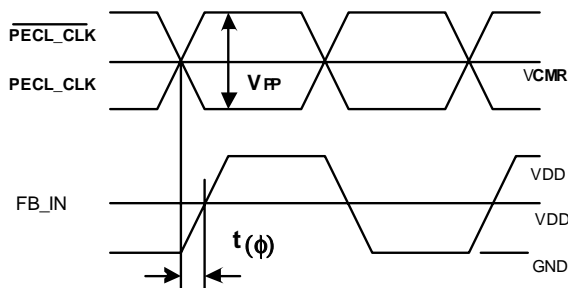
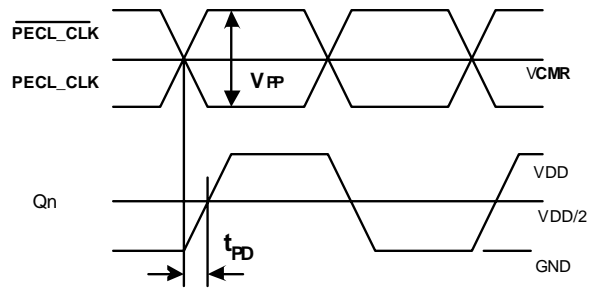
| Parameter | Description | Condition | Min. | Typ. | Max. | Unit |
|-----------|-----------------|---------------------------|------|------|------|------|
| f_{VCO} | VCO Frequency | | 200 | – | 500 | MHz |
| f_{in} | Input Frequency | ± 2 Feedback | 100 | – | 200 | MHz |
| | | ± 4 Feedback | 50 | – | 125 | |
| | | Bypass mode (BYPASS# = 0) | 0 | – | 200 | |

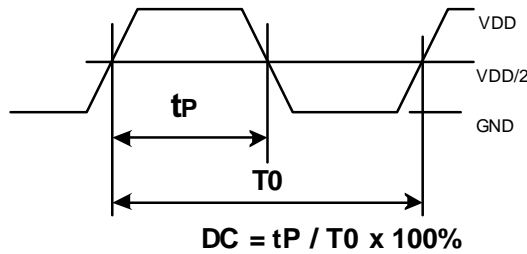
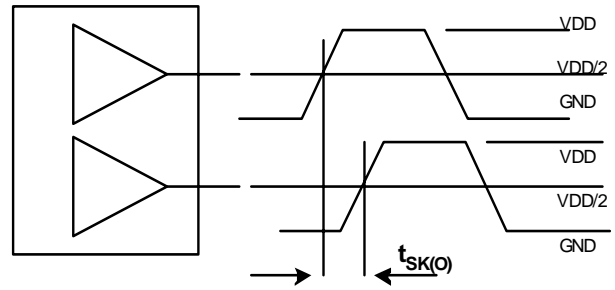
Notes:

- AC characteristics apply for parallel output termination of 50Ω to V_{TT} . Parameters are guaranteed by characterization and are not 100% tested.
- V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\phi)}$.

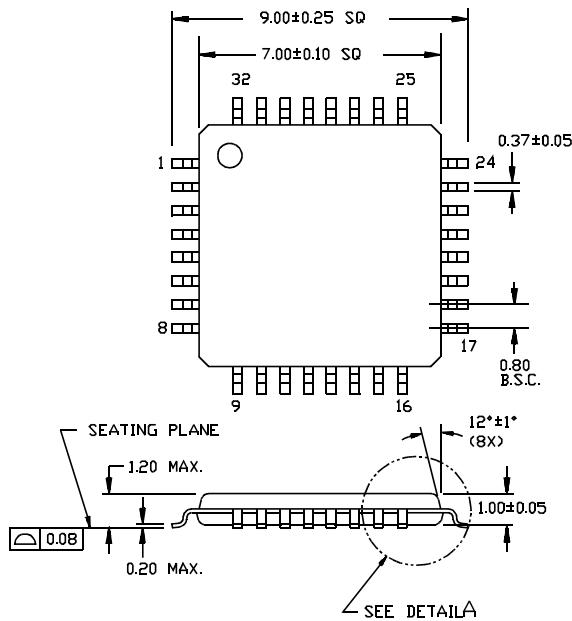
AC Electrical Specifications ($V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$) (continued)^[7]

| Parameter | Description | Condition | Min. | Typ. | Max. | Unit |
|-----------------|--|--------------------------------|------|-----------|----------------|------|
| f_{refDC} | Input Duty Cycle | | 40 | – | 60 | % |
| V_{PP} | Peak-Peak Input Voltage | LVPECL | 500 | – | 1000 | mV |
| V_{CMR} | Common Mode Range ^[8] | LVPECL | 1.2 | – | $V_{DD} - 0.9$ | V |
| f_{MAX} | Maximum Output Frequency | +2 Output | 100 | – | 200 | MHz |
| | | +4 Output | 50 | – | 125 | |
| DC | Output Duty Cycle | | 45 | – | 55 | % |
| t_r, t_f | Output Rise/Fall times | 0.55V to 2.4V | 0.1 | – | 1.0 | ns |
| $t_{(\phi)}$ | Propagation Delay (static phase offset) | PCLK to FB_IN, same VDD | –200 | – | 225 | ps |
| t_{PD} | Propagation Delay (PLL and divider bypass) | PCLK to Q0 – Q9 BYPASS# = 0 | 3.6 | 4.8 | 6.0 | ns |
| $t_{sk(O)}$ | Output-to-Output Skew | | – | – | 150 | ps |
| $t_{PLZ, HZ}$ | Output Disable Time | | – | – | 6 | ns |
| $t_{PZL, ZH}$ | Output Enable Time | | – | – | 6 | ns |
| BW | PLL Closed Loop Bandwidth (–3dB) | +2 Feedback | – | 1.9 – 2.2 | – | MHz |
| | | +4 Feedback | – | 1.8 – 2.1 | – | |
| $t_{JIT(CC)}$ | Cycle-to-Cycle Jitter | | – | – | 100 | ps |
| $t_{JIT(PER)}$ | Period Jitter | | – | – | 75 | ps |
| $t_{JIT(\phi)}$ | I/O Phase Jitter | I/O same VDD | – | – | 150 | ps |
| t_{LOCK} | Maximum PLL Lock Time | | – | – | 1 | ms |

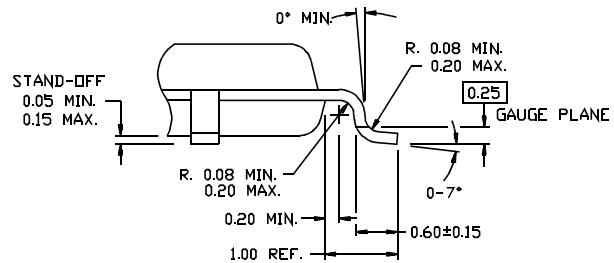

Figure 1. AC Test Reference for $V_{DD} = 3.3V / 2.5V$

Figure 2. Propagation Delay $t_{(\phi)}$, Static Phase Offset

Figure 3. Propagation Delay t_{PD} , PLL Bypass


Figure 4. Output Duty Cycle (DC)

Figure 5. Output-to-Output Skew $t_{sk(O)}$
Ordering Information

| Part Number | Package Type | Product Flow |
|-------------|-----------------------------|----------------------------|
| CY29658AI | 32-pin TQFP | Industrial, -40°C to +85°C |
| CY29658AIT | 32-pin TQFP – Tape and Reel | Industrial, -40°C to 85°C |

Package Drawing and Dimension
32-lead Thin Plastic Quad Flatpack 7 x 7 x 1.0mm A32


DIMENSIONS ARE IN MILLIMETERS


DETAIL A

51-85063-B

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Document History Page

| Document Title: CY29658 2.5V or 3.3V 200-MHz 10-Output Zero Delay Buffer Document Number: 38-07478 | | | | |
|---|----------------|-------------------|------------------------|------------------------------|
| Rev. | ECN No. | Issue Date | Orig. of Change | Description of Change |
| ** | 126716 | 05/19/03 | RGL | New Data Sheet |