# CYK001M16ZCCA
# MoBL3™

# 16-Mbit (1M x 16) Pseudo Static RAM

## Features

- **Wide voltage range: 2.70V–3.30V**
- **Access Time: 55 ns, 70 ns**
- **Ultra-low active power**
  - **Typical active current: 3 mA @ f = 1 MHz**
  - **Typical active current: 13 mA @ f = $f_{max}$**
- **Ultra low standby power**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Deep Sleep Mode**
- **Offered in a 48-ball BGA Package**

## Functional Description

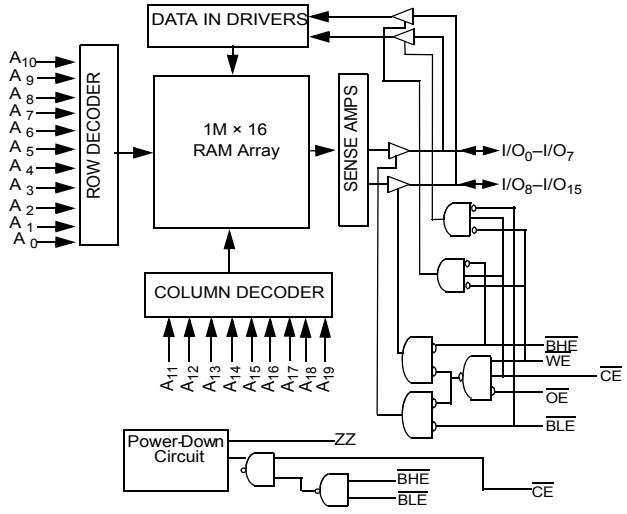
The CYK001M16ZCCAU is a high-performance CMOS Pseudo static RAM organized as 1M words by 16 bits that supports an asynchronous memory interface. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device can be put into standby mode when deselected (CE HIGH or both BHE and BLE are HIGH). The input/output pins ($I/O_0$ through $I/O_{15}$) are placed in a high-impedance state when: deselected (CE HIGH), outputs are disabled (OE HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or during a write operation (CE LOW and WE LOW).

Writing to the device is accomplished by asserting Chip Enable (CE) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins ($I/O_0$ through $I/O_7$), is written into the location specified on the address pins ($A_0$ through $A_{17}$). If Byte High Enable (BHE) is LOW, then data from I/O pins ($I/O_8$ through $I/O_{15}$) is written into the location specified on the address pins ($A_0$ through $A_{17}$).

Reading from the device is accomplished by asserting Chip Enable (CE) and Output Enable (OE) inputs LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on $I/O_0$ to $I/O_7$. If Byte High Enable (BHE) is LOW, then data from memory will appear on $I/O_8$ to $I/O_{15}$. Refer to the truth table for a complete description of read and write modes.

This device incorporates a Low Power mode wherein data integrity is not guaranteed, but Power Consumption reduces to less than 100 µW. This mode (Deep Sleep Mode) is enabled by driving ZZ LOW.See the Truth Table for a complete description of Read, Write, and Deep Sleep mode.

## Logic Block Diagram

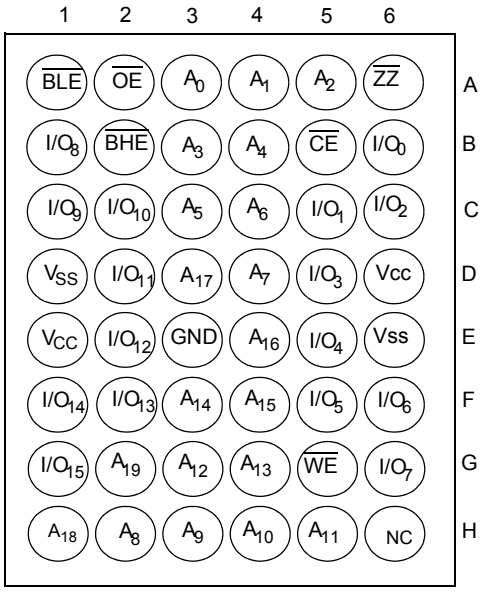



**Note:**
1. For best-practice recommendations, please refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com.

## Pin Configuration[2, 3, 4]

**FBGA**

**Top View**




## Product Portfolio[5]

| Product | $V_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Operating $I_{CC}$(mA) | | | | Standby $I_{SB2}$(μA) | |
| | | | | | f = 1MHz | | f = $f_{max}$ | | | |
| | Min. | Typ.[5] | Max. | | Typ.[5] | Max. | Typ.[5] | Max. | Typ.[5] | Max. |
| CYK001M16ZCCAU | 2.70 | 3.0 | 3.30 | 55 | 3 | 5 | 13 | 22 | 80 | 150 |
| | | | | 70 | | | | 17 | | |

**Notes:**
2. DNU pins have to be left floating.
3. Ball H6 can be used to upgrade to 32M density.
4. NC “no connect”—not connected internally to the die.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25°C$.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to + 150°C

Ambient Temperature with Power Applied.....–55°C to + 125°C

Supply Voltage to Ground Potential ..... –0.4V to 4.6V

DC Voltage Applied to Outputs in High Z State[6, 7, 8] .....–0.4V to 3.7V

DC Input Voltage[6, 7, 8].....–0.4V to 3.7V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... > 200 mA

## Operating Range

| Device | Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|---|
| CYK001M16ZCCA | Industrial | –25°C to +85°C | 2.70V to 3.30V |

## DC Electrical Characteristics (Over the Operating Range)

| Parameter | Description | Test Conditions | | CYK001M16ZCCAU-55 | | | CYK001M16ZCCAU-70 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ.[5] | Max. | Min. | Typ.[5] | Max. | |
| $V_{CC}$ | Supply Voltage | | | 2.7 | 3.0 | 3.3 | 2.7 | | 3.3 | V |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –-0.1 mA | | $V_{CC}$ – 0.4 | | | $V_{CC}$ – 0.4 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 0.1mA | | | | 0.4 | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | $V_{CC}$= 2.7V to 3.3V | | 0.8 * $V_{CC}$ | | $V_{CC}$+ 0.4V | 0.8 * $V_{CC}$ | | $V_{CC}$+ 0.4V | V |
| $V_{IL}$ | Input LOW Voltage | | | –0.4 | | 0.4 | -0.4 | | 0.4 | V |
| $I_{IX}$ | Input Leakage Current | GND ≤ $V_{IN}$ ≤ $V_{CC}$ | | –1 | | +1 | –1 | | +1 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_{OUT}$ ≤ $V_{CC}$, Output Disabled | | –1 | | +1 | –1 | | +1 | µA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | f = $f_{MAX}$ = 1/$t_{RC}$ | $V_{CC}$ = $V_{CCmax}$ $I_{OUT}$ = 0 mA CMOS levels | | 13 | 22 | | 13 | 17 | mA |
| | | f = 1 MHz | | | 3 | 5 | | 3 | 5 | mA |
| $I_{SB1}$ | Automatic CE Power-Down Current — CMOS Inputs | $\overline{CE}$ ≥ $V_{CC}$–0.2V $V_{IN}$ ≥ $V_{CC}$–0.2V, $V_{IN}$ ≤ 0.2V) f = $f_{MAX}$ (Address and Data Only), f = 0 ($\overline{OE}$, WE, $\overline{BHE}$ and $\overline{BLE}$), $V_{CC}$ = 3.30V | $V_{CC}$ = 3.3V | | 100 | 525 | | 100 | 525 | µA |
| $I_{SB2}$ | Automatic CE Power-Down Current — CMOS Inputs | $\overline{CE}$ ≥ $V_{CC}$ – 0.2V $V_{IN}$ ≥ $V_{CC}$ – 0.2V or $V_{IN}$ ≤ 0.2V, f = 0, $V_{CC}$ = 3.30V | $V_{CC}$ = 3.3V | | 80 | 150 | | 80 | 150 | µA |
| $I_{ZZ}$ | Deep Sleep Current | $V_{CC}$ = $V_{CCMAX}$; ZZ = LOW | | | | 50 | | | 50 | µA |

**Notes:**
6. $V_{IL(MIN)}$ = –0.5V for pulse durations less than 20 ns.
7. $V_{IH(Max)}$ = Vcc + 0.5V for pulse durations less than 20 ns.
8. Overshoot and undershoot specifications are characterized and are not 100% tested.

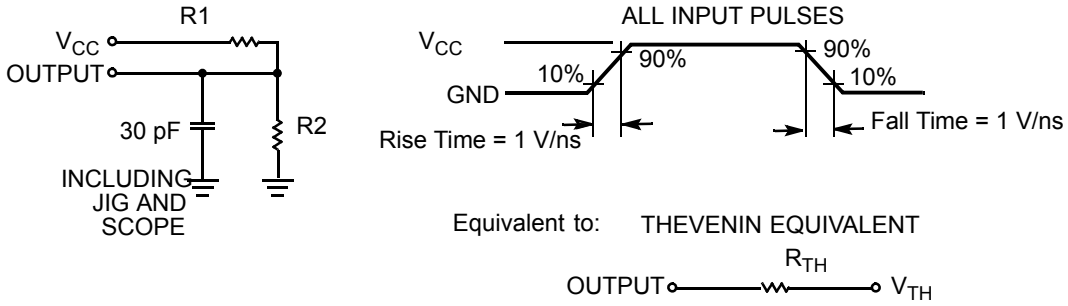
## Capacitance[9]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = $V_{CC(typ)}$ | 8 | pF |
| $C_{OUT}$ | Output Capacitance | | 8 | pF |

## Thermal Resistance[9]

| Parameter | Description | Test Conditions | BGA | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51. | 55 | °C/W |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case) | | 17 | °C/W |

## AC Test Loads and Waveforms




| Parameters | 3.0V $V_{CC}$ | Unit |
|---|---|---|
| R1 | 22000 | Ω |
| R2 | 22000 | Ω |
| $R_{TH}$ | 11000 | Ω |
| $V_{TH}$ | 1.50 | V |

**Note:**
9. Tested initially and after any design or process changes that may affect these parameters.

## Switching Characteristics Over the Operating Range[10, 11, 12, 13, 14]

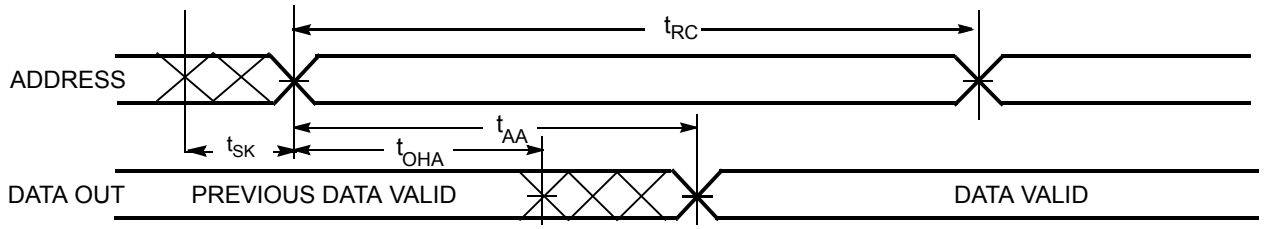
| Parameter | Description | 55 ns[14] | | 70 ns | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| **Read Cycle** | | | | | | |
| $t_{RC}$ | Read Cycle Time | 55[14] | | 70 | | ns |
| $t_{AA}$ | Address to Data Valid | | 55 | | 70 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 5 | | 5 | | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to Data Valid | | 55 | | 70 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 25 | | 35 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to LOW Z[11, 13] | 5 | | 5 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z[11, 13] | | 25 | | 25 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to Low Z[11, 13] | 2 | | 5 | | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to High Z[11, 13] | | 25 | | 25 | ns |
| $t_{DBE}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to Data Valid | | 55 | | 70 | ns |
| $t_{LZBE}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to Low Z[11, 13] | 5 | | 5 | | ns |
| $t_{HZBE}$ | $\overline{BLE}$/$\overline{BHE}$ HIGH to HIGH Z[11, 13] | | 10 | | 25 | ns |
| $t_{SK}$[14] | Address Skew | | 0 | | 10 | ns |
| **Write Cycle**[12] | | | | | | |
| $t_{WC}$ | Write Cycle Time | 55 | | 70 | | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to Write End | 45 | | 60 | | ns |
| $t_{AW}$ | Address Set-up to Write End | 45 | | 60 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | 0 | | ns |
| $t_{SA}$ | Address Set-up to Write Start | 0 | | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 40 | | 45 | | ns |
| $t_{BW}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to Write End | 50 | | 60 | | ns |
| $t_{SD}$ | Data Set-up to Write End | 25 | | 45 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | 0 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High-Z[11, 13] | | 25 | | 25 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low-Z[11, 13] | 5 | | 5 | | ns |

**Notes:**

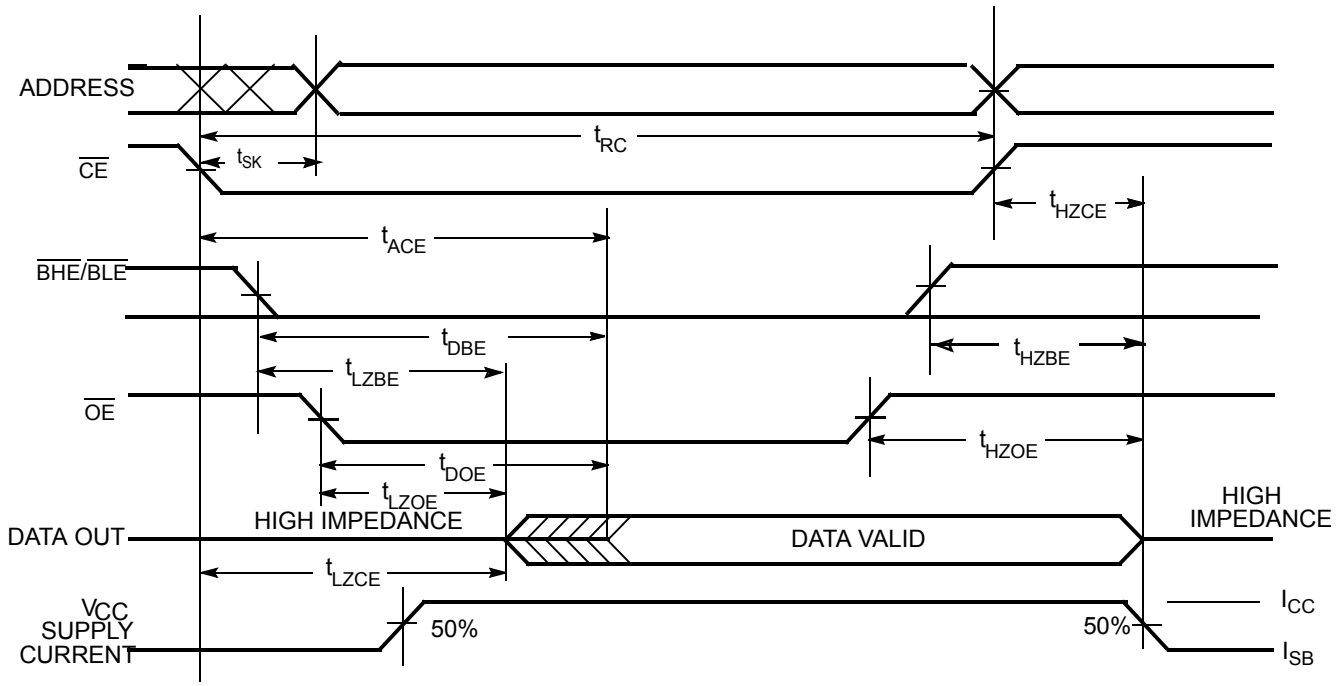
10. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0V to $V_{CC(typ.)}$, and output loading of the specified $I_{OL}/I_{OH}$ as shown in the "AC Test Loads and Waveforms" section.
11. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high impedence state.
12. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE}$ = $V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
13. High-Z and Low-Z parameters are characterized and are not 100% tested.
14. To achieve 55-ns performance, the read access should be $\overline{CE}$ controlled. In this case $t_{ACE}$ is the critical parameter and $t_{SK}$ is satisfied when the addresses are stable prior to chip enable going active. For the 70-ns cycle, the addresses must be stable within 10 ns after the start of the read cycle

## Switching Waveforms

### Read Cycle 1 (Address Transition Controlled)[14, 15, 16]



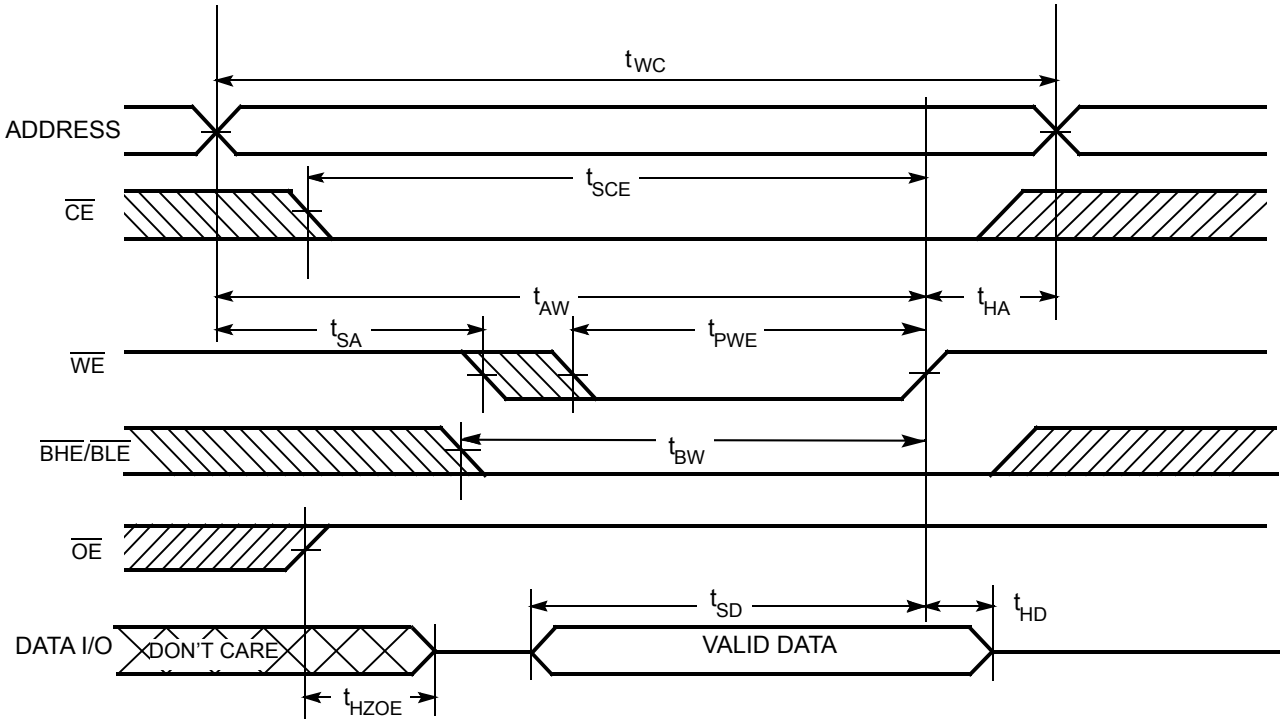

### Read Cycle 2 ($\overline{OE}$ Controlled)[14, 16]



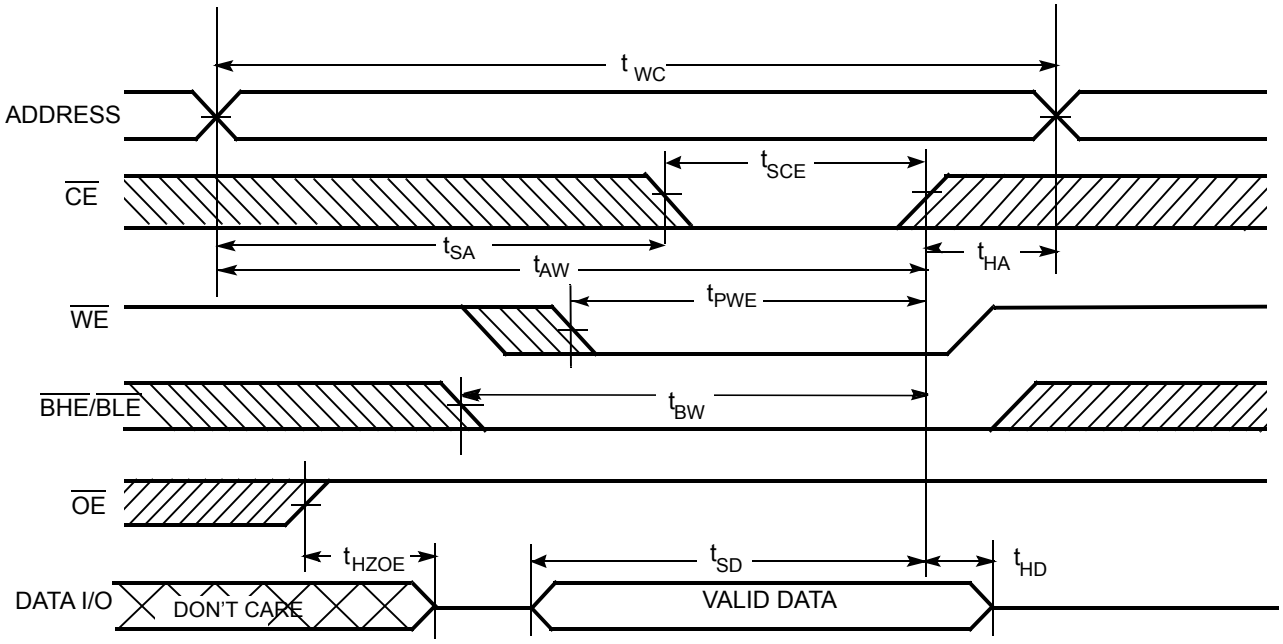

**Notes:**
15. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = $V_{IL}$.
16. $\overline{WE}$ is HIGH for Read Cycle.

## Switching Waveforms (continued)

### Write Cycle 1 ($\overline{WE}$ Controlled)[12, 13, 17, 18, 19]



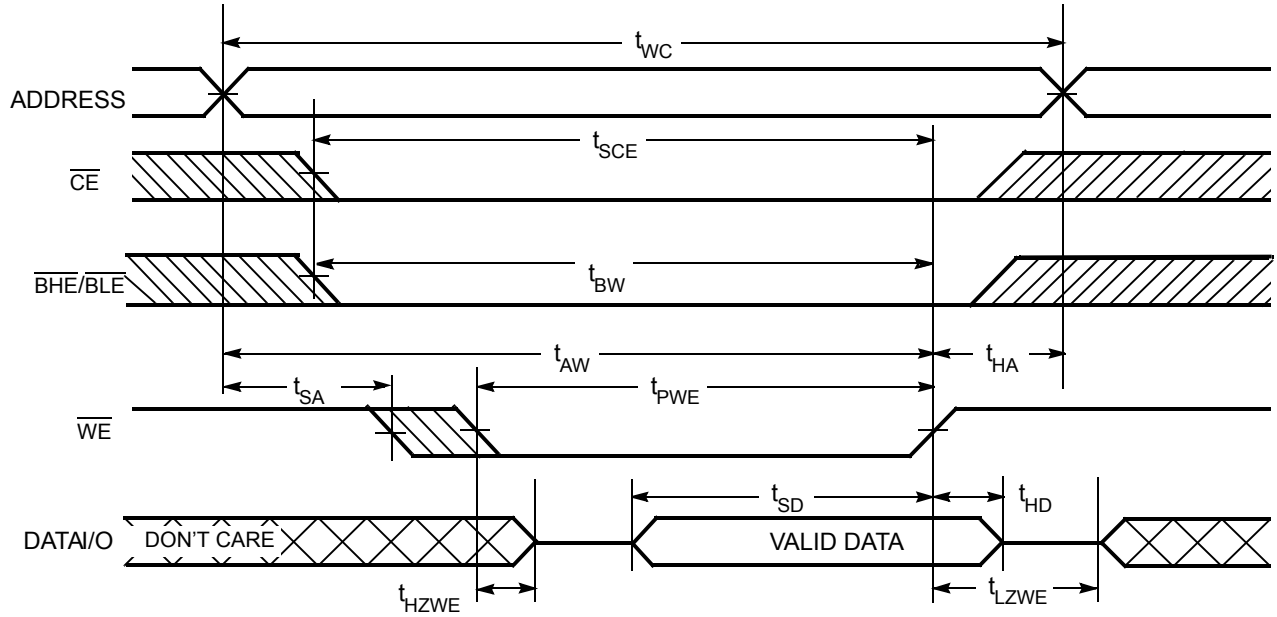

### Write Cycle 2 ($\overline{CE}$ Controlled)[12, 13, 17, 18, 19]



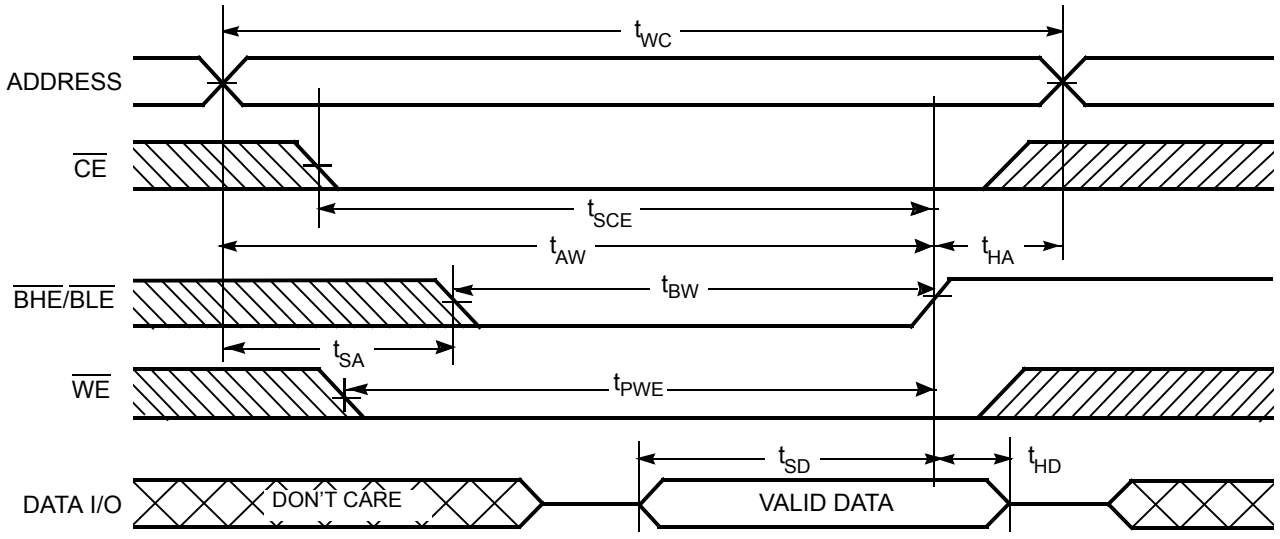

**Notes:**
17. Data I/O is high impedance if $\overline{OE} \geq V_{IH}$.
18. If Chip Enable goes INACTIVE with $\overline{WE} = V_{IH}$, the output remains in a high-impedance state.
19. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

## Switching Waveforms (continued)

**Write Cycle 3 (WE Controlled, OE LOW)**[18, 19]



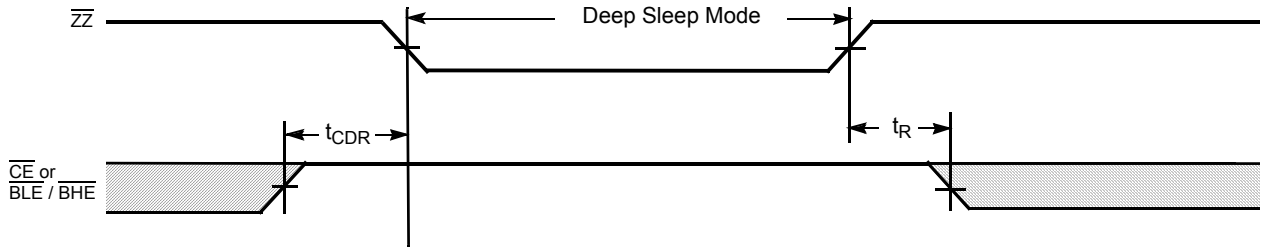

**Write Cycle 4 (BHE/BLE Controlled, OE LOW)**[18, 19]



## Deep Sleep Mode

This mode can be used to lower the power consumption of the PSRAM in an application. In this mode, the data integrity of the PSRAM is not guaranteed. Deep Sleep Mode can be enabled by driving $\overline{ZZ}$ LOW. The device stays in the deep sleep mode until $\overline{ZZ}$ is driven HIGH.

## Deep Sleep Mode—Entry/Exit[20]




## Deep Sleep Access Timings[21, 22]

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{CDR}$ | Chip Deselect to $\overline{ZZ}$ LOW | 0 | | ns |
| $t_R$ | Operation Recovery Time | | 200 | µs |

## Truth Table[23]

| $\overline{ZZ}$ | $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|---|---|---|
| H | H | X | X | X | X | High Z | Deselect/Power-down | Standby ($I_{SB}$) |
| H | X | X | X | H | H | High Z | Deselect/Power-down | Standby ($I_{SB}$) |
| H | L | H | L | L | L | Data Out ($I/O_0$–$I/O_{15}$) | Read (Upper Byte and Lower Byte) | Active ($I_{CC}$) |
| H | L | H | L | H | L | Data Out ($I/O_0$–$I/O_7$); $I/O_8$–$I/O_{15}$ in High Z | Read (Lower Byte only) | Active ($I_{CC}$) |
| H | L | H | L | L | H | Data Out ($I/O_8$–$I/O_{15}$); $I/O_0$–$I/O_7$ in High Z | Read (Upper Byte only) | Active ($I_{CC}$) |
| H | L | H | H | L | L | High Z | Output Disabled | Active ($I_{CC}$) |
| H | L | H | H | H | L | High Z | Output Disabled | Active ($I_{CC}$) |
| H | L | H | H | L | H | High Z | Output Disabled | Active ($I_{CC}$) |
| H | L | L | X | L | L | Data In ($I/O_0$–$I/O_{15}$) | Write (Upper Byte and Lower Byte) | Active ($I_{CC}$) |
| H | L | L | X | H | L | Data In ($I/O_0$–$I/O_7$); $I/O_8$–$I/O_{15}$ in High Z | Write (Lower Byte Only) | Active ($I_{CC}$) |
| H | L | L | X | L | H | Data In ($I/O_8$–$I/O_{15}$); $I/O_0$ –$I/O_7$ in High Z | Write (Upper Byte Only) | Active ($I_{CC}$) |
| L | H | X | X | H | H | High Z | Deep Power-down | Deep Sleep ($I_{ZZ}$) |

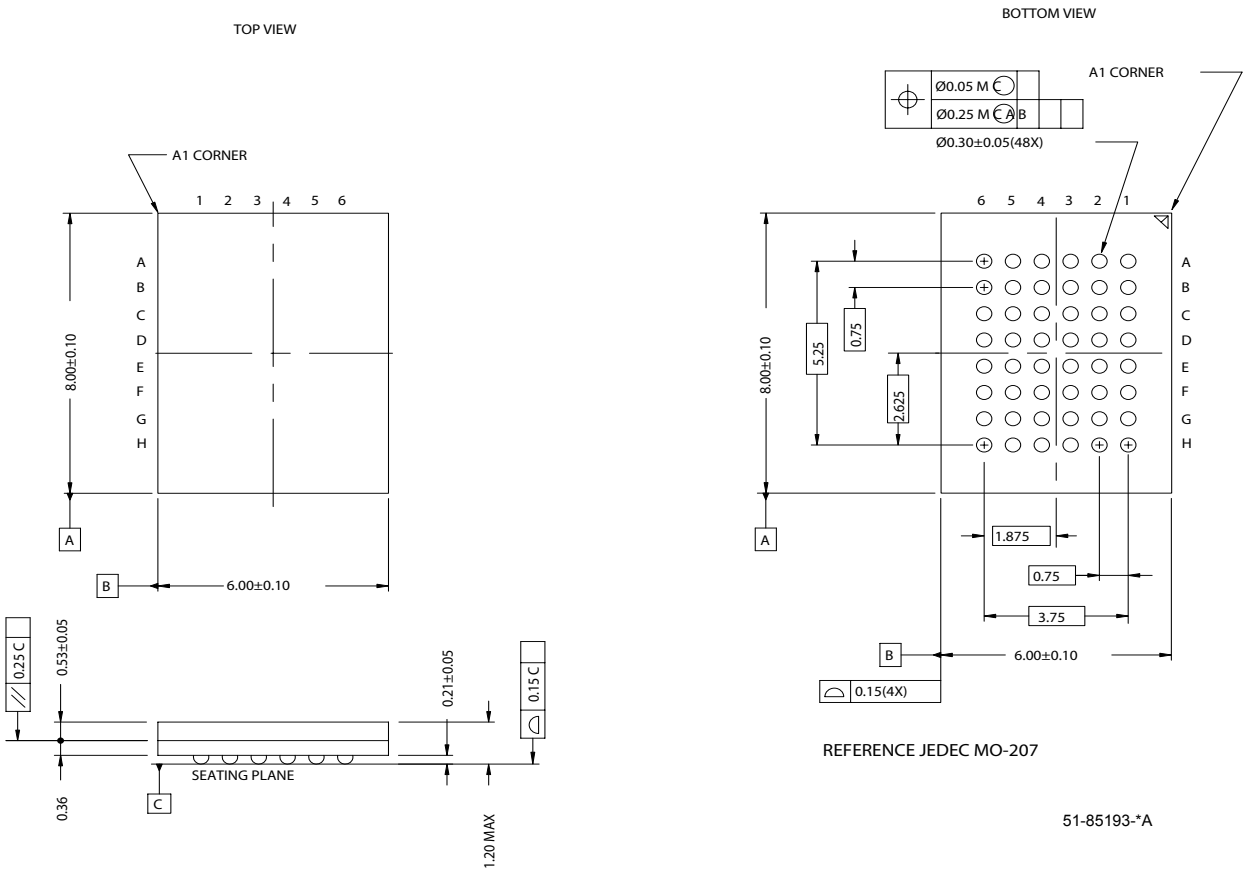
**Notes:**
20. $\overline{OE}$ and the data pins are in a “don’t care” state while the device is in Deep Sleep Mode.
21. All other timing parameters are as shown in the switching characteristics section.
22. $t_R$ applies only in the Deep Sleep Mode.
23. H = Logic HIGH, L = Logic LOW, X = Don’t Care.

## Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 55 | CYK001M16ZCCAU-55BAI | BA48K | 48-ball Fine Pitch BGA (6 mm × 8mm × 1.2 mm) | Industrial |
| 70 | CYK001M16ZCCAU-70BAI | BA48K | 48-ball Fine Pitch BGA (6 mm × 8mm × 1.2 mm) | Industrial |

## Package Diagram

**48-Lead FBGA (6 x 8 x 1.2 mm) BA48K**



## Document History Page

| Document Title: CYK001M16ZCCA MoBL3™ 16-Mbit (1M x 16) Pseudo Static RAM<br>Document Number: 38-05454 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 132407 | 01/27/04 | AWK | New Data Sheet |
| *A | 220121 | See ECN | REF | Changed the datasheet from AdvanceInformation to Final<br>Added 55-ns speed bin and address skew restriction for 55-ns speed bin.<br>Changed Izz from 30 μA to 50 μA. |
| *B | 230851 | See ECN | AJU | Changed ball A6 from NC to $\overline{ZZ}$<br>Modified ordering code in “Ordering Information” table on page 10<br>Replaced package diagram<br>Modified MAX limit on DC Input voltage in ‘Maximum Ratings’ section |