

4-Mbit (256K x 16) Static RAM

Features

- Pin equivalent to CY7C1041BV33
- Temperature Ranges
 - Commercial: 0°C to 70°C
 - Industrial: -40°C to 85°C
 - Automotive: -40°C to 125°C
- High speed
 - $t_{AA} = 10$ ns
- Low active power
 - 324 mW (max.)
- 2.0V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE} and \overline{OE} features

Functional Description^[1]

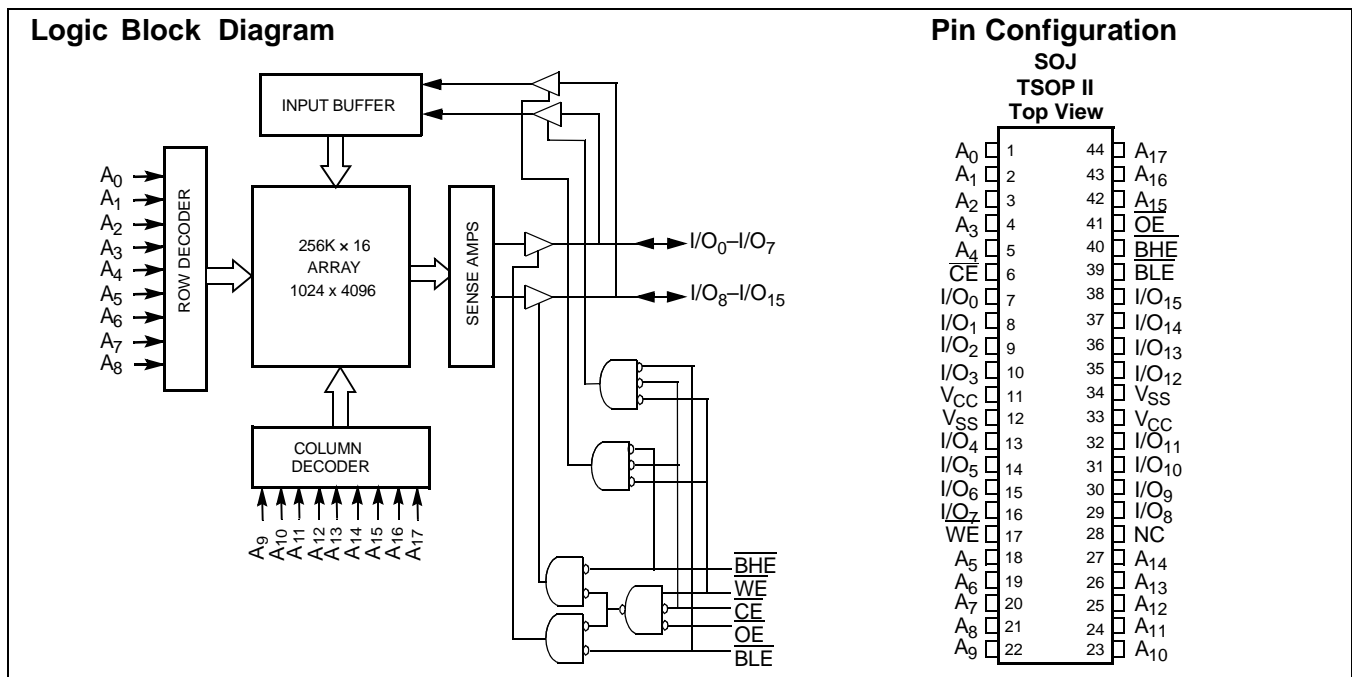
The CY7C1041CV33 is a high-performance CMOS Static RAM organized as 262,144 words by 16 bits.

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte LOW Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_0 – I/O_7), is written into the location specified on the address pins (A_0 – A_{17}). If Byte HIGH Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_8 – I/O_{15}) is written into the location specified on the address pins (A_0 – A_{17}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte LOW Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 – I/O_7 . If Byte HIGH Enable (\overline{BHE}) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the truth table at the back of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O_0 – I/O_{15}) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), the \overline{BHE} and \overline{BLE} are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a Write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY7C1041CV33 is available in a standard 44-pin 400-mil-wide body width SOJ and 44-pin TSOP II package with center power and ground (revolutionary) pinout, as well as a 48-ball fine-pitch ball grid array (FBGA) package.



Notes:

1. For guidelines on SRAM system design, please refer to the "System Design Guidelines" Cypress application note, available on the internet at www.cypress.com.

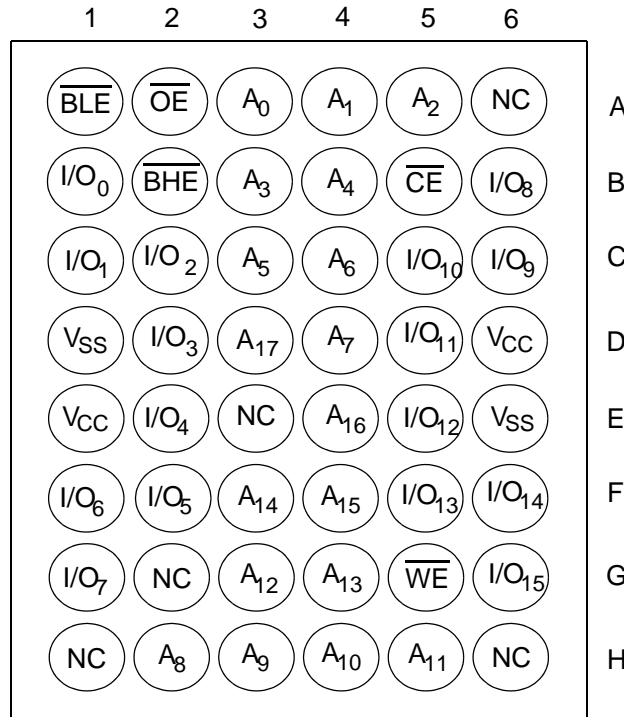
Selection Guide

| | | -8 | -10 | -12 | -15 | -20 | Unit |
|------------------------------|---------------------------|-----|-----|-----|-----|-----|------|
| Maximum Access Time | | 8 | 10 | 12 | 15 | 20 | ns |
| Maximum Operating Current | Commercial | 100 | 90 | 85 | 80 | 75 | mA |
| | Industrial | 110 | 100 | 95 | 90 | 85 | mA |
| | Automotive | - | - | - | - | 90 | mA |
| Maximum CMOS Standby Current | Commercial/ Industrial | 10 | 10 | 10 | 10 | 10 | mA |
| | Automotive | - | - | - | - | 15 | mA |

Shaded areas contain advance information.

Pin Configurations

**48-ball Mini FBGA
(Top View)**



Pin Definitions

| Pin Name | 44-SOJ, 44-TSOP Pin Number | 48-ball FBGA Pin Number | I/O Type | Description |
|---|----------------------------------|---|---------------|---|
| A ₀ -A ₁₇ | 1-5,18-27, 42-44 | A3,A4,A5,B3, B4,C3,C4,D4, H2,H3,H4,H5,G 3,G4,F3,F4,E4, D3 | Input | Address Inputs used to select one of the address locations. |
| I/O ₀ - I/O ₁₅ | 7-10,13-16, 29-32,35-38 | B1,C1,C2,D2,E 2,F2,F1,G1,B6, C6,C5,D5,E5, F5,F6,G6 | Input/Output | Bidirectional Data I/O lines. Used as input or output lines depending on operation |
| NC ^[2] | 28 | A6,E3,G2,H1, H6 | No Connect | No Connects. This pin is not connected to the die |
| $\overline{\text{WE}}$ | 17 | G5 | Input/Control | Write Enable Input, active LOW. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted. |
| $\overline{\text{CE}}$ | 6 | B5 | Input/Control | Chip Enable Input, active LOW. When LOW, selects the chip. When HIGH, deselects the chip. |
| $\overline{\text{BHE}}$, $\overline{\text{BLE}}$ | 39,40 | A1,B2 | Input/Control | Byte Write Select Inputs, active LOW. $\overline{\text{BHE}}$ controls I/O ₇ -I/O ₀ , $\overline{\text{BLE}}$ controls I/O ₁₅ -I/O ₈ . |
| $\overline{\text{OE2}}$ | 41 | A2 | Input/Control | Output Enable, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. |
| V _{SS} | 12,34 | D1,E6 | Ground | Ground for the device. Should be connected to ground of the system. |
| V _{CC} | 11,33 | D6,E1 | Power Supply | Power Supply inputs to the device. |

Note:

2. NC pins are not connected on the die.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[3] -0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State^[3] -0.5V to V_{CC} + 0.5V

DC Input Voltage^[3] -0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) 20 mA

Operating Range

| Range | Ambient Temperature | V _{CC} |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C | 3.3V ± 0.3V |
| Industrial | -40°C to +85°C | |
| Automotive | -40°C to +125°C | |

DC Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | -8 | | -10 | | -12 | | -15 | | -20 | | Unit | |
|--------------------------------|---|---|---------------|-----------------------|------|-----------------------|------|-----------------------|------|-----------------------|------|-----------------------|------|----|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -4.0 mA | 2.4 | | 2.4 | | 2.4 | | 2.4 | | 2.4 | | V | |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 8.0 mA | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | V | |
| V _{IH} | Input HIGH Voltage | | 2.0 | V _{CC} + 0.3 | 2.0 | V _{CC} + 0.3 | 2.0 | V _{CC} + 0.3 | 2.0 | V _{CC} + 0.3 | 2.0 | V _{CC} + 0.3 | V | |
| V _{IL} ^[3] | Input LOW Voltage | | -0.3 | 0.8 | -0.3 | 0.8 | -0.3 | 0.8 | -0.3 | 0.8 | -0.3 | 0.8 | V | |
| I _{IX} | Input Load Current | GND ≤ V _I ≤ V _{CC} | Com'l / Ind'l | -1 | +1 | -1 | +1 | -1 | +1 | -1 | +1 | -1 | +1 | μA |
| | | | Automotive | | | | | | | | | -20 | +20 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled | Com'l / Ind'l | -1 | +1 | -1 | +1 | -1 | +1 | -1 | +1 | -1 | +1 | μA |
| | | | Automotive | | | | | | | | | -20 | +20 | μA |
| I _{CC} | V _{CC} Operating Supply Current | V _{CC} = Max., f = f _{MAX} = 1/t _{RC} | Comm'l | | 100 | | 90 | | 85 | | 80 | | 75 | mA |
| | | | Ind'l | | 110 | | 100 | | 95 | | 90 | | 85 | mA |
| | | | Automotive | | | | | | | | | | | 90 |
| I _{SB1} | Automatic CE Power-down Current — TTL Inputs | Max. V _{CC} , CE ≥ V _{IH} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX} | Com'l / Ind'l | | 40 | | 40 | | 40 | | 40 | | 40 | mA |
| | | | Automotive | | | | | | | | | | 45 | mA |
| I _{SB2} | Automatic CE Power-down Current — CMOS Inputs | Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0 | Com'l / Ind'l | | 10 | | 10 | | 10 | | 10 | | 10 | mA |
| | | | Automotive | | | | | | | | | | 15 | mA |

Shaded areas contain advance information.

Capacitance^[4]

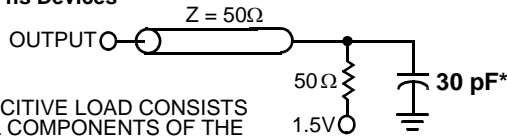
| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|-------------------|--|------|------|
| C _{IN} | Input Capacitance | T _A = 25°C, f = 1 MHz, V _{CC} = 3.3V | 8 | pF |
| C _{OUT} | I/O Capacitance | | 8 | pF |

Thermal Resistance^[4]

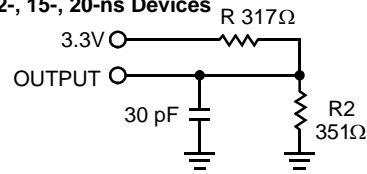
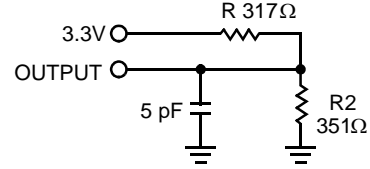
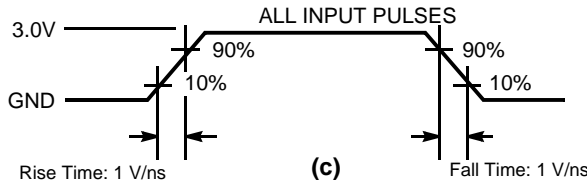
| Parameter | Description | Test Conditions | 44-pin TSOP-II (Non Pb-Free) | 48-FBGA (Non Pb-Free) | Unit |
|-----------------|--|--|------------------------------|-----------------------|------|
| Θ _{JA} | Thermal Resistance (Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51. | 76.85 | 92.78 | °C/W |
| Θ _{JC} | Thermal Resistance (Junction to Case) | | 11.26 | 8.88 | °C/W |

Notes:

- V_{IL} (min.) = -2.0V and V_{IH} (max) = V_{CC} + 0.5V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms^[11]
8-, 10-ns Devices


* CAPACITIVE LOAD CONSISTS OF ALL COMPONENTS OF THE TEST ENVIRONMENT

(a)
12-, 15-, 20-ns Devices

(b)
High-Z Characteristics

(d)

(c)
AC Switching Characteristics^[5] Over the Operating Range

| Parameter | Description | -8 | | -10 | | -12 | | -15 | | -20 | | Unit |
|--------------------------------------|--|------|------|------|------|------|------|------|------|------|------|---------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Read Cycle | | | | | | | | | | | | |
| $t_{power}^{[6]}$ | V_{CC} (typical) to the first access | 1 | | 1 | | 1 | | 1 | | 1 | | μs |
| t_{RC} | Read Cycle Time | 8 | | 10 | | 12 | | 15 | | 20 | | ns |
| t_{AA} | Address to Data Valid | | 8 | | 10 | | 12 | | 15 | | 20 | ns |
| t_{OHA} | Data Hold from Address Change | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| t_{ACE} | \overline{CE} LOW to Data Valid | | 8 | | 10 | | 12 | | 15 | | 20 | ns |
| t_{DOE} | \overline{OE} LOW to Data Valid | | 4 | | 5 | | 6 | | 7 | | 8 | ns |
| t_{LZOE} | \overline{OE} LOW to Low-Z | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{HZOE} | \overline{OE} HIGH to High-Z ^[7, 8] | | 4 | | 5 | | 6 | | 7 | | 8 | ns |
| t_{LZCE} | \overline{CE} LOW to Low-Z ^[8] | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| t_{HZCE} | \overline{CE} HIGH to High-Z ^[7, 8] | | 4 | | 5 | | 6 | | 7 | | 8 | ns |
| t_{PU} | \overline{CE} LOW to Power-Up | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{PD} | \overline{CE} HIGH to Power-Down | | 8 | | 10 | | 12 | | 15 | | 20 | ns |
| t_{DBE} | Byte Enable to Data Valid | | 4 | | 5 | | 6 | | 7 | | 8 | ns |
| t_{LZBE} | Byte Enable to Low-Z | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{HZBE} | Byte Disable to High-Z | | 6 | | 6 | | 6 | | 7 | | 8 | ns |
| Write Cycle^[9, 10] | | | | | | | | | | | | |
| t_{WC} | Write Cycle Time | 8 | | 10 | | 12 | | 15 | | 20 | | ns |
| t_{SCE} | \overline{CE} LOW to Write End | 6 | | 7 | | 8 | | 10 | | 10 | | ns |
| t_{AW} | Address Set-Up to Write End | 6 | | 7 | | 8 | | 10 | | 10 | | ns |

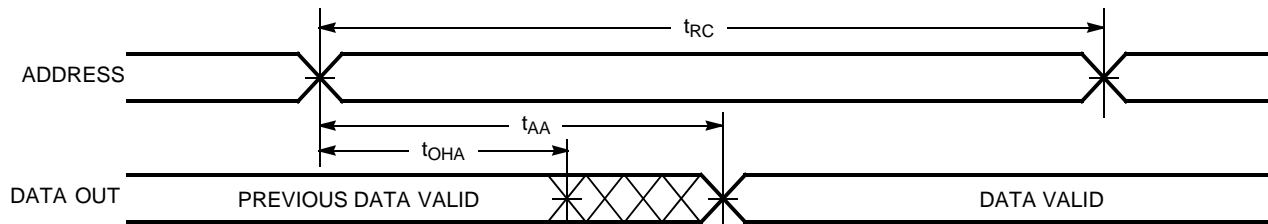
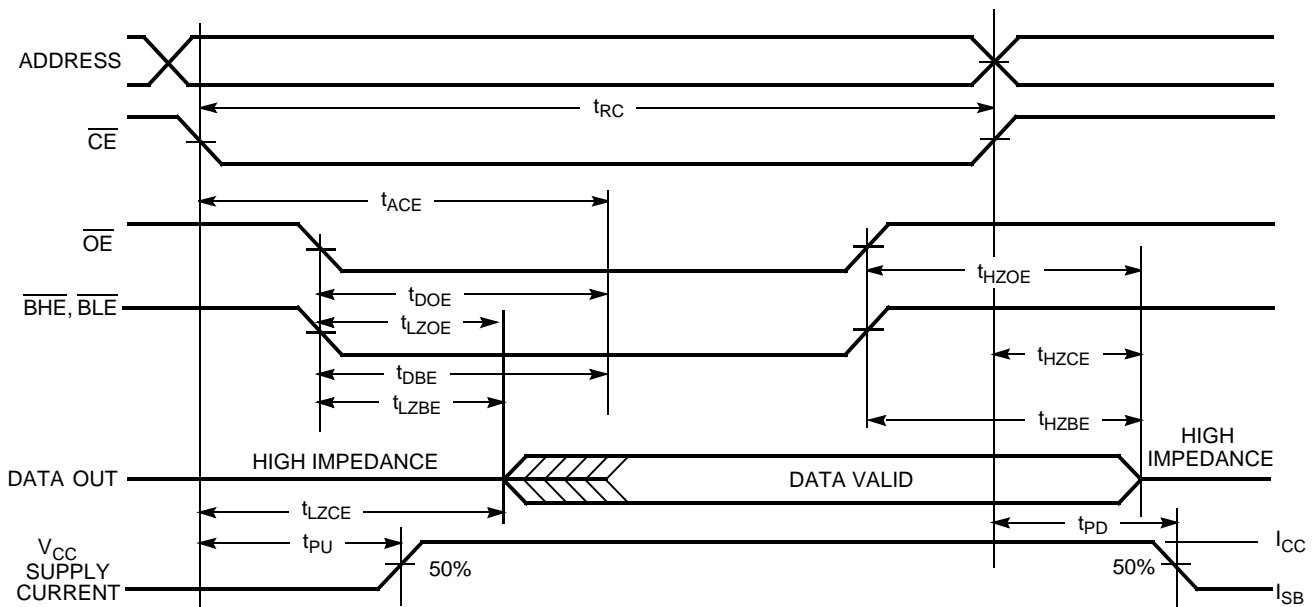
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Notes:

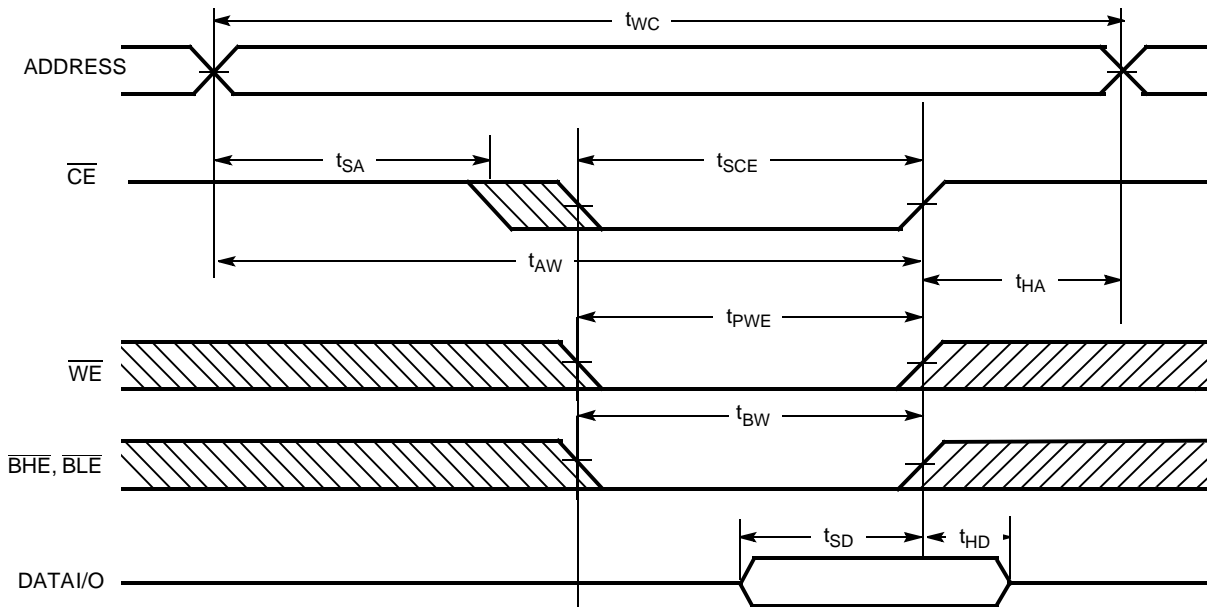
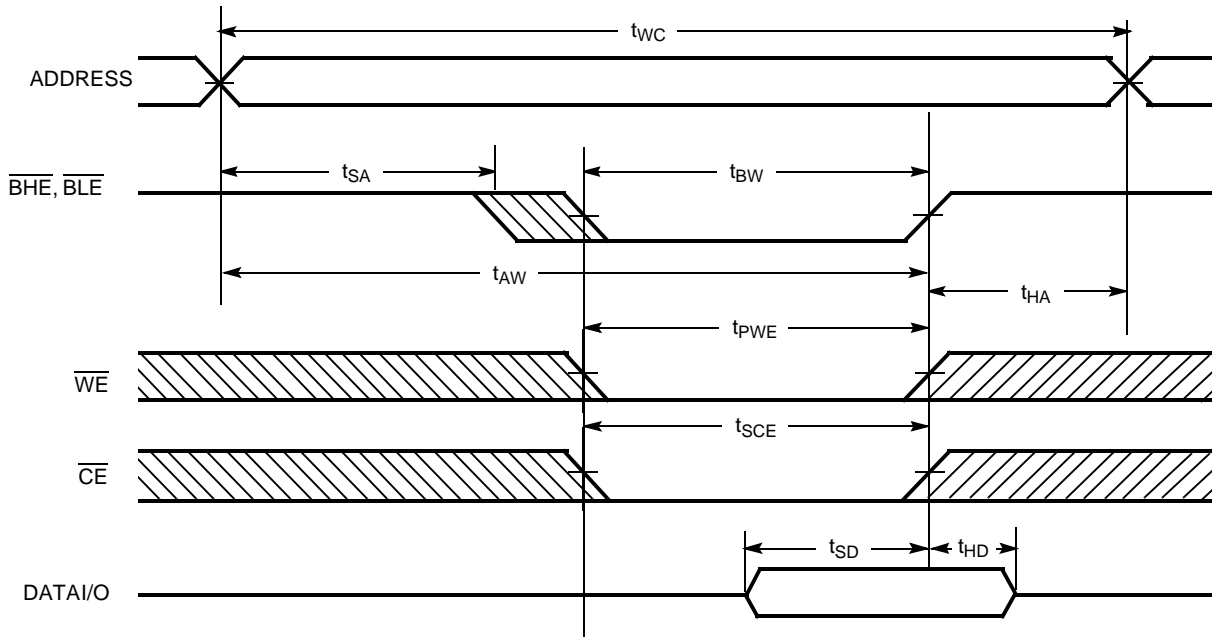
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
- t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal Write time of the memory is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

AC Switching Characteristics^[5] Over the Operating Range (continued)

| Parameter | Description | -8 | | -10 | | -12 | | -15 | | -20 | | Unit |
|------------|---|------|------|------|------|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{HA} | Address Hold from Write End | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{SA} | Address Set-Up to Write Start | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{PWE} | \overline{WE} Pulse Width | 6 | | 7 | | 8 | | 10 | | 10 | | ns |
| t_{SD} | Data Set-Up to Write End | 4 | | 5 | | 6 | | 7 | | 8 | | ns |
| t_{HD} | Data Hold from Write End | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{LZWE} | \overline{WE} HIGH to Low-Z ^[8] | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| t_{HZWE} | \overline{WE} LOW to High-Z ^[7, 8] | | 4 | | 5 | | 6 | | 7 | | 8 | ns |
| t_{BW} | Byte Enable to End of Write | 6 | | 7 | | 8 | | 10 | | 10 | | ns |

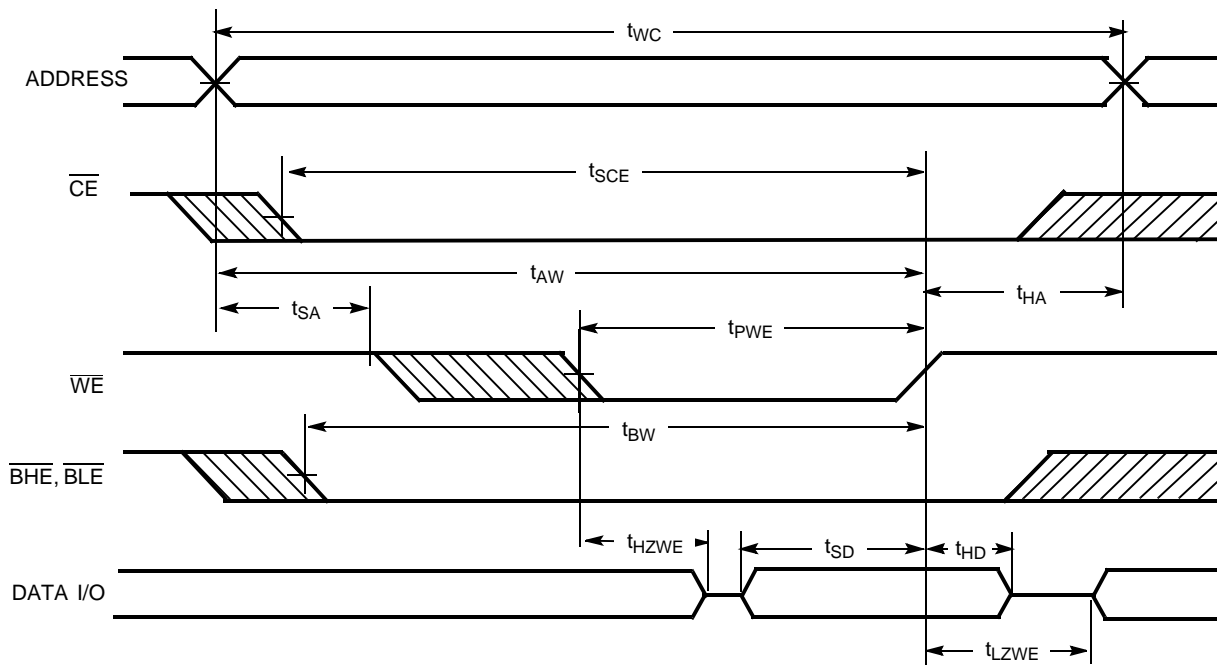
Switching Waveforms
Read Cycle No. 1^[12, 13]

Read Cycle No. 2 (\overline{OE} Controlled)^[13, 14]

Notes:

11. AC characteristics (except High-Z) for all 8-ns and 10-ns parts are tested using the load conditions shown in Figure (a). All other speeds are tested using the Thevenin load shown in Figure (b). High-Z characteristics are tested for all speeds using the test load shown in Figure (d).
12. Device is continuously selected. OE, CE, BHE and/or BHE = V_{IL} .
13. WE is HIGH for Read cycle.
14. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[15, 16]

Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)

Notes:

15. Data I/O is high-impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{\text{IH}}$.
 16. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} LOW)

Truth Table

| CE | OE | WE | BLE | BHE | I/O ₀ -I/O ₇ | I/O ₈ -I/O ₁₅ | Mode | Power |
|----|----|----|-----|-----|------------------------------------|-------------------------------------|----------------------------|----------------------|
| H | X | X | X | X | High-Z | High-Z | Power-down | Standby (I_{SB}) |
| L | L | H | L | L | Data Out | Data Out | Read All Bits | Active (I_{CC}) |
| L | L | H | L | H | Data Out | High-Z | Read Lower Bits Only | Active (I_{CC}) |
| L | L | H | H | L | High-Z | Data Out | Read Upper Bits Only | Active (I_{CC}) |
| L | X | L | L | L | Data In | Data In | Write All Bits | Active (I_{CC}) |
| L | X | L | L | H | Data In | High-Z | Write Lower Bits Only | Active (I_{CC}) |
| L | X | L | H | L | High-Z | Data In | Write Upper Bits Only | Active (I_{CC}) |
| L | H | H | X | X | High-Z | High-Z | Selected, Outputs Disabled | Active (I_{CC}) |

Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range | |
|------------|---------------------|---------------------|--|--|------------|
| 10 | CY7C1041CV33-10BAC | BA48B | 48-ball Fine Pitch BGA | Commercial | |
| | CY7C1041CV33-10BAXC | BA48B | 48-ball Fine Pitch BGA (Pb-Free) | | |
| | CY7C1041CV33-10VC | V34 | 44-lead (400-mil) Molded SOJ | | |
| | CY7C1041CV33-10VXC | V34 | 44-lead (400-mil) Molded SOJ (Pb-Free) | | |
| | CY7C1041CV33-10ZC | Z44 | 44-pin TSOP II Z44 | | |
| | CY7C1041CV33-10ZXC | Z44 | 44-pin TSOP II Z44 (Pb-Free) | | |
| | 10 | CY7C1041CV33-10BAI | BA48B | 48-ball Fine Pitch BGA | Industrial |
| | | CY7C1041CV33-10BAXI | BA48B | 48-ball Fine Pitch BGA (Pb-Free) | |
| | | CY7C1041CV33-10VI | V34 | 44-lead (400-mil) Molded SOJ | |
| | | CY7C1041CV33-10ZI | Z44 | 44-pin TSOP II Z44 | |
| | | CY7C1041CV33-10ZXI | Z44 | 44-pin TSOP II Z44 (Pb-Free) | |
| | | | | | |
| 12 | CY7C1041CV33-12BAC | BA48B | 48-ball Fine Pitch BGA | Commercial | |
| | CY7C1041CV33-12VC | V34 | 44-lead (400-mil) Molded SOJ | | |
| | CY7C1041CV33-12VXC | V34 | 44-lead (400-mil) Molded SOJ (Pb-Free) | | |
| | CY7C1041CV33-12ZC | Z44 | 44-pin TSOP II Z44 | | |
| | CY7C1041CV33-12ZXC | Z44 | 44-pin TSOP II Z44 (Pb-Free) | | |
| | 12 | CY7C1041CV33-12BAI | BA48B | 48-ball Fine Pitch BGA | Industrial |
| | | CY7C1041CV33-12BAXI | BA48B | 48-ball Fine Pitch BGA (Pb-Free) | |
| | | CY7C1041CV33-12VI | V34 | 44-lead (400-mil) Molded SOJ | |
| | | CY7C1041CV33-12VXI | V34 | 44-lead (400-mil) Molded SOJ | |
| | | CY7C1041CV33-12ZI | Z44 | 44-pin TSOP II Z44 | |
| | | CY7C1041CV33-12ZXI | Z44 | 44-pin TSOP II Z44 (Pb-Free) | |
| | | | | | |
| 15 | CY7C1041CV33-15BAC | BA48B | 48-ball Fine Pitch BGA | Commercial | |
| | CY7C1041CV33-15VC | V34 | 44-lead (400-mil) Molded SOJ | | |
| | CY7C1041CV33-15VXC | V34 | 44-lead (400-mil) Molded SOJ (Pb-Free) | | |
| | CY7C1041CV33-15ZC | Z44 | 44-pin TSOP II Z44 | | |
| | CY7C1041CV33-15ZXC | Z44 | 44-pin TSOP II Z44 (Pb-Free) | | |
| | 15 | CY7C1041CV33-15BAI | BA48B | 48-ball Fine Pitch BGA | Industrial |
| | | CY7C1041CV33-15VI | V34 | 44-lead (400-mil) Molded SOJ | |
| | | CY7C1041CV33-15VXI | V34 | 44-lead (400-mil) Molded SOJ (Pb-Free) | |
| | | CY7C1041CV33-15ZI | Z44 | 44-pin TSOP II Z44 | |
| | | CY7C1041CV33-15ZXI | Z44 | 44-pin TSOP II Z44 (Pb-Free) | |
| 20 | CY7C1041CV33-20BAC | BA48B | 48-ball Fine Pitch BGA | Commercial | |
| | CY7C1041CV33-20VC | V34 | 44-lead (400-mil) Molded SOJ | | |
| | CY7C1041CV33-20VXC | V34 | 44-lead (400-mil) Molded SOJ (Pb-Free) | | |
| | CY7C1041CV33-20ZC | Z44 | 44-pin TSOP II Z44 | | |
| | CY7C1041CV33-20ZXC | Z44 | 44-pin TSOP II Z44 (Pb-Free) | | |
| | 20 | CY7C1041CV33-20BAI | BA48B | 48-ball Fine Pitch BGA | Industrial |
| | | CY7C1041CV33-20VI | V34 | 44-lead (400-mil) Molded SOJ | |
| | | CY7C1041CV33-20ZI | Z44 | 44-pin TSOP II Z44 | |
| | | CY7C1041CV33-20ZXI | Z44 | 44-pin TSOP II Z44 (Pb-Free) | |

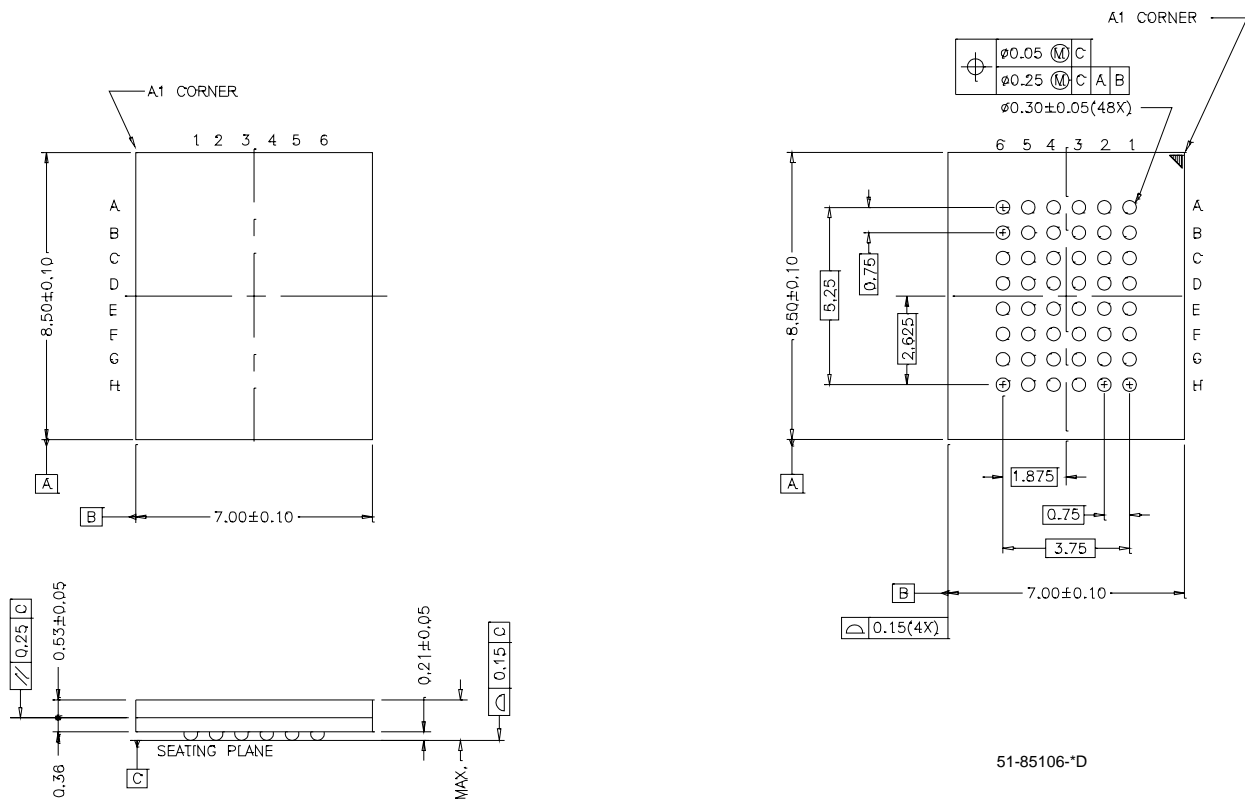
Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|---------------------|--------------|--|-----------------|
| 20 | CY7C1041CV33-20BAE | BA48B | 48-ball Fine Pitch BGA | Automotive |
| | CY7C1041CV33-20VE | V34 | 44-lead (400-mil) Molded SOJ | |
| | CY7C1041CV33-20VXE | V34 | 44-lead (400-mil) Molded SOJ (Pb-Free) | |
| | CY7C1041CV33-20ZE | Z44 | 44-pin TSOP II Z44 | |
| | CY7C1041CV33-20ZSXE | Z44 | 44-pin TSOP II Z44 (Pb-Free) | |

Package Diagrams
48-ball (7.00 mm x 8.50 mm x 1.2 mm) FBGA BA48B

TOP VIEW

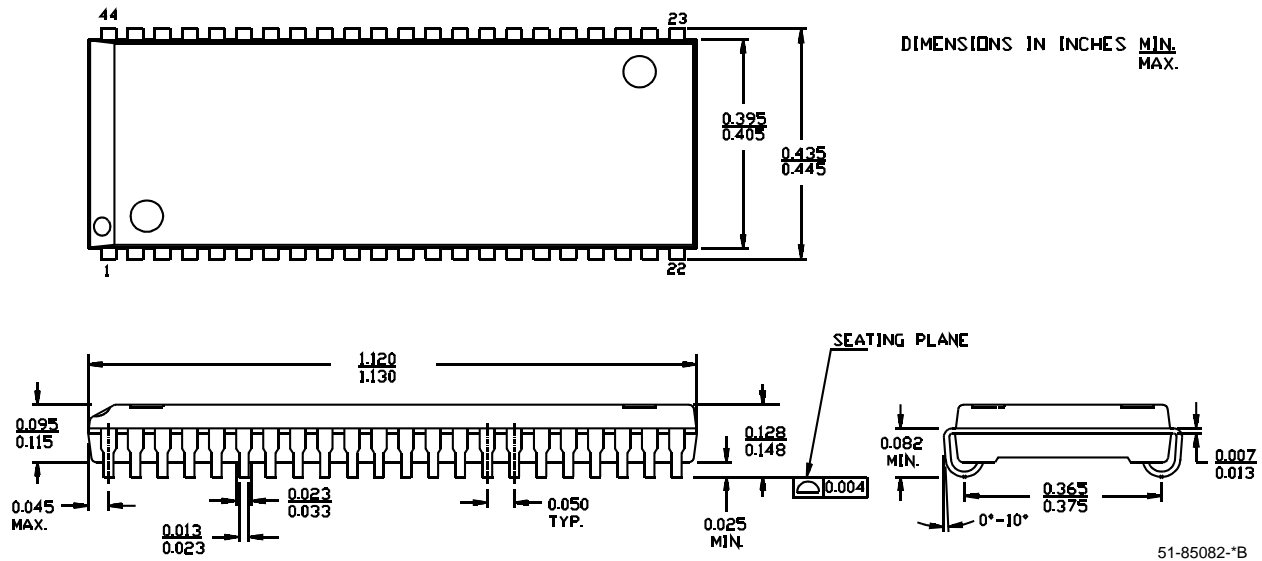
BOTTOM VIEW



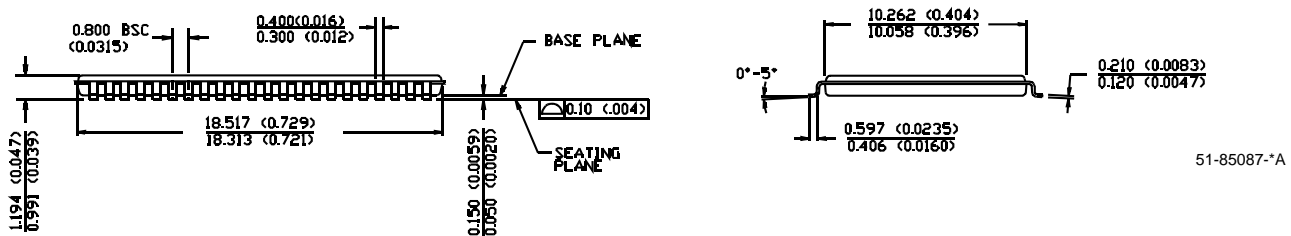
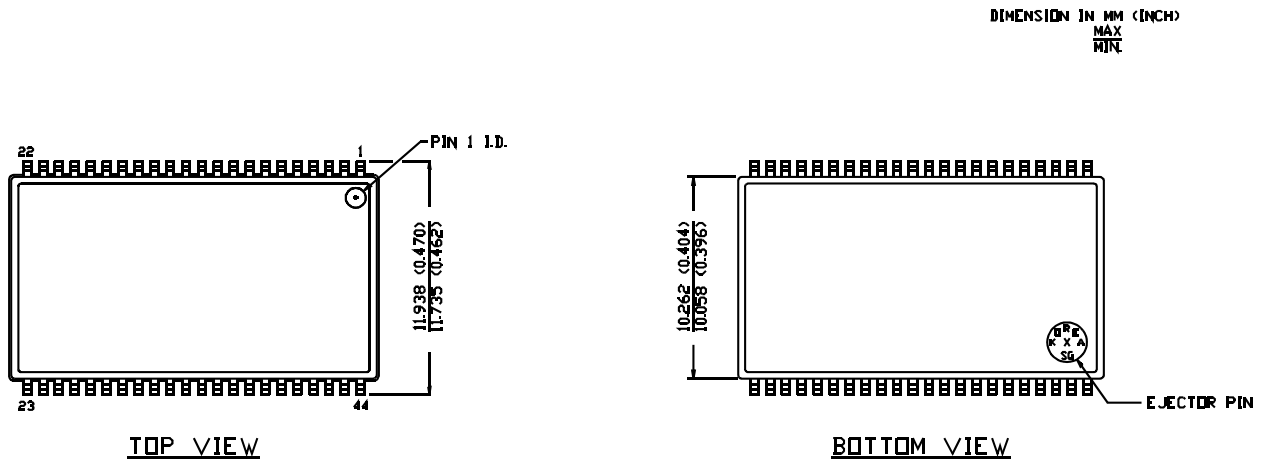
51-85106-D

Package Diagrams (continued)

44-lead (400-mil) Molded SOJ V34



44-pin TSOP II Z44



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Document History Page

| Document Title: CY7C1041CV33 4-Mbit (256K x 16) Static RAM | | | | |
|--|---------|------------|-----------------|--|
| Document Number: 38-05134 | | | | |
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 109513 | 12/13/01 | HGK | New Data Sheet |
| *A | 112440 | 12/20/01 | BSS | Updated 51-85106 from revision *A to *C |
| *B | 112859 | 03/25/02 | DFP | Added CY7C1042CV33 in BGA package Removed 1042 BGA option pin ACC Final Data Sheet |
| *C | 116477 | 09/16/02 | CEA | Add applications foot note to data sheet |
| *D | 119797 | 10/21/02 | DFP | Added 20-ns speed bin |
| *E | 262949 | See ECN | RKF | 1) Added Lead (Pb)-Free parts in the Ordering info (Page #9) 2) Added Automotive Specs to Datasheet |
| *F | 361795 | See ECN | SYT | Added Pb-Free offerings in the Ordering Information |