CY62168DV30
MoBL®

16-Mbit (2048K x 8) MoBL® Static RAM

Features

- **Very high speed: 55 ns and 70 ns**
  - **Wide voltage range: 2.20V – 3.60V**
- **Ultra-low active power**
  - **Typical active current: 2 mA @ f = 1 MHz**
  - **Typical active current: 15 mA @ f = f_{max}**
- **Ultra-low standby power**
- **Easy memory expansion with $\overline{CE}_1$, CE_2 and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Packages offered in a 48-ball FBGA**

Functional Description[1]

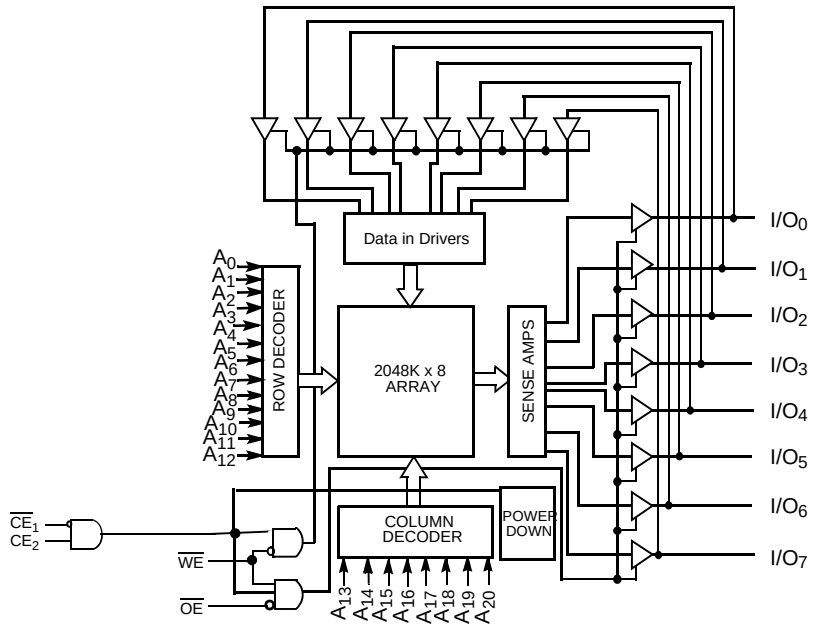
The CY62168DV30 is a high-performance CMOS static RAMs organized as 2048Kbit words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. The device can be put into standby mode reducing power consumption by 90% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected Chip Enable 1 ($\overline{CE}_1$) HIGH or Chip Enable 2 (CE_2) LOW. The input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when: deselected Chip Enable 1 ($\overline{CE}_1$) HIGH or Chip Enable 2 (CE_2) LOW, outputs are disabled ($\overline{OE}$ HIGH), or during a write operation (Chip Enable 1 ($\overline{CE}_1$) LOW and Chip Enable 2 (CE_2) HIGH and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable 1 ($\overline{CE}_1$) LOW and Chip Enable 2 (CE_2) HIGH and Write Enable ($\overline{WE}$) input LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins(A_0 through A_{20}).

Reading from the device is accomplished by taking Chip Enable 1 ($\overline{CE}_1$) and Output Enable ($\overline{OE}$) LOW and Chip Enable 2 (CE_2) HIGH while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ LOW and CE_2 HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW and CE_2 HIGH and $\overline{WE}$ LOW). See the truth table for a complete description of read and write modes.

Logic Block Diagram

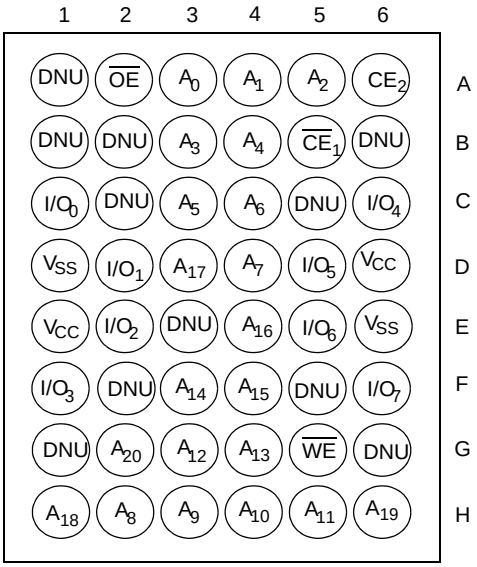


Note:
1. For best-practice recommendations, please refer to the Cypress application note entitled *System Design Guidelines*, available at http://www.cypress.com.

Pin Configuration[2]

FBGA

Top View



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (μA)	
					f = 1 MHz		f = f_{max}			
	Min.	Typ.[3]	Max.		Typ.[3]	Max.	Typ.[3]	Max.	Typ.[3]	Max.
CY62168DV30L	2.2	3.0	3.6	55	2	4	15	30	2.5	30
				70			12	25		
CY62168DV30LL	2.2	3.0	3.6	55	2	4	15	30	2.5	22
				70			12	25		

Notes:
2. DNU pins have to be left floating or tied to V_{SS} to ensure proper application.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25°C$.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential ..... –0.3V to $V_{CC(max)}$ + 0.3V

DC Voltage Applied to Outputs in High-Z State[4, 5] ..... –0.3V to $V_{CC(max)}$ + 0.3V

DC Input Voltage[4, 5] .....–0.3V to $V_{CC(max)}$ + 0.3V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature (T_A)[6]	V_{CC}[7]
Industrial	–40°C to +85°C	2.2V – 3.6V

DC Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions		CY62168DV30-55 Min.	CY62168DV30-55 Typ.[3]	CY62168DV30-55 Max.	CY62168DV30-70 Min.	CY62168DV30-70 Typ.[3]	CY62168DV30-70 Max.	Unit
V_{OH}	Output HIGH Voltage	$2.2 \le V_{CC} \le 2.7$	I_{OH} = –0.1 mA	2.0			2.0			V
		$2.7 \le V_{CC} \le 3.6$	I_{OH} = –1.0 mA	2.4			2.4			
V_{OL}	Output LOW Voltage	$2.2 \le V_{CC} \le 2.7$	I_{OL} = 0.1 mA			0.4			0.4	V
		$2.7 \le V_{CC} \le 3.6$	I_{OH} = 2.1 mA			0.4			0.4	
V_{IH}	Input HIGH Voltage	$2.2 \le V_{CC} \le 2.7$		1.8		V_{CC} + 0.3	1.8		V_{CC} + 0.3	V
		$2.7 \le V_{CC} \le 3.6$		2.2		V_{CC} + 0.3	2.2		V_{CC} + 0.3	
V_{IL}	Input LOW Voltage	$2.2 \le V_{CC} \le 2.7$		–0.3		0.6	–0.3		0.6	V
		$2.7 \le V_{CC} \le 3.6$		–0.3		0.8	–0.3		0.8	
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		–1		+1	–1		+1	µA
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CC}$, Output disabled		–1		+1	–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$	V_{CC} = 3.6V, I_{OUT} = 0 mA, CMOS level		15	30		12	25	mA
		f = 1 MHz			2	4		2	4	
I_{SB1}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE}_1 \ge V_{CC} - 0.2V$, $CE_2 \le 0.2V$, $V_{IN} \ge V_{CC} - 0.2V$, $V_{IN} \le 0.2V$, $f = f_{MAX}$ (Address and Data Only), f = 0 (OE, WE)	L		2.5	30		2.5	30	µA
			LL		2.5	22		2.5	22	
I_{SB2}	Automatic CE Power-down Current— CMOS Inputs	$\overline{CE}_1 \ge V_{CC} - 0.2V$, $CE_2 \le 0.2V$, $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$, f = 0, V_{CC} = 3.6V	L		2.5	30		2.5	30	µA
			LL		2.5	22		2.5	22	

Thermal Resistance

Parameter	Description	Test Conditions	BGA	Unit
Θ_{JA}	Thermal Resistance[8] (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, four-layer printed circuit board	55	°C/W
Θ_{JC}	Thermal Resistance[8] (Junction to Case)		16	°C/W

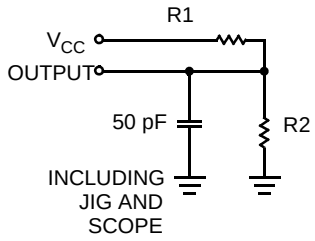
Notes:

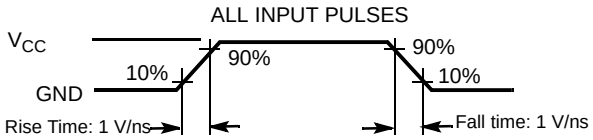
4. $V_{IL(min)}$ = –0.2V for pulse durations less than 20 ns.
5. $V_{IH(max)}$ = V_{CC} + 0.75V for pulse durations less than 20 ns.
6. T_A is the "Instant-On" case temperature.
7. Full device AC operation assumes a 100 µs ramp time from 0 to V_{CC}(min) and 100 µs wait time after V_{CC} stabilization.
8. Tested initially and after any design or process changes that may affect these parameters.

Capacitance[8]

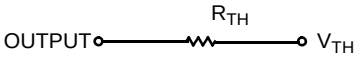
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ.)}$	8	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT

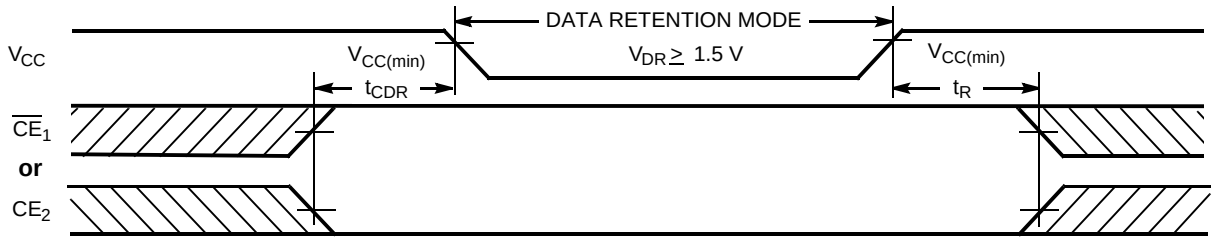


Parameters	2.50V	3.0V	Unit
R1	16600	1103	Ω
R2	15400	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.2	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions		Min.	Typ.[3]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			1.5		3.6	V
I_{CCDR}	Data Retention Current	V_{CC} = 1.5V $\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	L			15	µA
			LL			10	µA
t_{CDR}[8]	Chip Deselect to Data Retention Time			0			ns
t_R[9]	Operation Recovery Time			t_{RC}			ns

Data Retention Waveform



Note:
9. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.

Switching Characteristics Over the Operating Range [10]

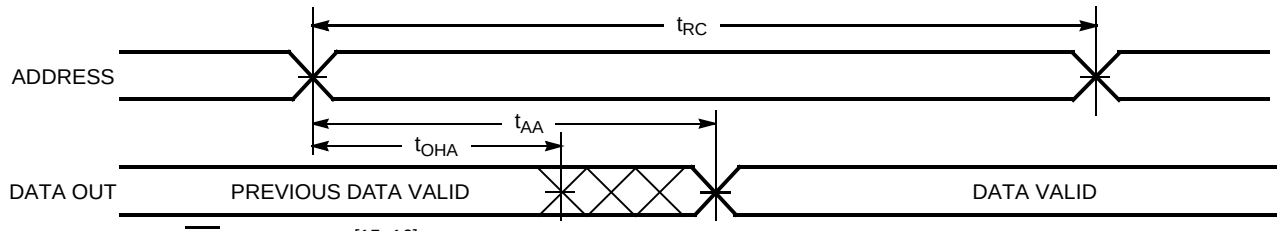
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Data Valid		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[11]	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[11, 12]		20		25	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[11]	10		10		ns
t_{HZCE}	$\overline{CE}_1$ HIGH or CE_2 LOW to High Z[11, 12]		20		25	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power-Up	0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH or CE_2 LOW to Power-Down		55		70	ns
Write Cycle[13]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Write End	40		60		ns
t_{AW}	Address Set-Up to Write End	40		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	40		45		ns
t_{SD}	Data Set-Up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[11, 12]		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[11]	10		10		ns

Notes:

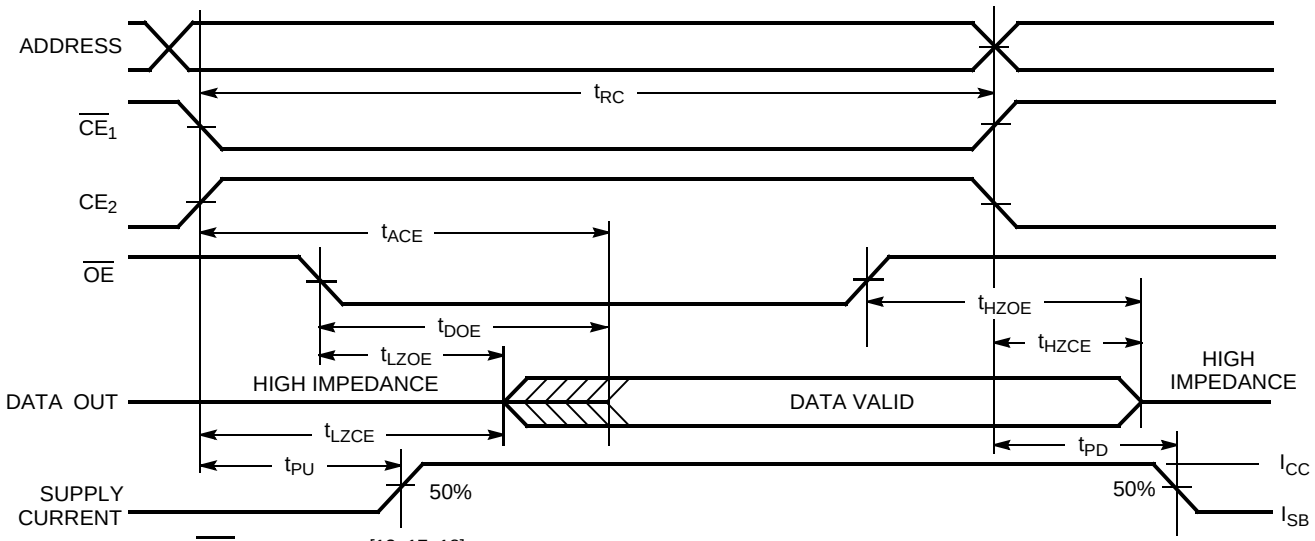
10. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3ns or less (1V/ns), timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the “AC Test Loads and Waveforms” section.
11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
12. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
13. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

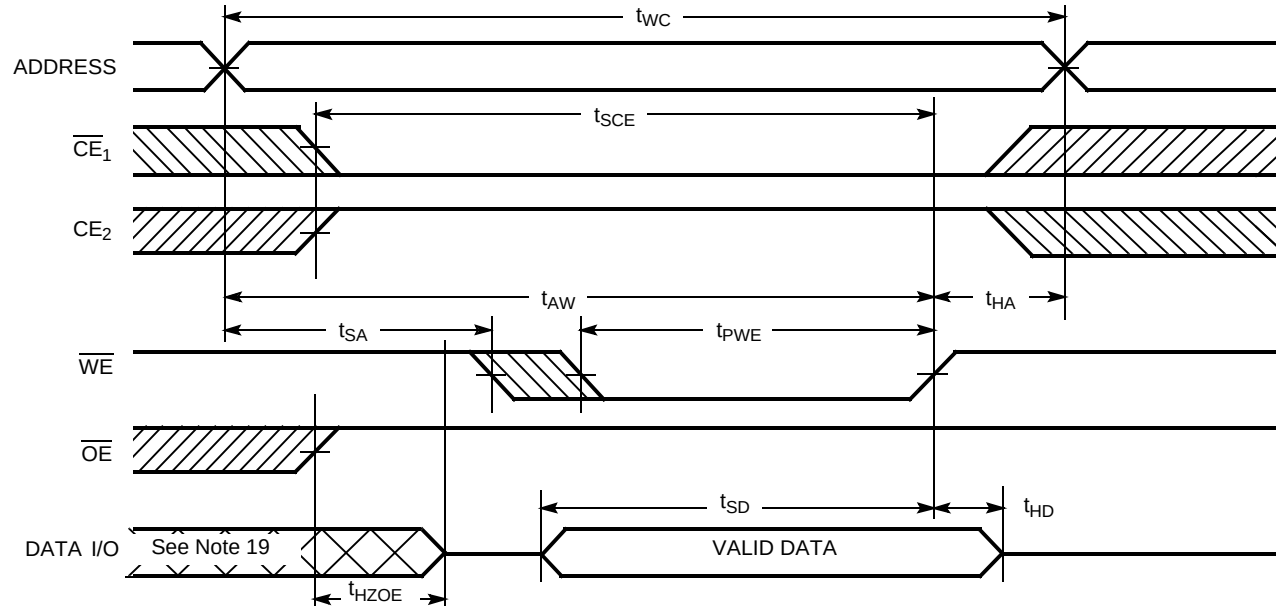
Read Cycle No. 1 (Address Transition Controlled)[14, 15]



Read Cycle No. 2 ($\overline{OE}$ Controlled)[15, 16]



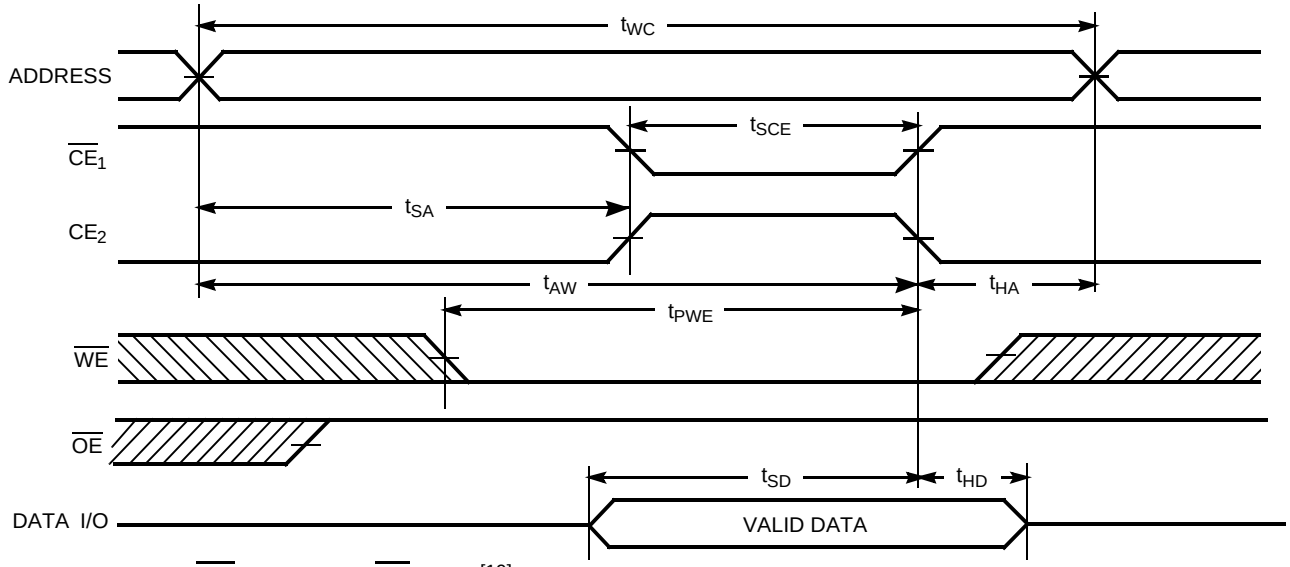
Write Cycle No. 1 ($\overline{WE}$ Controlled)[13, 17, 18]



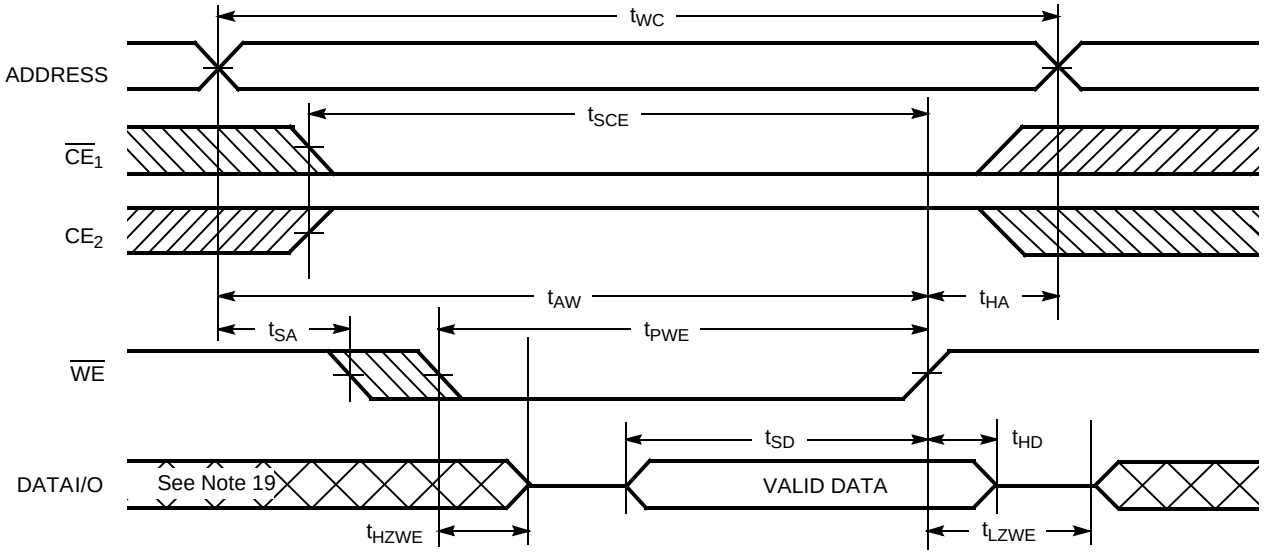
Notes:
14. Device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, CE_2 = V_{IH}.
15. $\overline{WE}$ is HIGH for read cycle.
16. Address valid prior to or coincident with $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.
17. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
18. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high-impedance state.
19. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE_1}$ or CE_2 Controlled)[13, 17, 18]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[19]



Truth Table

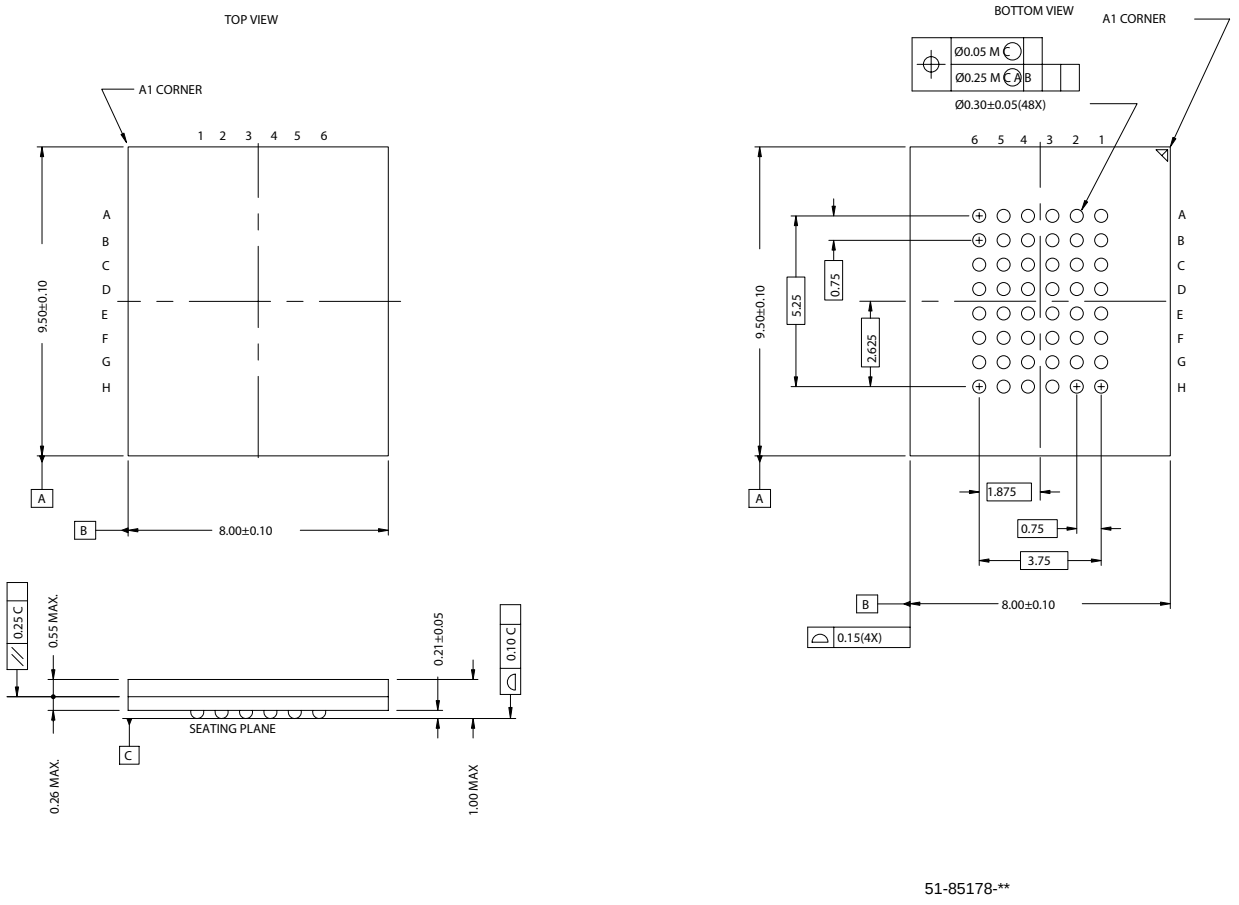
$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X	L	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	Data Out (I/O_0-I/O_7)	Read	Active (I_{CC})
L	H	H	H	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	Data in (I/O_0-I/O_7)	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62168DV30L-55BVXI	BV48B	48-ball Fine Pitch BGA (8.0 x 9.5 x 1.0 mm) (Pb-Free)	Industrial
	CY62168DV30LL-55BVXI	BV48B	48-ball Fine Pitch BGA (8.0 x 9.5 x 1.0 mm) (Pb-Free)	
70	CY62168DV30L-70BVXI	BV48B	48-ball Fine Pitch BGA (8.0 x 9.5 x 1.0 mm) (Pb-Free)	Industrial
	CY62168DV30LL-70BVXI	BV48B	48-ball Fine Pitch BGA (8.0 x 9.5 x 1.0 mm) (Pb-Free)	

Package Diagrams

48-Lead VFBGA (8 x 9.5 x 1 mm) BV48B



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Document History Page

Document Title: CY62168DV30 MoBL® 16-Mbit (2048K x 8) Static RAM Document Number: 38-05329				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	118409	09/30/02	GUG	New Data Sheet
*A	123693	02/05/03	DPM	Changed Advance Information to Preliminary Added package diagram
*B	126556	04/24/03	DPM	Minor change: Change sunset owner from DPM to HRT
*C	132869	01/15/04	XRJ	Changed Preliminary to Final
*D	272589	See ECN	PCI	Updated Final data sheet and added Pb-free package.
*E	335864	See ECN	PCI	Removed redundant packages from Ordering Information Table Added Address A_{20} to ball G2 in the Pin Configuration